The **8085 Microprocessor** is an 8-bit general-purpose microprocessor introduced by Intel in 1976. It is a classic piece of hardware often used to teach the fundamentals of computer architecture and assembly language.

Core Specifications

The "8" in 8085 stands for its 8-bit data bus, while the "5" indicates it uses a single **+5V** power supply.

Feature	Specification
Data Bus	8-bit (can process 8 bits of data at once)
Address Bus	16-bit (can address $2^{16} = 65,536$ or 64KB of memory)
Clock Frequency	Typically 3 MHz
Transistors	Approximately 6,500
Package	40-pin DIP (Dual In-line Package)

Architecture Highlights

The 8085 architecture consists of three main units: the **ALU**, the **Control Unit**, and the **Registers**.

- **ALU (Arithmetic Logic Unit):** Performs arithmetic (addition, subtraction) and logic operations (AND, OR, XOR).
- **Accumulator (A):** An 8-bit register that is part of the ALU. It stores the result of most operations.
- **Flags Register:** A 5-bit status register that indicates the results of operations (Sign, Zero, Auxiliary Carry, Parity, and Carry).

Internal Registers

The 8085 has several registers to store data temporarily:

1. **General Purpose Registers:** Six 8-bit registers (B, C, D, E, H, and L). They can be used in pairs (BC, DE, HL) to handle 16-bit data.
2. **Program Counter (PC):** A 16-bit register that holds the memory address of the **next** instruction to be executed.
3. **Stack Pointer (SP):** A 16-bit register used to point to the current location in the stack memory.

Pin Configuration & Signals

The 8085 uses a multiplexed address/data bus to save pins.

- **AD0–AD7:** Multiplexed Address/Data lines. They carry the lower 8 bits of the address during the first clock cycle and data during later cycles.
- **A8–A15:** High-order address lines.
- **ALE (Address Latch Enable):** A signal used to tell external hardware whether the bus is currently carrying an address or data.
- **Interrupts:** It has five hardware interrupts: **TRAP** (highest priority), **RST 7.5**, **RST 6.5**, **RST 5.5**, and **INTR**.

Summary Table: Interrupt Priorities

Interrupt	Type	Priority
TRAP	Non-maskable (Edge & Level)	1 (Highest)
RST 7.5	Maskable (Edge sensitive)	2
RST 6.5	Maskable (Level sensitive)	3
RST 5.5	Maskable (Level sensitive)	4
INTR	Maskable (Level sensitive)	5 (Lowest)

Pro-Tip: The **HL register pair** is also known as the "Memory Pointer" because many instructions use it to point to a memory location (referenced as 'M' in assembly).