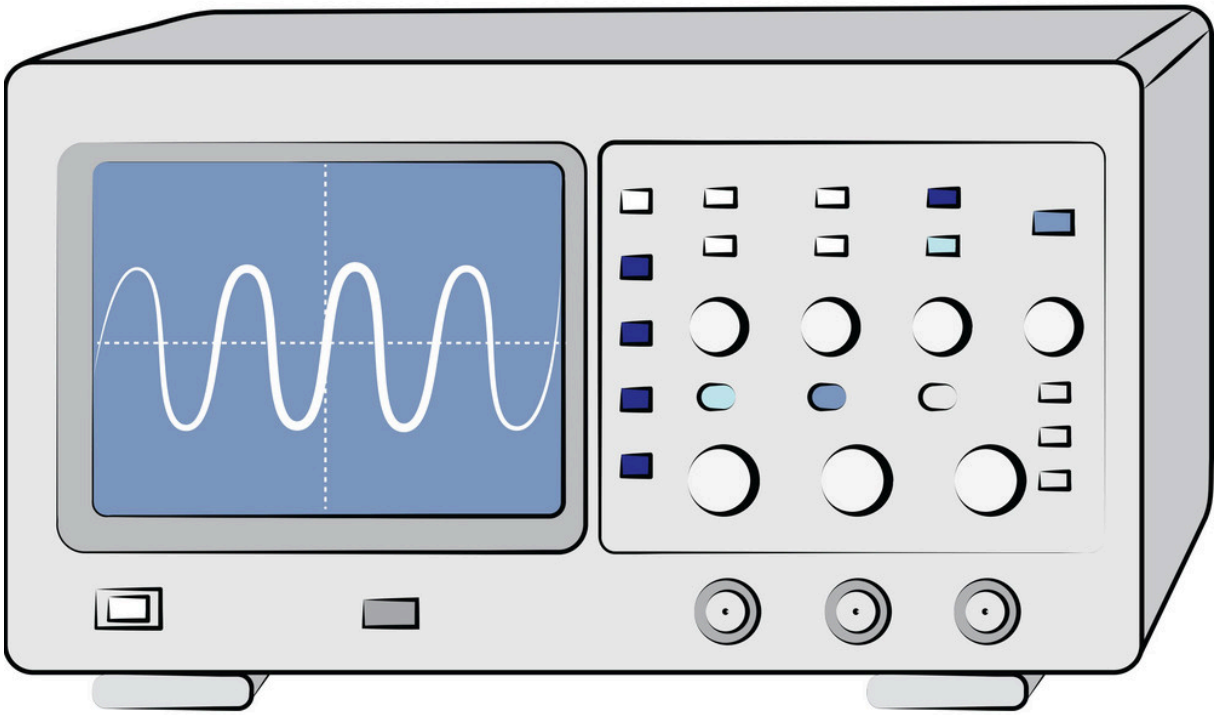

22/02/2024

Quickscope - FPGA based oscilloscope

Project specifications

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1. Project brief

The project consists of a Basic Oscilloscope based on a Nexys Video FPGA board.

The system uses the internal 12 bits 4 channels ADC to read Analog values from a PMOD connector. It then shows the Analog values over time on screen through an HDMI connection

1.1. Equipement

- Nexys Video
- PMOD Rotary Encoder
- HDMI screen
- Probe / cable (PMOD compatible)

2. Project schematics

2.1. General

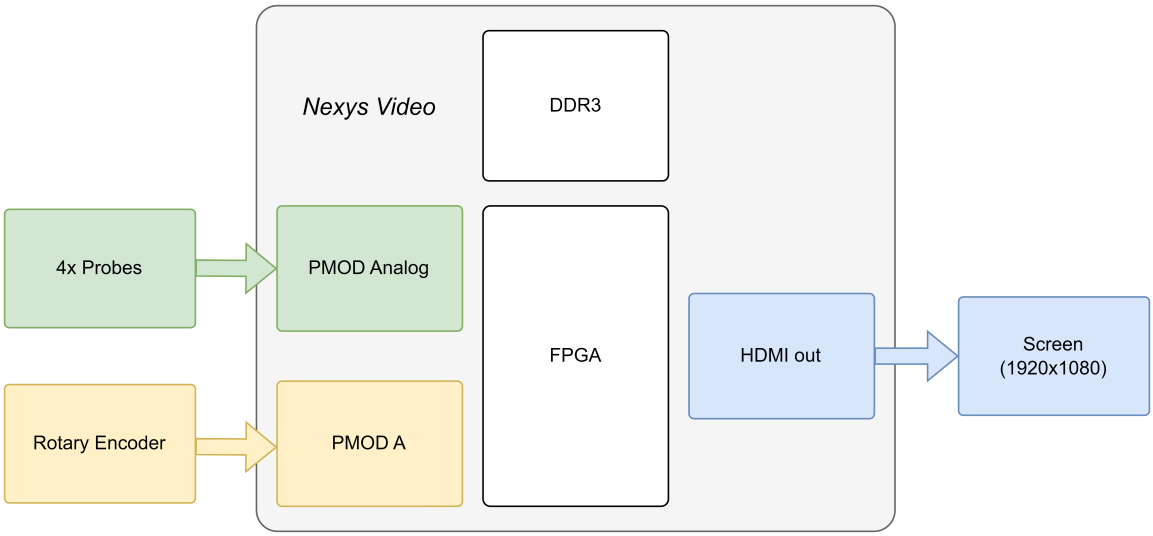

Figure 1: General Architecture of the system

2.2. Internal

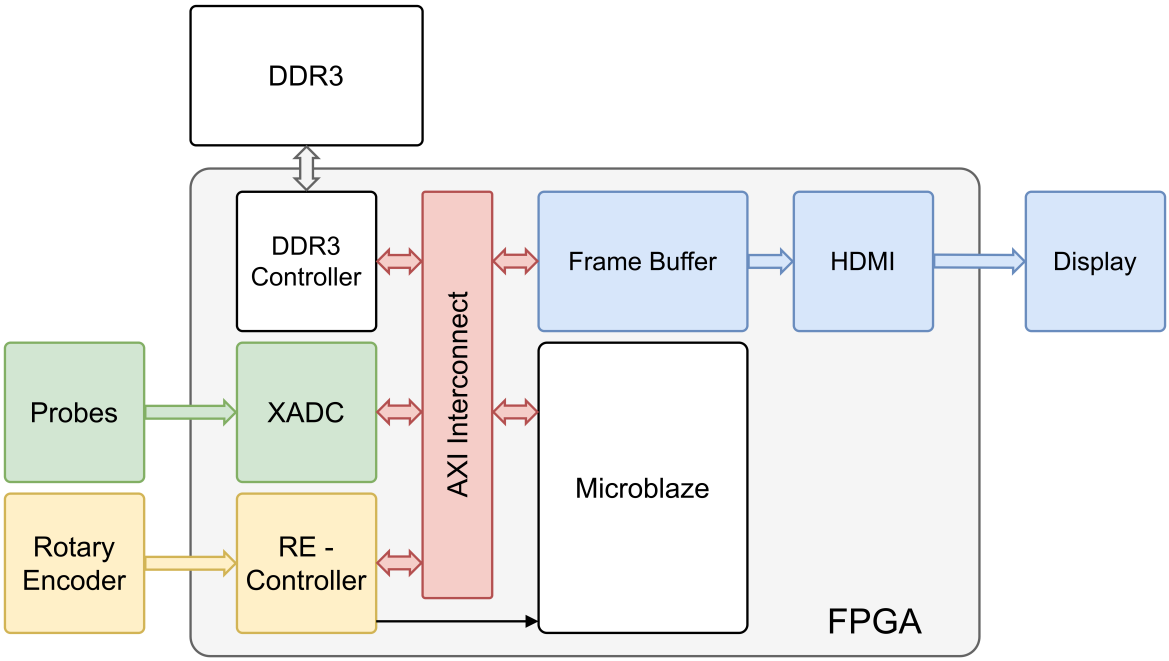

Figure 2: Internal detailed diagram describing inner connections and specifics

3. Imperatives

- 4x Analog Inputs
- Voltage range 0V - 5V
- Maximum 1 Mega sample / s
- 1920x1080 at 60 FPS
- Ajustable parameters
  - Sampling rate
  - Vertical scale (Amplitude)
  - Horizontal scale (Time)

4. Register decriptions

4.1. Rotary encoder

4.1.1. Data Register [RO]

31 - 3	2	1	0
X	BUTTON	ROTATE LEFT	ROTATE RIGHT

Table 1: Rotary Encoder Value Register

4.1.2. Clear interrupt Register [WO]

31 - 1	0
X	CLEAR

Table 2: Rotary Encoder Clear Interrupt Register

4.2. Screen layout

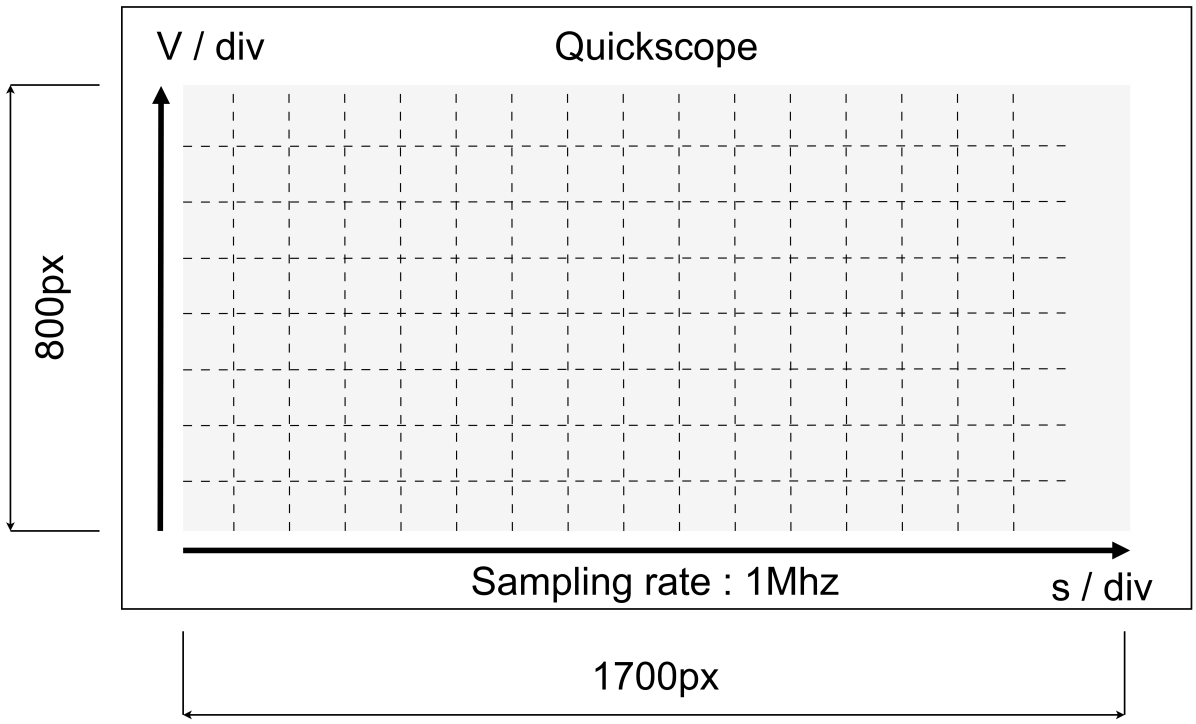

Figure 3: Frame organization 1920x1080 screen.

Each **Analog Input** has its own **vector** containing the pixels to show on the screen.

Each vector has **11 bits of address** (screen width = 1920 and 1920px < 2^11 - 1) saved as **10 bits data** (traces area is 800px and 800 < 2^10 −1) into the BRAM.

There is no real fully-fledged framebuffer, only the analog data are dynamic. This means the only changing part of the screen if the gray part containing the traces. The other parts are saved as bitmaps into the BRAM.

5. Pseudo-code Microblaze

```
void main()
{
  read_last_values_adc();
  update_display();
}

void routine_interrupt_re()
{
  value = read_reg_value_re();

  switch(value)
  {
    case LEFT:
      left();
    case RIGHT:
      right();
    default:
  }

  if(value == BUTTON_PRESSED)
    select();
}
```

6. Project planning

Due date : 06 / 05 / 2024

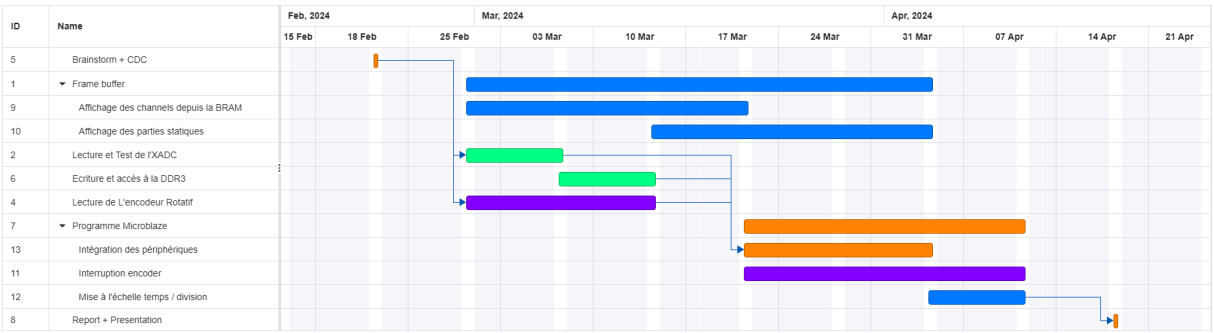

Figure 4: GANTT planning diagram (10 weeks)

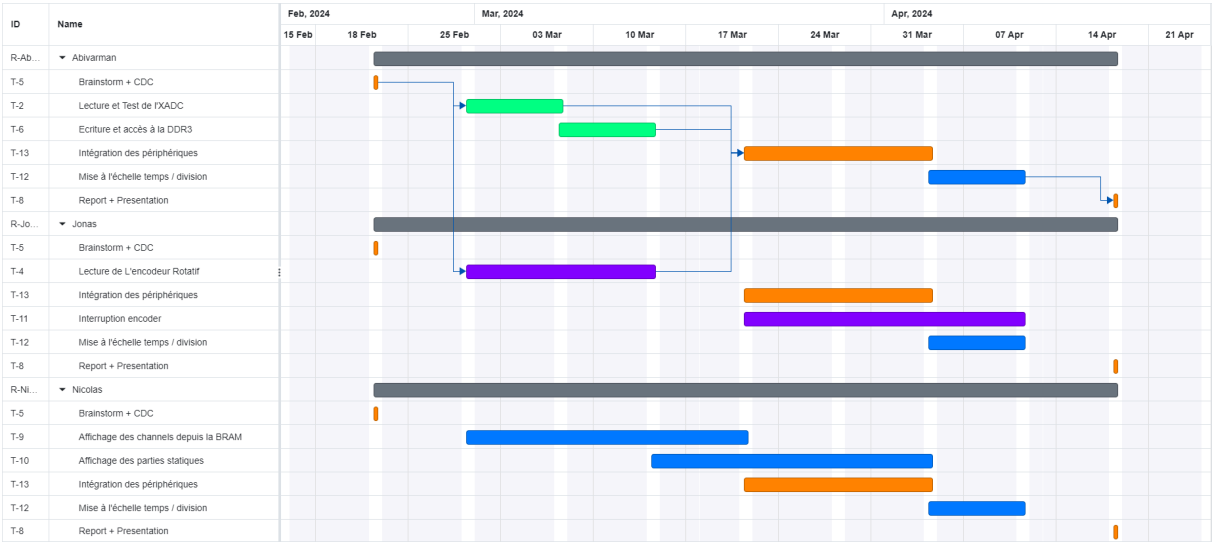

Figure 5: GANTT resources repartitions