CEE-325 Digital System Design
Exam 1 Review

WRITE YOUR NAME HERE: _____

1. (15 pts) Construct a Verilog HDL module for the combinational logic in Figure 1. Use the structural modeling technique with built-in primitives for logic gates such as NAND, OR gates and others to construct the module below:

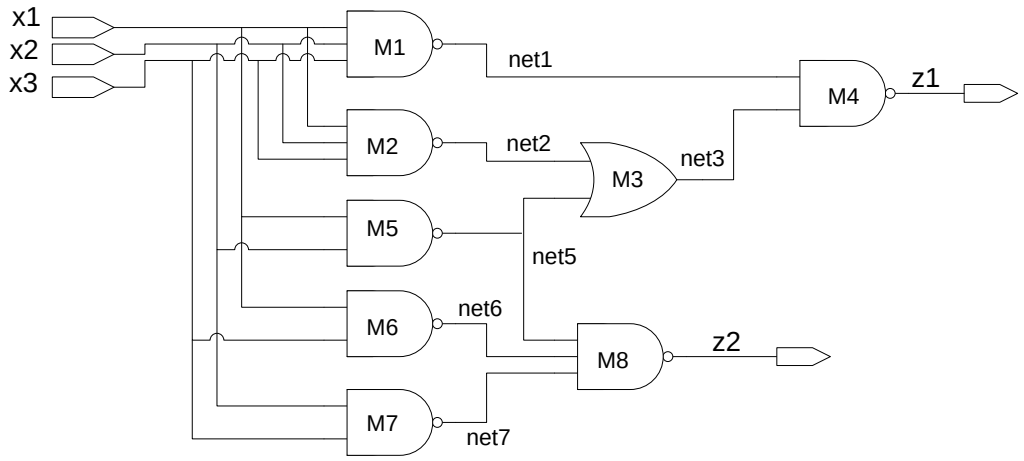


Figure 1 logic network with built-in Verilog HDL gate primitives

2. (15 pts) Develop a truth table for the combinational logic network in Figure 2

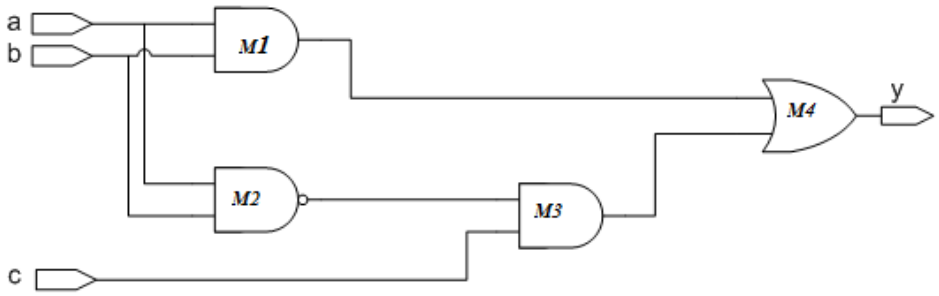


Figure 2 Combinational circuit

Truth table:

a	b	c	y

3. (15 pts) Construct a K-map for the logic network in Figure 2 **and** find the optimized/minimized Boolean equation from K-map in a sum of product (SOP) form.

4. (10 pts) Develop a structural model in Verilog HDL for the logic network in Fig. 2 using the gate-level primitives such as AND, NAND and OR gates.

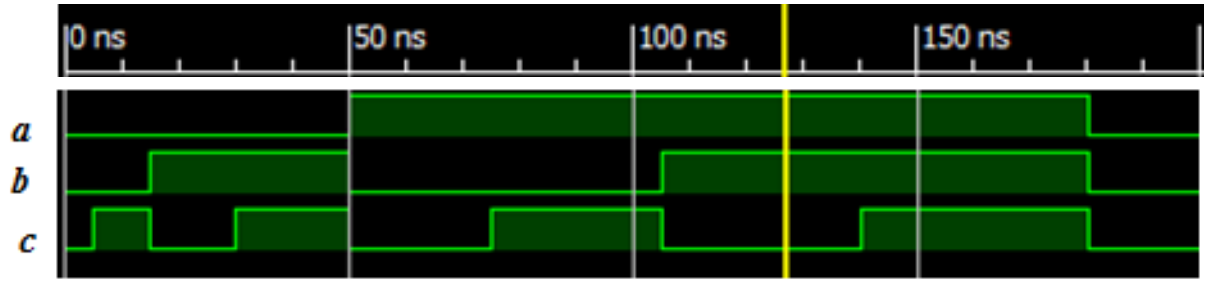
5. (10 pts) Write a test bench fixture/program to verify the logic network in Fig. 2. Use the input test vectors (a, b, and c) to verify its output (y). The simulation output you obtain from this test bench program should produce the **same output file** as shown in Fig. 3.

```
ISim M.70d (signature 0x36e8438f)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Time=     1.0ns, a=0, b=0, c=0, y=0
Time=     6.0ns, a=0, b=0, c=1, y=1
Time=    16.0ns, a=0, b=1, c=0, y=0
Time=    31.0ns, a=0, b=1, c=1, y=1
Time=    51.0ns, a=1, b=0, c=0, y=0
Time=    76.0ns, a=1, b=0, c=1, y=1
Time=   106.0ns, a=1, b=1, c=0, y=1
Time=   141.0ns, a=1, b=1, c=1, y=1
Time=   181.0ns, a=0, b=0, c=0, y=0
ISim>
```

Fig. 3 simulation output

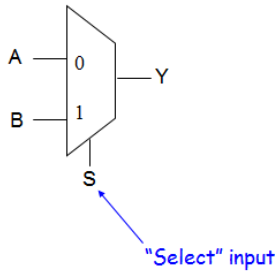
Test Bench

6. (10 pts) The input waveforms a, b, and c are applied to the logic network in Fig.2. Draw a timing diagram at the output node (y) in proper relation to the inputs. Make sure that your answer for the output y is properly lined up with the input waveforms.



Draw the timing diagram at the output node (y):

7. (15 pts) a 2 to 1 multiplexer:



1. Write a Behavioral Verilog HDL module to describe the multiplexer.

2. Draw a 2 to 1 multiplexer schematic using AND, OR, NOT, and/or other logic gates.

8. (10 pts) In the knight rider LED display exercise, we had the HDL code as shown below and the code has a gated clock issue: "gated clock: sourced by a combinational pin; it's not a good design practice". How do you fix the design issue? You can use IF and ELSE statement to rewrite the multiplexer implementation to eliminate the gated clock problem. Show the HDL code that would fix the problem in the space below.

assign shift_clock = speed ? fast_clock : slow_clock;

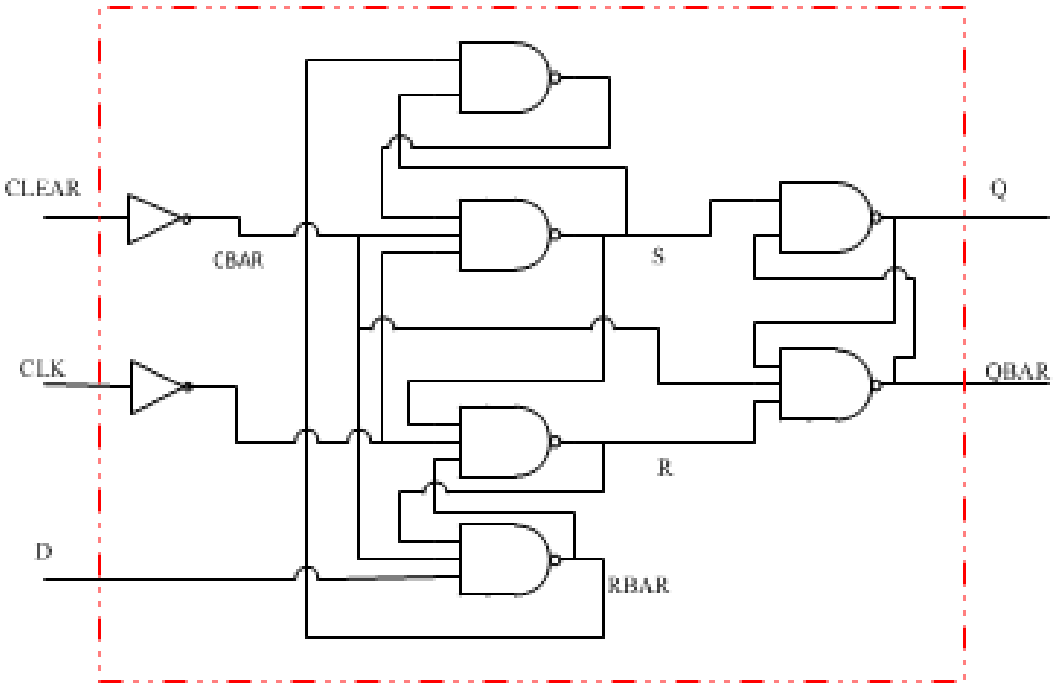
// where shift_clock is 'reg' data type and fast_clock and slow_clock are 'wire' data type.

⚠ WARNING:PhysDesignRules:372 - Gated clock.

9. Use the Case, if-else, and/or assign statements to create a Verilog modulle for the following circuits:

   a. Decoder (e.g. 2 to 4 decoder, 3 to 8 decoder etc.,)
   b. Multiplexer (e.g. 2 to 4 Mux, 3 to 8 Mux etc.,)
   c. Encoder

10. Answer the following two questions on the sequential circuit below:



A. What is the circuit called?
B. Create a Verilog module for the sequential circuit below:
C. Use the waveforms for data (D) and clock signal (CLK) to draw the timing waveform of the circuit at node Q. (Use the circuit as a negative-triggered device)