SM16206

Overview

SM16206 is a constant-current LED driver chip with a built-in CMOS shift register and latch function to convert serial input data to a parallel output.

The working voltage of the SM16206 is 3.3V – 5.0V. It includes 16 current sources, each of which can provide a constant current of 1 mA – 32 mA at each output port, with current variation of less than ± 2.5% within a single IC chip and less than ± 3.5% between multiple ICs. Channel output current does not vary with output voltage (V_{DS}) changes and varies by less than 1% due to voltage and ambient temperature. The output current of each channel is determined by the external resistor adjustment.

The output port of the SM16206 can withstand voltages up to +15V, so it can be used to drive series strings of multiple LEDs. In addition the SM16206 supports clock frequencies up to 25 MHz to meet the system's need for high data volumes.

Features

- 16-channel constant current source output
- Constant Current:

  1—32mA@VDD=5.0V

  Intra-chip error < ±2.5%, inter-chip error < ±3.5%

  1—22mA@VDD=3.3V

  Intra-chip error < ±2.5%, inter-chip error < ±3.5%
- Output current adjustable with external R_{ext} resistor
- Fast Output Current Response, $\overline{OE}$ (Min): 35ns
- Up to 25MHz clock frequency
- Working voltage: 3.3V~5.0V
- Package: SSOP24, QSOP24, QFN24(4*4)

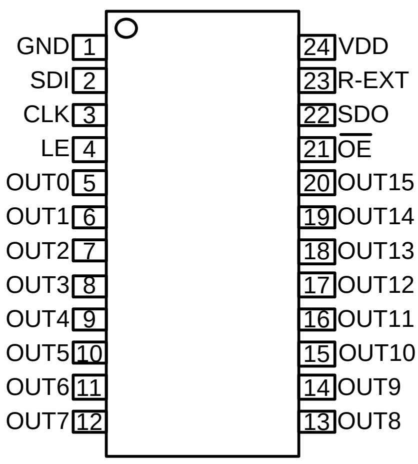
Applications

- LED Display
- LED Lighting

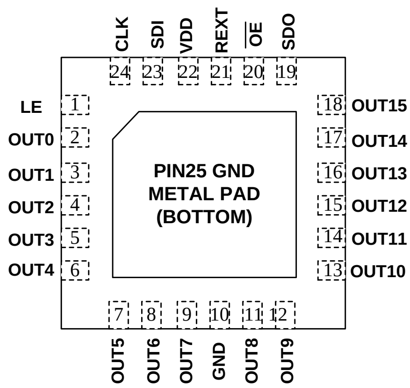
Package Information

Product	Package	Body Size (mm)	Pitch (mm)
SM16206D	SSOP24	13.0*6.0*1.8	1.0
SM16206S	QSOP24	8.65*3.9*1.4	0.635
SM16206N-2	QFN24(4*4)	4*4*0.85	0.5

Pin Definition



(SSOP24/QSOP24)



QFN24(4*4)

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Internal Functional Block Diagram

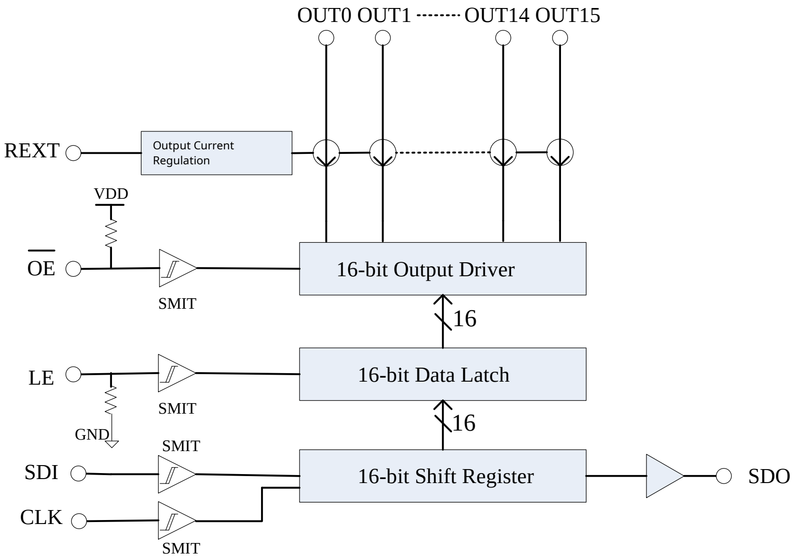


Fig. SM16206 Internal Functional Block Diagram

Pin Description

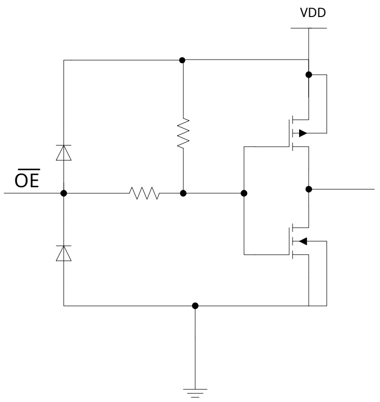
Pin	Function Description
GND	Chip ground
SDI	Serial Data input
CLK	Serial Clock input; data is shifted in on the rising edge of the clock
LE	Data Latch Control input; when LE is high the shift register output is transferred to the latch; when LE is low the latch holds its value
OUT0～OUT15	Constant Current Driver outputs
$\overline{OE}$	Output Enable control input; when $\overline{OE}$ is low, the OUT0~OUT15 outputs are active; when $\overline{OE}$ is high the OUT0~OUT15 outputs are disabled
SDO	Serial Data output; can be connected to the SDI port of the next chip
R-EXT	Input for external resistor; sets the output current of all output channels
VDD	Chip Power

Ordering Information

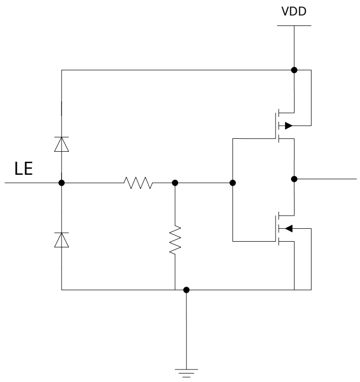
Model	Package	Packing		Reel size
		Tube	Tape	
SM16206D	SSOP24	36000 Pieces / box	2000 Pieces / box	13 inch
SM16206S	QSOP24	100000 Pieces / box	4000 Pieces / box	13 inch
SM16206N-2	QFN24(4*4)	/	5000 Pieces / box	13 inch

Output and Input Equivalent Circuits

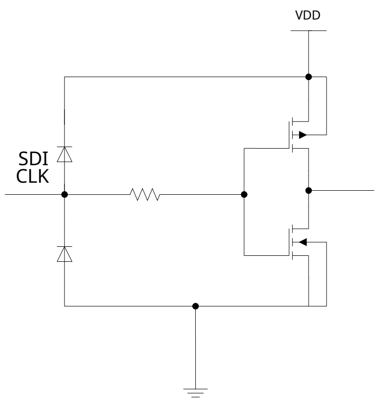
- $\overline{\text{OE}}$ Input



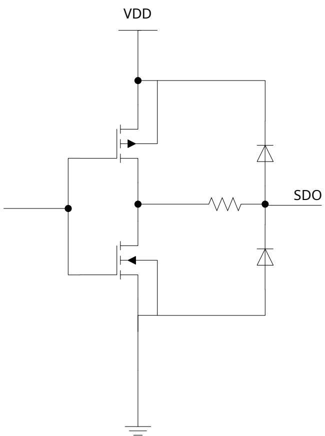
LE Input



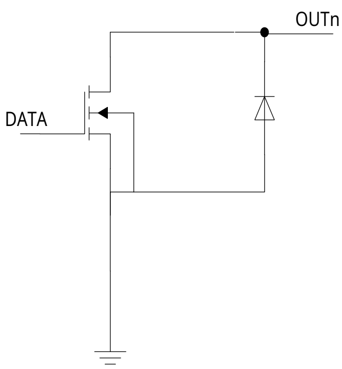
- CLK,SDI Input



SDO Output



- OUT0~OUT15 Output



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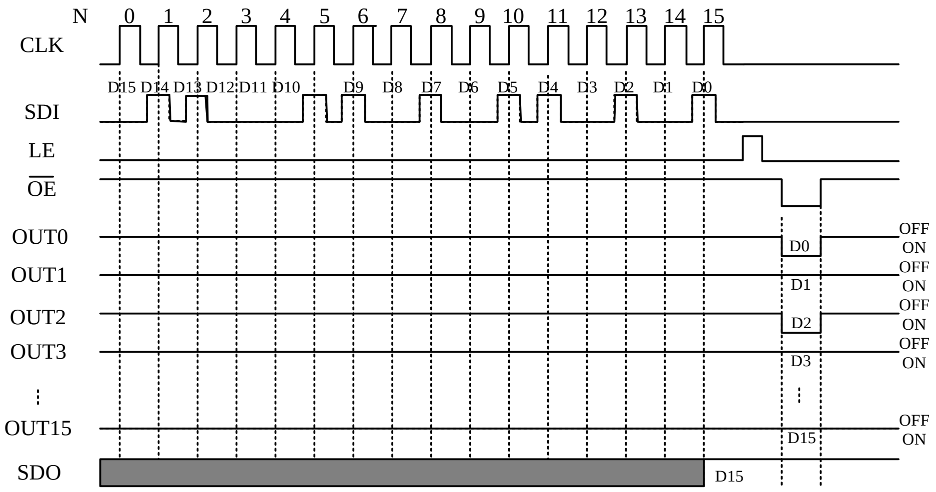
Note: please refer to the website for the latest version of this datasheet.

Timing Diagram



: **Not Defined**

Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$... $\overline{OUT7}$... $\overline{OUT15}$	SDO
↑	H	L	Dn	$\overline{Dn}$...$\overline{Dn-7}$...$\overline{Dn-15}$	Dn-15
↑	L	L	Dn+1	No Change	Dn-14
↑	H	L	Dn+2	$\overline{Dn+2}$...$\overline{Dn-5}$...$\overline{Dn-13}$	Dn-13
↓	X	L	Dn+3	Dn+2...Dn-5...Dn-13	Dn-13
↓	X	H	Dn+3	off	Dn-13

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	VDD	0～7.0	V
Input Voltage	V_{SDA},V_{CLK},V_{LE},V_{OE}	-0.4～VDD+0.4	V
OUT port current	I_{OUT}	45	mA
OUT port voltage	V_{DS}	-0.5～+16.0	V
Clock frequency	f_{CLK}	30	MHz
Operating ambient temperature	T_{opr}	-40～+85	℃
Storage ambient temperature	T_{stg}	-55～+150	℃
HBM (Human Body Model)	V_{ESD}	>4	KV

Remarks: The peak reflow temperature for surface mount products must not exceed 260°C. Select a reflow temperature curve appropriate for your process according to the J-STD-020 standard and the recommendations of your solder paste manufacturer.

DC Characteristics

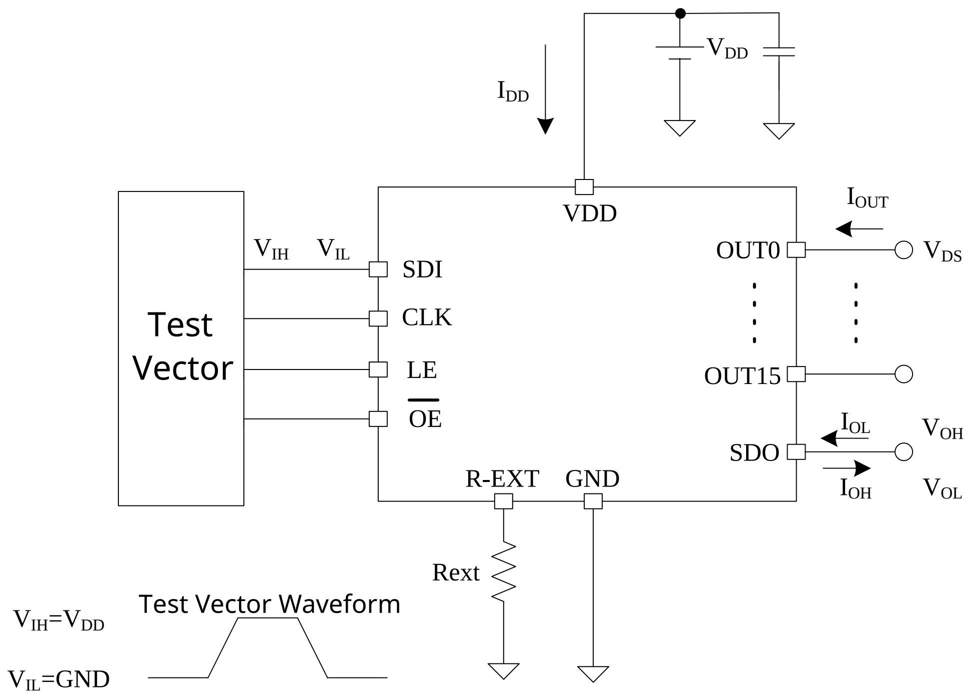
(VDD= 5.0V, Ta = 25℃)

Parameter	Symbol	Measurement conditions		Min	Typ	Max	Unit
Quiescent Current	$I_{DD}(off)1$	Rext floating, OUT0~OUT15 = OFF		-	1.5	-	mA
	$I_{DD}(off)2$	Rext = 1800 Ω, OUT0~OUT15 = OFF		-	2.6	-	mA
	$I_{DD}(off)3$	Rext = 920 Ω, OUT0~OUT15 = OFF		-	3.8	-	mA
SDO Drive Current	I_{OH}	VDD = 5.0V		-	-21	-	mA
	I_{OL}			-	21	-	mA
SDO Output Voltage	V_{OL}	I_{OL} = +1mA		-	-	0.4	V
	V_{OH}	I_{OH} = -1mA		4.6	-	-	V
Input Voltage	V_{IH}	VDD=5.0V		0.7*VDD	-	VDD	V
	V_{IL}			GND	-	0.3*VDD	V
OUT Leakage Current	I_{LEAK}	V_{DS} =15V， OUT0~OUT15 = OFF		-	-	0.5	uA
OUT Output Current	I_{OUT}	VDD = 5.0V		1	-	32	mA
OUT Output Current 1	I_{OUT1}	V_{DS} =1.0V	rext = 1800Ω	-	9.2	-	mA
Output Current Error	D_{IOUT}	V_{DS} = 1.0V rext = 1800Ω	Intra-chip	-	±2.5%	-	
			Inter-chip	-	±3.5%	-	
OUT Output Current 2	I_{OUT2}	V_{DS} = 1.0V	rext = 920Ω	-	17.9	-	mA
Output Current Error	D_{IOUT}	VDS = 1.0V rext = 920Ω	Intra-chip	-	±2.5%	-	
			Inter-chip	-	±3.5%	-	
Output Current Error / V_{DS} Variation	%/ΔV_{DS}	V_{DS} =1.0V～3.0V， I_{OUT} =17.9mA		-	1	-	%/V
Output Current Error / V_{DD} Variation	%/ΔV_{DD}	V_{DD} =4.5V～5.5V， I_{OUT} =17.9mA		-	1	-	%/V
Pull-up Resistance	$R_{OE}(up)$	$\overline{OE}$		-	250	-	KΩ
Pull-down Resistance	$R_{LE}(down)$	LE		-	250	-	KΩ

(VDD=3.3V, Ta = 25°C)

Parameter	Symbol	Measurement conditions		Min	Typ	Max	Unit
Quiescent Current	$I_{DD}(off)1$	Rext floating, OUT0~OUT15 = OFF		-	1.2	-	mA
	$I_{DD}(off)2$	Rext = 1800 Ω, OUT0~OUT15 = OFF		-	3.6	-	mA
	$I_{DD}(off)3$	Rext = 920 Ω, OUT0~OUT15 = OFF		-	2.5	-	mA
SDO Drive Current	V_{OL}	I_{OL} = +1mA		-	-	0.3	V
	V_{OH}	I_{OH} = -1mA		3.0	-	-	V
SDO Output Voltage	I_{OH}	VDD = 3.3V		-	-10.5	-	mA
	I_{OL}			-	13.3	-	mA
Input Voltage	V_{IH}	VDD=3.3V		0.7*VDD	-	VDD	V
	V_{IL}			GND	-	0.3*VDD	V
OUT Leakage Current	I_{LEAK}	V_{DS} =15V， OUT0~OUT15 = OFF		-	-	0.5	uA
OUT Output Current	I_{OUT}	VDD =3.3V		1	-	22	mA
OUT Output Current 1	I_{OUT1}	V_{DS} =1.0V	rext = 1800Ω	-	9.2	-	mA
Output Current Error	D_{IOUT}	V_{DS} = 1.0V rext = 1800Ω	Intra-chip	-	±2.5%	-	
			Inter-chip	-	±3.5%	-	
OUT Output Current 2	I_{OUT2}	V_{DS} = 1.0V	rext = 920Ω	-	17.9	-	mA
Output Current Error	D_{IOUT}	V_{DS} = 1.0V rext = 920Ω	Intra-chip	-	±2.5%	-	
			Inter-chip	-	±3.5%	-	
Output Current Error / V_{DS} Variation	%/ΔV_{DS}	V_{DS} =1.0V～3.0V， I_{OUT} = 17.9mA		-	1	-	%/V
Output Current Error / V_{DD} Variation	%/ΔV_{DD}	V_{DD} =3.3V～3.8V， I_{OUT} = 17.9mA		-	1	-	%/V
Pull-up Resistance	$R_{OE}(up)$	$\overline{OE}$		-	250	-	KΩ
Pull-down Resistance	$R_{LE}(down)$	LE		-	250	-	KΩ

DC Characteristics Test Circuit



AC Characteristics

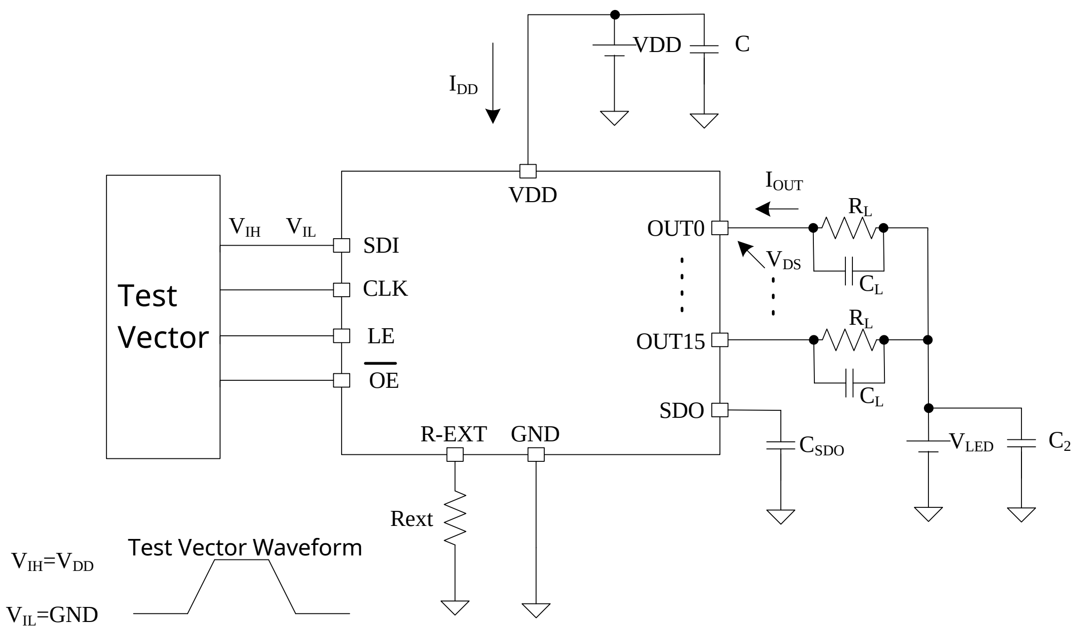
(VDD= 5.0V, Ta = 25℃)

Parameter		Symbol	Measurement Conditions	Min	Typ	Max	Unit
Propagation Time (low to high)	CLK——OUT	t_{pLH1}	V_{IH}=VDD V_{IL}=GND Rext=1800Ω VDD=5.0V R_L=400Ω C_L=10pF	--	30	--	ns
	LE——OUT	t_{pLH2}		--	26	--	ns
	OE——OUT	t_{pLH3}		--	30	--	ns
	CLK——SDO	t_{pLH}		--	28	--	ns
Propagation Time (high to low)	CLK——OUT	t_{pHL1}		--	35	--	ns
	LE——OUT	t_{pHL2}		--	33	--	ns
	OE——OUT	t_{pHL3}		--	35	--	ns
	CLK——SDO	t_{pHL}		--	27	--	ns
Current output rise time		$t_{OUT-RISE}$		--	30	--	ns
Current output fall time		$t_{OUT-FALL}$		--	35	--	ns

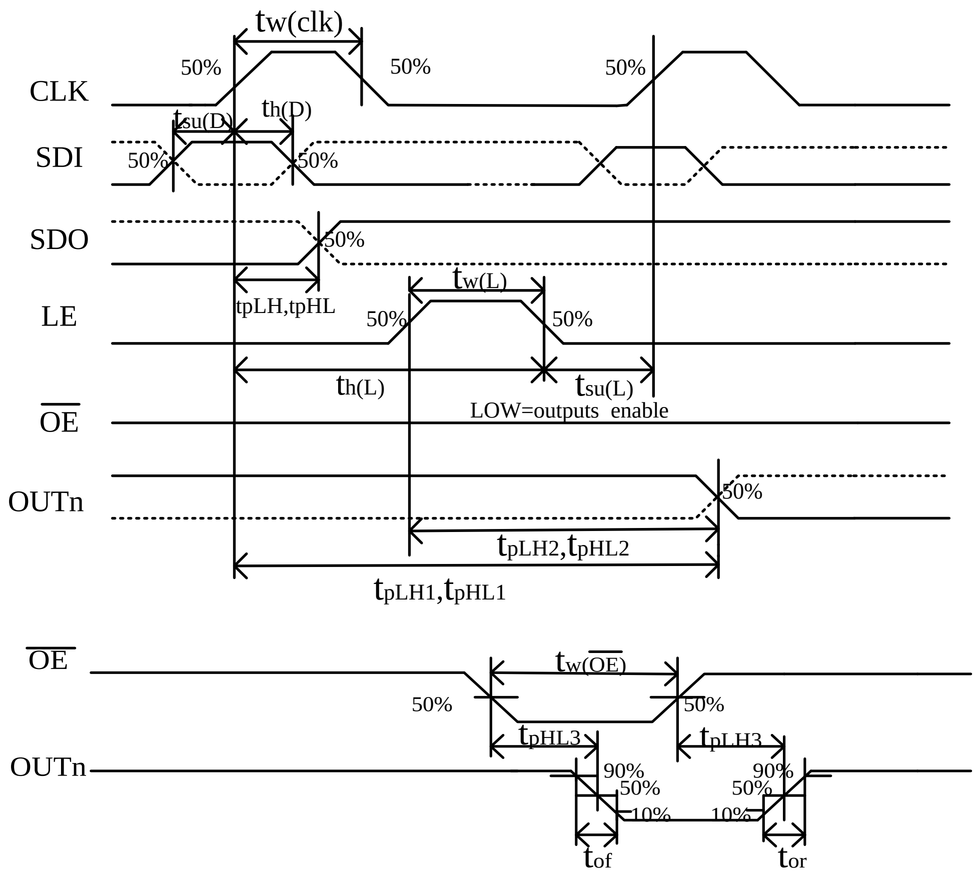
(VDD= 3.3V, Ta = 25℃)

Parameter		Symbol	Measurement Conditions	Min	Typ	Max	Unit
Propagation Time (low to high)	CLK——OUT	t_{pLH1}	V_{IH}=VDD V_{IL}=GND Rext=1800Ω VDD=3.3V R_L=200Ω C_L=10pF	--	42	--	ns
	LE——OUT	t_{pLH2}		--	36	--	ns
	OE——OUT	t_{pLH3}		--	45	--	ns
	CLK——SDO	t_{pLH}		--	30	--	ns
Propagation Time (high to low)	CLK——OUT	t_{pHL1}		--	38	--	ns
	LE——OUT	t_{pHL2}		--	33	--	ns
	OE——OUT	t_{pHL3}		--	40	--	ns
	CLK——SDO	t_{pHL}		--	29	--	ns
Current output rise time		$t_{OUT-RISE}$		--	26	--	ns
Current output fall time		$t_{OUT-FALL}$		--	18	--	ns

AC Characteristics Test Circuit



Timing Diagram



Applications

The output current variation between channels and chips is very small due to the excellent constant current output characteristics of the SM16206:

- The maximum current error between channels on one chip is less than ± 2.5%, and the maximum current error between chips is less than ± 3.5%.
- When the load terminal voltage (V_{DS}) changes, the stability of the output current is not affected, as shown in the figure below.

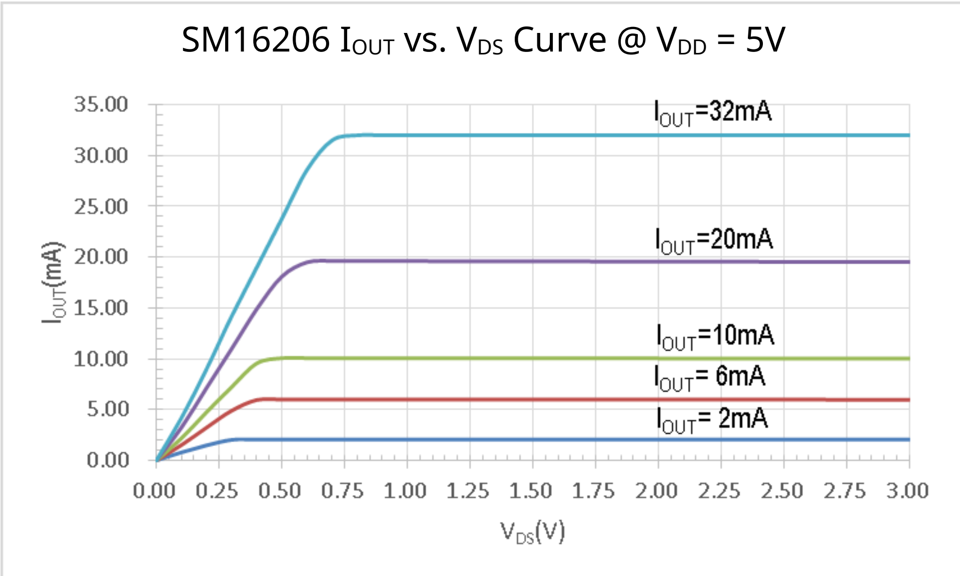


Fig. SM16206 I_{OUT} Constant Current Characteristic Curve

Output Current Adjustment

As shown in the figure below, the output current I_{OUT} is adjusted by an external resistor R_{EXT}, and the output current value can be calculated by applying the following formula:

$I_{OUT}=16500/R_{EXT}$ mA

The R_{EXT} in the formula refers to the resistance from the R-EXT pin to ground and the current is in mA. For example, when R_{EXT} = 750Ω the output current is 22 mA, and when R_{EXT} = 6000Ω, the output current is 2.8 mA.

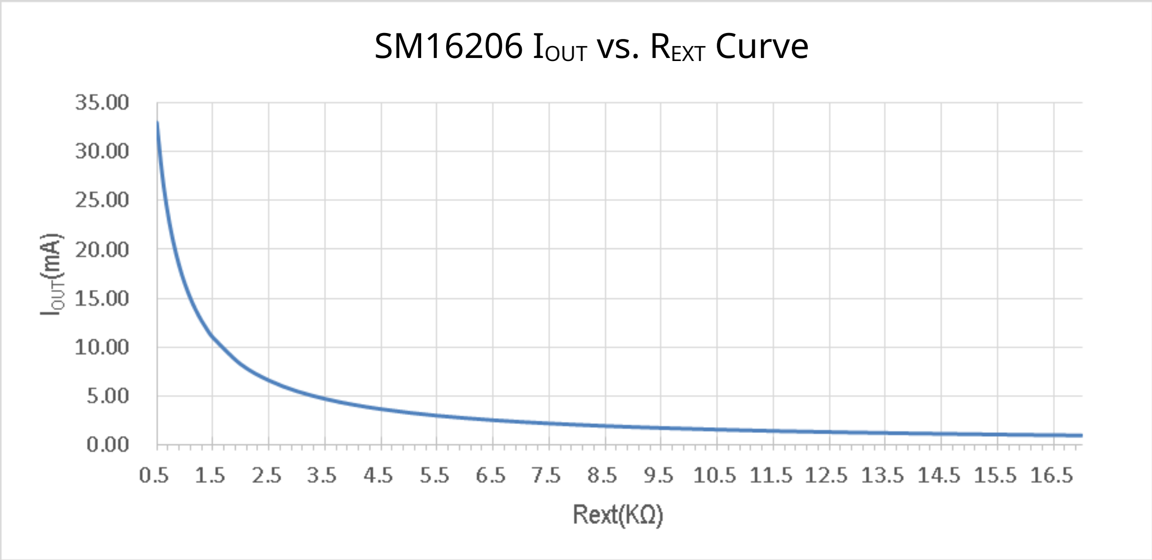


Fig. SM16206 I_{OUT} vs R_{EXT} Resistance Curve

Package Power Dissipation (PD)

The maximum power dissipation of the package is given by the formula:

$$P_{D(max)} = \frac{(T_j - T_a)}{R_{th(j\text{-}a)}}$$

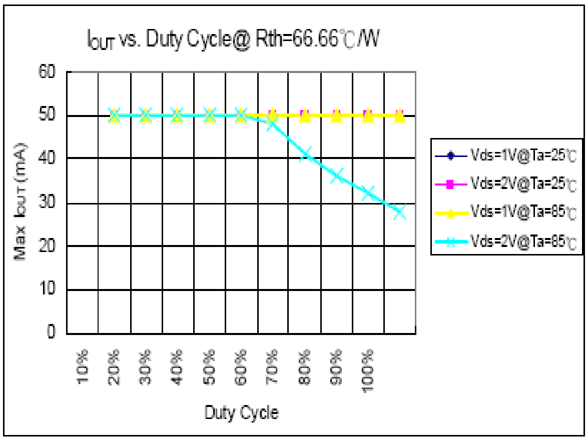
When 16 channels are fully turned on, the actual power dissipation is:

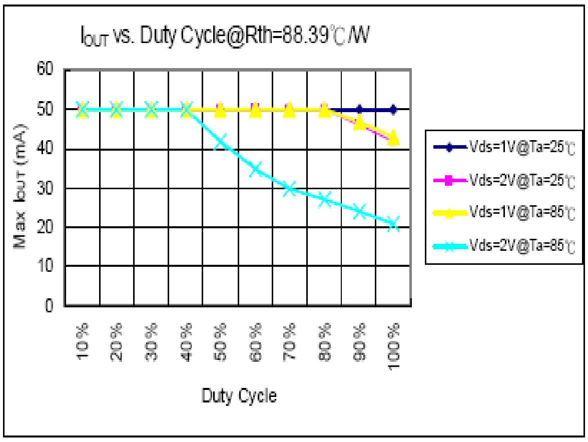
$$P_{D(act)} = IDD*VDD + I_{OUT}*Duty*V_{DS}*16$$

The actual power dissipation must be less than the maximum power dissipation, that is, $P_{D(act)} < P_{D(max)}$. The relationship between the maximum output current and the duty cycle is:

$$I_{out} = \frac{\dfrac{T_j - T_a}{R_{th(j-a)}} - IDD * VDD}{V_{DS} * Duty * 16}$$

Where T_j is the operating (junction) temperature of the IC, T_a is the ambient temperature, V_{DS} is the average output port voltage, Duty is the duty cycle, and $R_{th(j\text{-}a)}$ is the thermal resistance of the package. The figures below shoud the relationship between the maximum output current and the duty cycle.





If you need a larger I_{OUT}, you can add a heatsink with thermal resistance R_{fc} given by the formula:

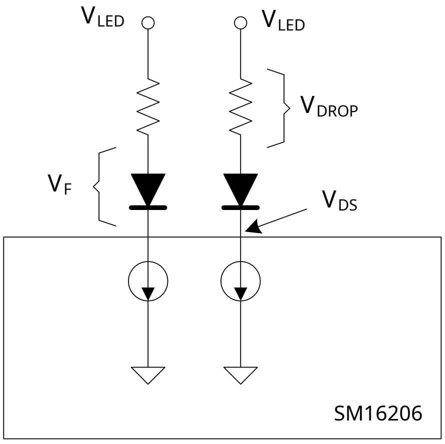
Given $\frac{1}{R_{th(j\text{-}a)}} + \frac{1}{R_{fc}} = \frac{P_{D(act)}}{T_j - T_a}$ then:

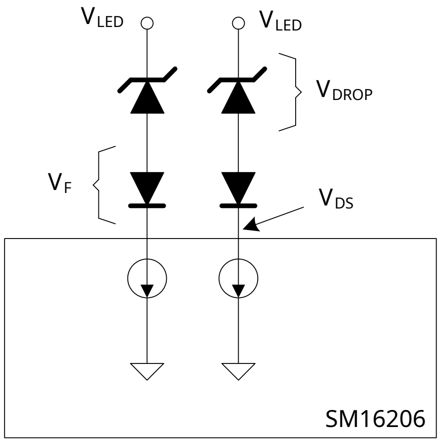
$$R_{fc} = \frac{R_{th(j\text{-}a)} * T_j - T_a}{P_{D(act)} * R_{th(j\text{-}a)} - T_j + T_a}$$

Where $P_{D(act)} = IDD*VDD + I_{OUT}*Duty*V_{DS}*16$

Load Terminal Voltage (V_{LED})

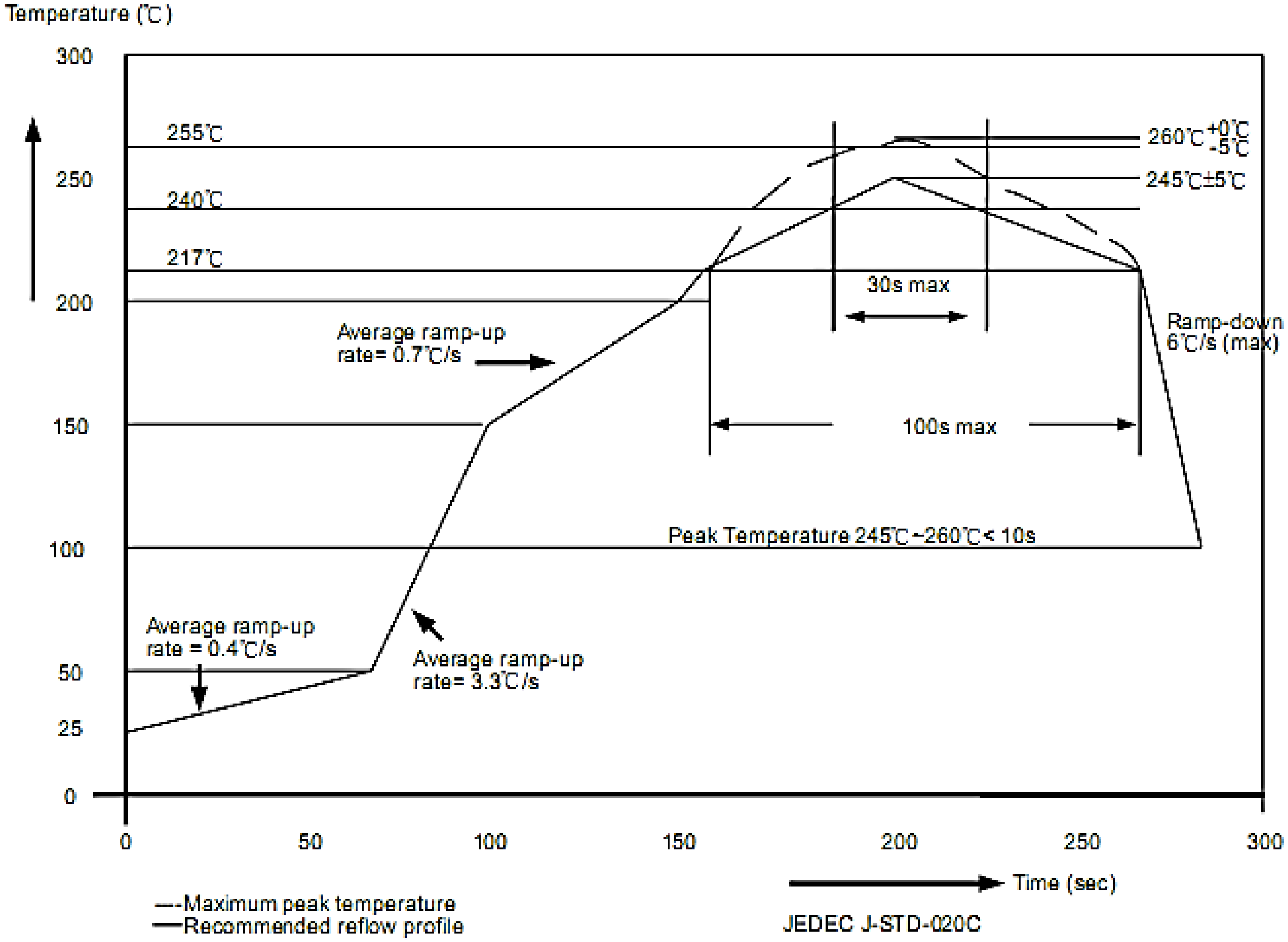
In order to minimize the power dissipated in the package, it is recommended to keep the output terminal voltage V_{DS} at about 1.0V (based on I_{OUT} = 1mA ~ 32mA). If $V_{DS} = V_{LED} - V_F$ and V_{LED} = 5.0V, the high output voltage V_{DS} may cause $P_{D\,(act)} > P_{D\,(max)}$. In this situation, it is recommended to use a lower V_{LED} supply voltage where possible. You can also use an external resistor or Zener diode with a voltage drop V_{DROP} to reduce V_{DS} according to $V_{DS} = (V_{LED} - V_F) - V_{DROP}$.





Package Soldering Process

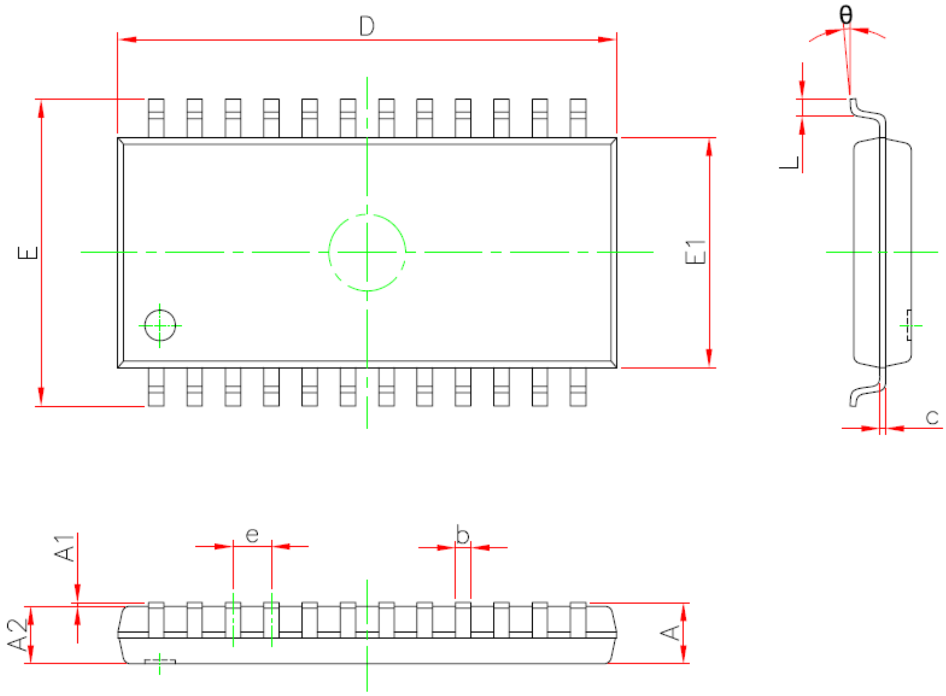
These semiconductors comply with the European RoHS standard, and the reflow temperature in the packaging and soldering process must comply with the J-STD-020 standard.



Package Thickness	Volume mm³< 350	Volume mm³：350~2000	Volume mm³≥ 2000
<1.6mm	260+0°C	260+0°C	260+0°C
1.6mm~2.5mm	260+0°C	250+0°C	245+0°C
≥2.5mm	250+0°C	245+0°C	245+0°C

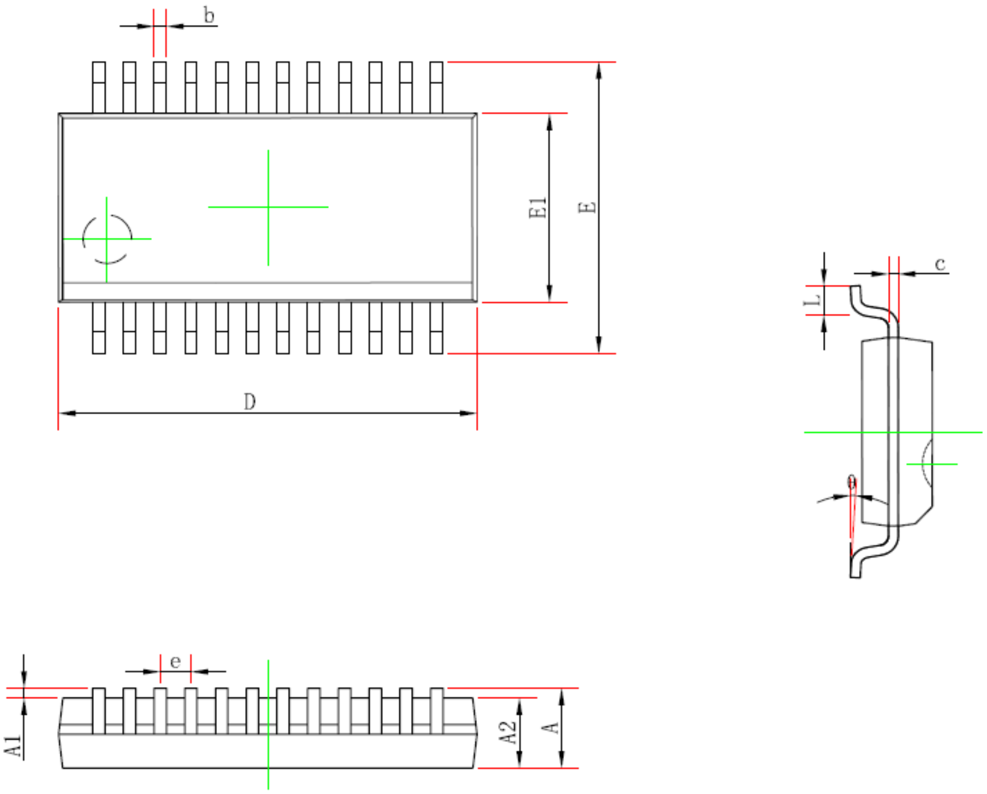
Packages

SSOP24



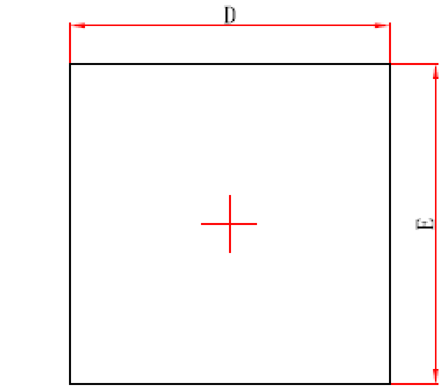
Symbol	Min(mm)	Max(mm)
A	-	2.15
A1	0.05	0.35
A2	1.2	1.9
b	0.15	0.75
c	0.05	0.45
D	12.6	13.5
E	7.6	8.5
E1	5.6	6.5
e	1.0TYP	
L	0.2	1.0
θ	0°	10°

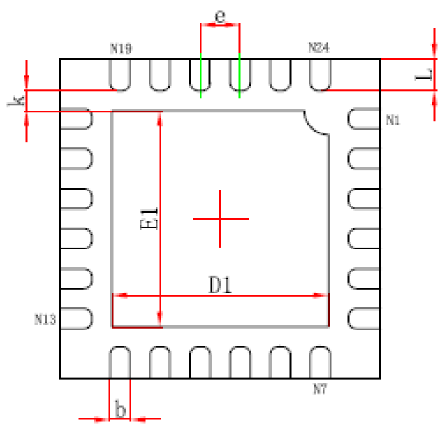
QSOP24



Symbol	Min(mm)	Max(mm)
A	-	1.95
A1	0.05	0.35
A2	1.05	-
b	0.1	0.4
c	0.05	0.254
D	8.2	9.2
E1	3.6	4.2
E	5.6	6.5
e	0.635TYP	
L	0.3	1.5
θ	0°	10°

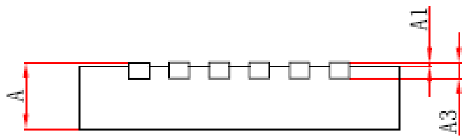
QFN24(4*4)





Top View

Bottom View



Side View

Symbol	Min(mm)	Max(mm)
A	0.6	1.0
A1	-	0.1
A3	0.203REF	
D	3.8	4.3
E	3.8	4.3
D1	2.4	3.0
E1	2.4	3.0
K	0.2min	
e	0.5TYP	
b	0.1	0.4
L	0.2	0.7

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