The flip-flop operates like a latch and transfers data from Port P23 during each ALE cycle.

c. Once the previous conditions are met (the RAM is addressed) and line CE2 is high, data from the RAM is transferred to the Data Lines.

7-F-63. Sending Data to the RAM. The RAM can receive new Data when its R/W line (Read/Write at U512 pin 20) is low. This can only happen if the 3478A's Cal Enable Switch (located on the front panel) is on and the $\overline{WR}$ line of the CPU (Write at U501 pin 10) is low. The following explains the operation.

a. The Cal Enable Switch brings one input of NOR gate U508C low.

b. The other input of the gate is a low from the $\overline{WR}$ line.

c. The output of U508C goes high, and since NOR gate U508D is configured as an inverter, the output of U508D goes low. The RAM is now ready to receive new data.

7-F-64. Since the 3478A's Calibration Constants are stored in the CMOS RAM, the constants must remain in the RAM when the 3478A is turned off (or power removed). This is done by battery BT701 in the +5V Power Supply Circuit. In addition, the RAM should not see any possible write commands (R/W low) during the time that power is removed. The RAM must be disabled. This is because a write command may erase some calibration constants. The RAM is disabled by comparator U550C (part of the CPU's power-on circuit in the +5V power supply). The operation is as follows (refer to Schematic 4 for the explanation):

a. As long as the 3478A is on, the RAM gets its supply voltage from CR500.

b. When power is off, the RAM gets its supply voltage from battery BT701 through diode CR764. The battery voltage is used for data retention.

c. After turning power off, the RAM is disabled by setting line CE2 low. This is done by comparator U550C (see Schematic 4). The comparator senses a low (or no +5V) from voltage divider R761, R762, and R763. Since U550C's inverting input is at the battery voltage, the output of U550C becomes low. This discharges capacitor C763 before the power supply goes off. This makes line CE2 low and disables the RAM.

7-F-65. Keyboard Operation. The Keyboard's pushbuttons are connected in a 4x4 matrix and are continuously scanned by the CPU. The operation is as follows:

a. One side of the matrix is connected to Ports P10 to P13 of the CPU (U501 pins 27 to 30) and the other side is connected to Ports P14 to P17 (U501 pins 31 to 34).

b. Before scanning starts, Ports P14 to P17 are low. When scanning begins, starting with Port P14, each port goes sequentially high.

c. During the time that the keyboard is scanned, the CPU determines which one and if any of Ports P10 to P13 are high. A high on P10 to P13 is used to determine the button pressed. For example, the SRQ button is pressed and turns the corresponding SRQ switch on. This connects Port P11 to P17 and makes P11 high when P17 is high. Since the CPU knows when it sets P17 high and also knows when P11 is high, the pressed button is determined.

7-F-66. Display Operation. The 3478A Display is an alphanumeric display with 12 annunciators. The CPU sends serial data to the Display Circuitry which in turn does all the necessary decoding of the data (to display readings, etc.). The operation is as follows:

a. With line PWO high, the CPU can send new data to the Display Circuitry. Data is in serial form and is sent on the Data line (U506 pin 4). For the Display Circuitry to receive and decode the data, the other display lines have to send certain information to the circuitry. This is as follows:

1. The Display Circuitry requires two clock inputs to receive data, I1 and I2. The inputs come from flip-flop U506 (pin3) and Port P25 for clock inputs I1 and I2, respectively. (Flip-flop U506 is used as a latch between the CPU and the Display Circuitry.)

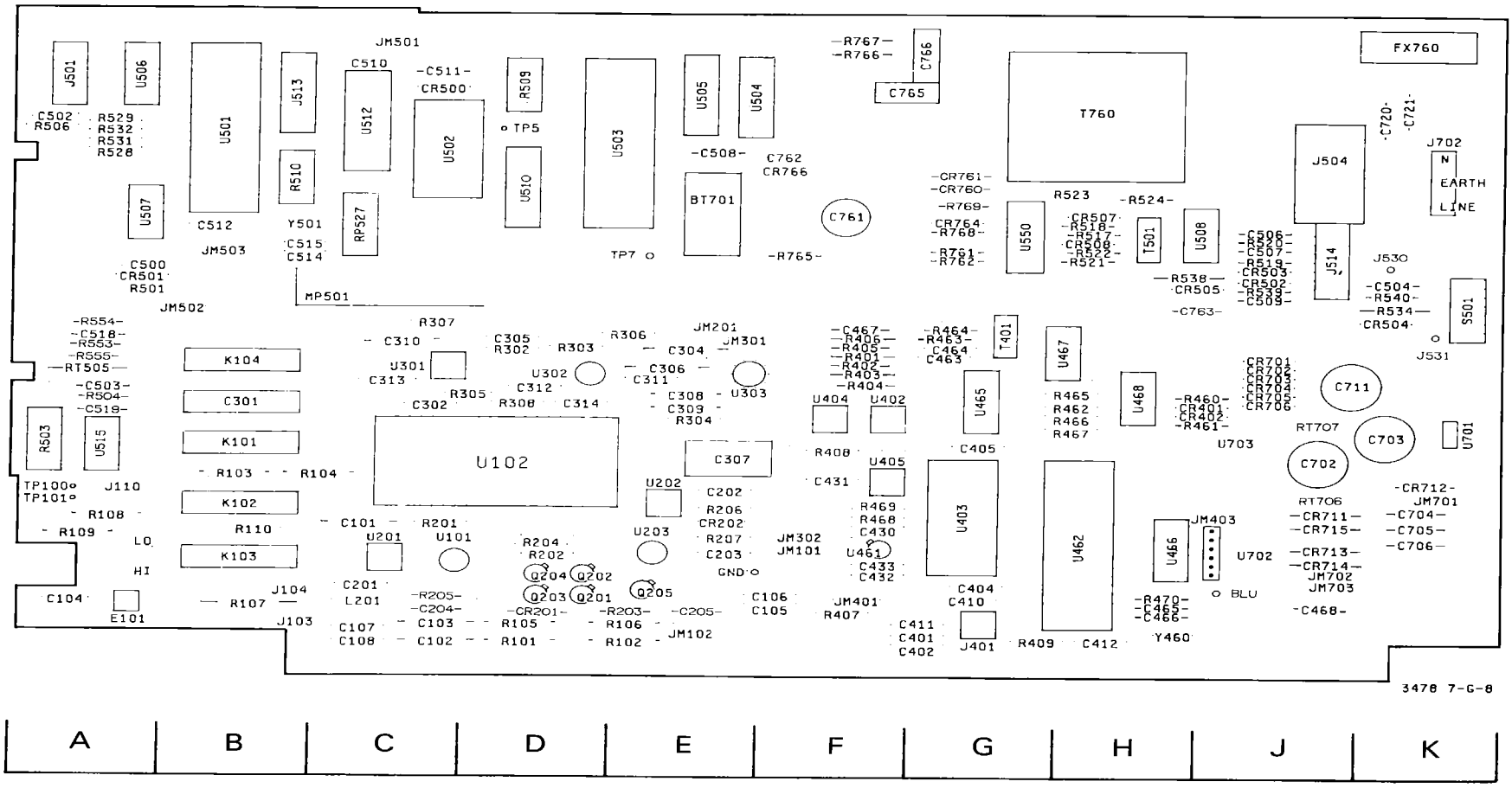
2. The ISA line (U506 pin 5) is used to give instructions to the Display Circuitry.

3. The SYNC line (U506 pin 6) is used to tell the Display Circuitry when to look for instructions.

b. With line PWO (from Port P23 of the CPU at U501 pin 36) low, the Display Circuitry operates without receiving any data from the CPU. The circuitry can operate in this mode since it has an internal clock (capacitor C502 is the frequency reference). With the circuitry in the internal mode, no updating of the display is done. Line PWO is controlled by the CPU.

7-F-67. HP-IB Operation. All interfacing between the CPU and the Hewlett-Packard Interface Bus (HP-IB) is done by the HP-IB Chip (U503) and two Bus Transceivers (U504 and U505). The HP-IB Chip is a microprocessor and changes the data sent and received by the CPU to the necessary HP-IB information (e.g. Listen, Talk, etc.). The Transceivers transfer and receive the HP-IB information between the HP-IB Chip and the Bus. The circuitry operates as follows:

a. The HP-IB Chip (U503) receives its clock signal from the CPU's T0 output (U501 pin 1).



Component Locator for A/D Converter and Control Logic
7-G-8

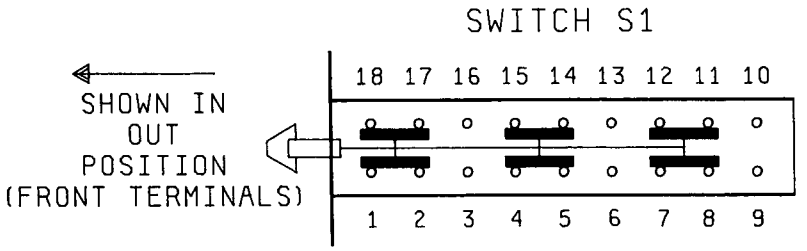
COMPONENT LOCATOR TABLE FOR SCHEMATIC 3 (LOGIC)

Component	Col.
C401	F,G
C402	F,G
C404	G
C405	G
C410	G
C411	F,G
C412	H
C430	F
C431	F
C432	F
C433	F
C463	G
C464	G
C465	H
C466	H
C467	F
C468	J
C501	A
C502	A
C503	A
C504	K
C506	J
C507	J
C508	E
C509	J
C510	C
C511	C
C512	B
C514	B,C
C515	B,C
C518	A
CR401	H
CR402	H
CR500	A

Component	Col.
CR501	A
CR502	J
CR503	J
CR504	J,K
CR505	H
CR507	H
CR508	H
J501	A
J504	J
JM401	F
JM403	H
JM501	C
JM502	A,B
JM503	B
R401	E
R402	F
R403	F
R404	F
R405	F
R406	F
R407	F
R408	F
R409	G
R460	H
R461	H
R462	G,H
R463	G
R464	G
R465	G,H
R466	G,H
R467	G,H
R468	F

Component	Col.
R469	F
R470	H
R501	A
R503	A
R504	A
R506	A
R509	D
R510	B
R517	H
R518	H
R519	J
R520	J
R521	H
R522	H
R523	H
R524	H
R528	A
R529	A
R531	A
R532	A
R534	K
R538	H
R539	J
R553	A
RT505	A
RP527	C
S501	K
T401	G
T501	H
TP2	B

Component	Col.
TP3	B
TP4	B
TP5	D
TP6	A
TP7	E
TP8	B
TP9	B
U401	G
U402	F
U403	G
U404	F
U405	F
U461	F
U462	G,H
U465	G
U466	H
U467	G,H
U468	H
U501	B
U502	C
U503	D,E
U504	E,F
U505	E
U506	A
U507	A
U510	D
U512	C
U513	B
U514	J
U515	A
U550	G
Y460	H
Y501	B



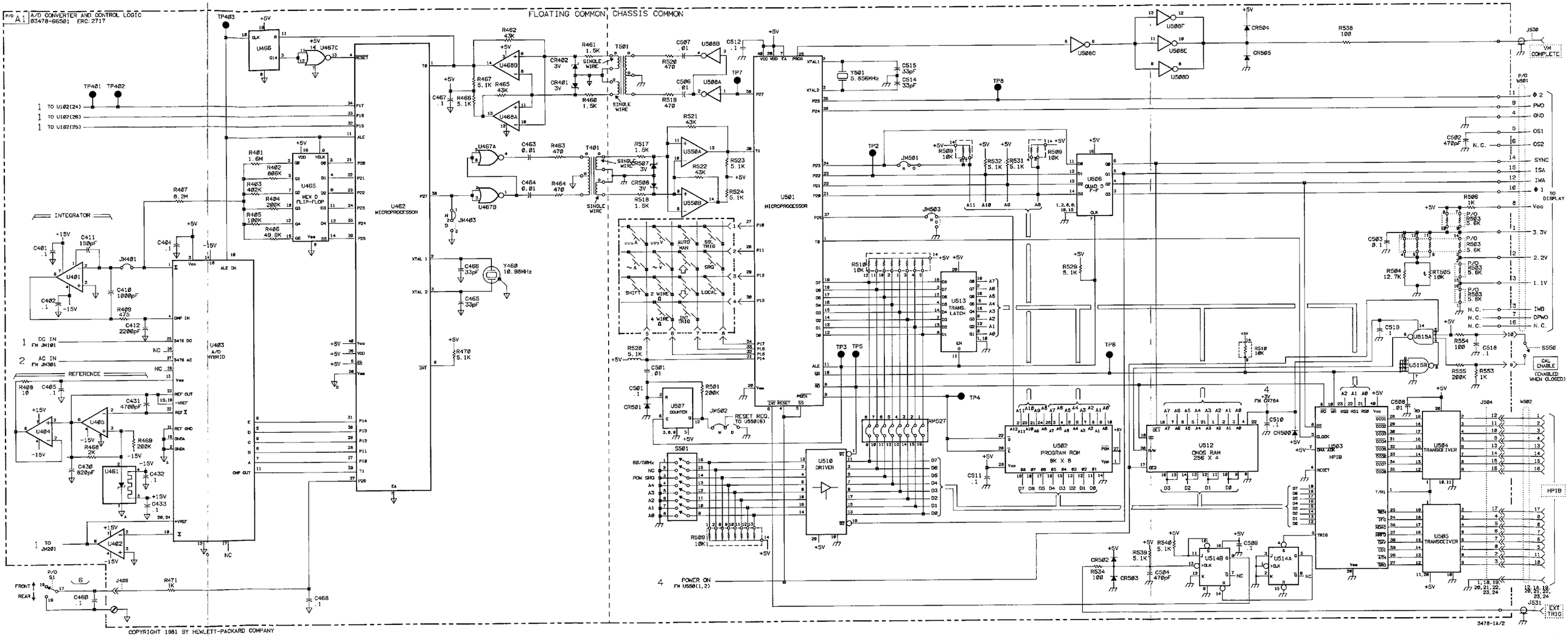


Figure 7-G-5. A/D Converter and Control Logic