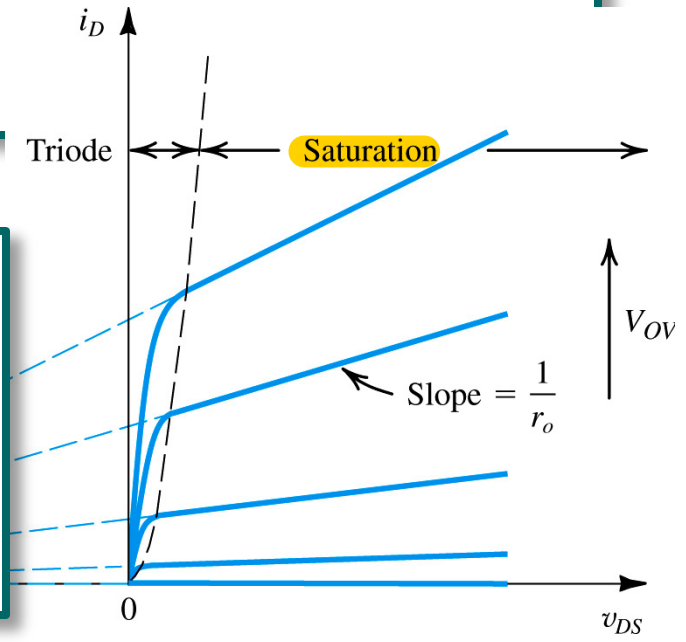
4. MOS Amplifier Biasing & Discrete MOS Amplifiers

Sedra & Smith Sec. 5.7 & 5.8

(S&S 5th Ed: Sec. 4.7 & 4.9)

The major goal of "Bias" is to ensure that MOS is in saturation at all times

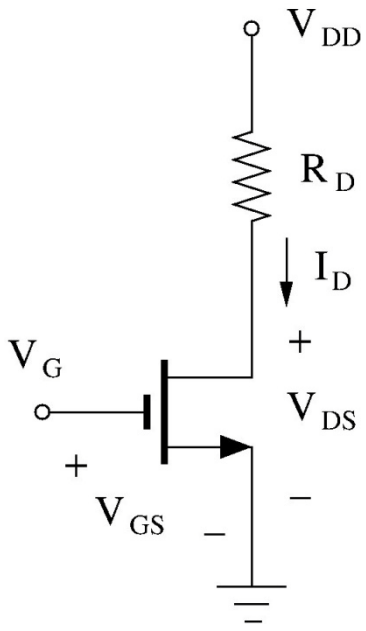
- **Bias is the state of the system when there is no signal.**
- Bias point should be stable (i.e., resilient to variations in $\mu_n C_{ox}$ (W/L), V_t , … due to temperature and/or manufacturing variability.)
  - Important parameters are I_D and V_{DS}



In addition:

- Bias point impacts the small-signal parameters.
- Bias point impacts how large a signal can be amplified.
- Bias point impact power consumption.

Bias with Gate Voltage



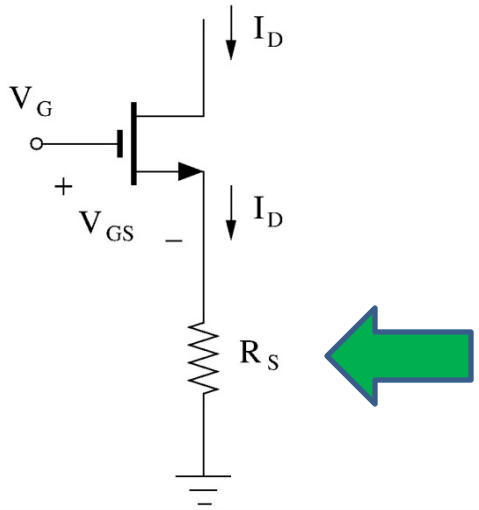
$$I_D = 0.5\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

$$V_{DS} = V_{DD} - I_D R_D$$

- This method is NOT desirable as $\mu_n C_{ox}\,(W/L)$ and V_t are not "well-defined." Bias point (i.e., I_D and V_{DS}) can change drastically due to temperature and/or manufacturing variability.
  - See Exercise 5.33 (S&S 5th Ed: Exercise 4.19) Changing V_t from 1 to 1.5 V leads to 75% change in I_D.

Bias with Source Degeneration (Resistor R_s provides negative feedback)

$$\begin{cases} V_{GS} = V_G - R_S I_D \\ I_D = 0.5\mu_n C_{ox} \dfrac{W}{L}(V_{GS} - V_t)^2 \end{cases}$$



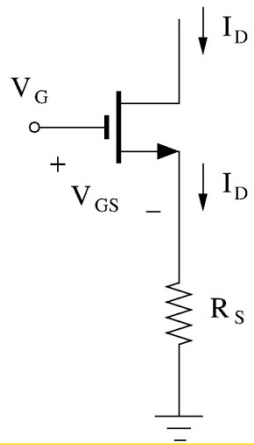
Negative Feedback:

- If $I_D \uparrow$ (because $\mu_n C_{ox} \uparrow$ or $V_{tn} \downarrow$) $\xrightarrow{\text{GS KVL}}$ $V_{GS} \downarrow$ $\xrightarrow{I_D \text{ Eq.}}$ $I_D \downarrow$
- If $I_D \downarrow$ (because $\mu_n C_{ox} \downarrow$ or $V_{tn} \uparrow$) $\xrightarrow{\text{GS KVL}}$ $V_{GS} \uparrow$ $\xrightarrow{I_D \text{ Eq.}}$ $I_D \uparrow$

➢ Feedback is most effective if $R_S I_D >> V_{GS}$

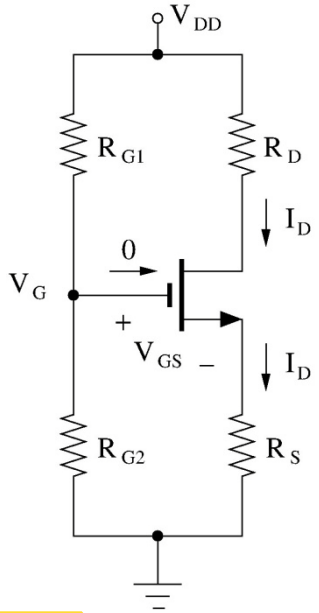
$$V_{GS} - V_G + R_S I_D = 0 \Rightarrow I_D \approx V_G / R_S$$

Examples of Bias with Source Degeneration



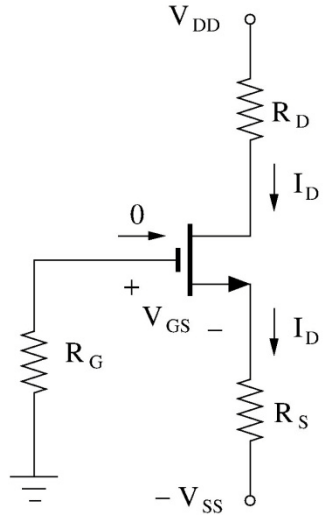
Basic Arrangement

$$V_{GS} = V_G - R_S I_D$$



Bias with <u>one</u> power supply

$$V_{GS} = V_G - R_S I_D$$

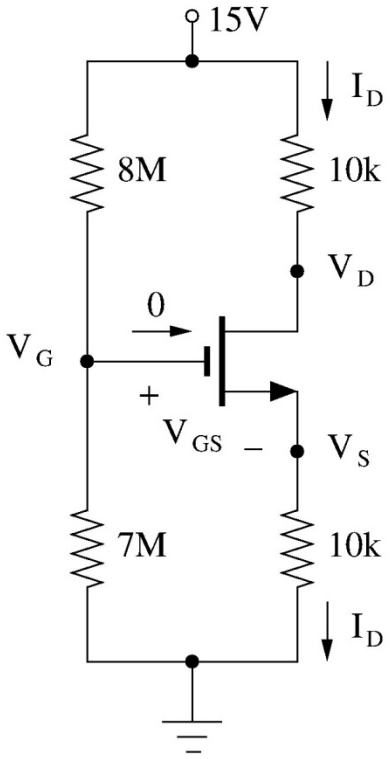


Bias with <u>two</u> power supply

$$V_{GS} = V_{SS} - R_S I_D$$

$$(\text{KVL}: \quad 0 = R_G \times 0 + V_{GS} + R_S I_D - V_{SS})$$

Example: Find Bias point for $V_t = 1$ V and $\mu_n C_{ox}\,(W/L) = 1.0$ mA/V^2
(Ignore channel-width modulation.



Impact of R_S (prove it)
if $V_t = 1.5$ V (50% change),
$I_D = 0.455$mA (9% change)

Voltage divider ($I_G = 0$)

$$V_G = (7)/(7+8)\times 15 = 7 \text{ V}$$

$$I_D = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

$$\text{GS-KVL}: V_G = V_{GS} + R_S I_D = 7$$

$$V_{OV} + V_t + R_S I_D = 7$$

$$V_{OV} + 1 + 10^4 \times (0.5\times 10^{-3} V_{OV}^2) = 7$$

$$5V_{OV}^2 + V_{OV} - 6 = 0 \;\rightarrow\; V_{OV} = 1 \text{ V}$$

$$V_{GS} = V_{OV} + 1 = 2 \text{ V}$$

$$V_S = V_G - V_{GS} = 7 - 2 = 5 \text{ V}$$

$$I_D = V_S / R_S = 0.5 \text{ mA}$$

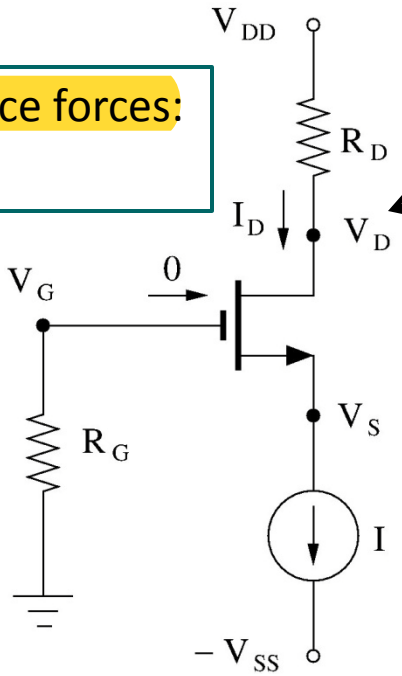
$$\text{DS-KVL}: 15 = R_D I_D + V_D$$

$$V_D = 15 - R_D I_D = 10 \text{ V}$$

$$V_{DS} = V_D - V_S = 5 \text{ V}$$

Biasing in ICs

- Resistors take too much space on the chip. So, source degeneration with R_S is NOT implemented in ICs.
- Recall that the goal of a good bias is to ensure I_D and V_{DS} would not change (e.g., due to temperature variation). One can force I_D to be constant using a current source.



1) Current source forces:
$$I_D = I$$

2) $V_D = V_{DD} - R_D I_D$

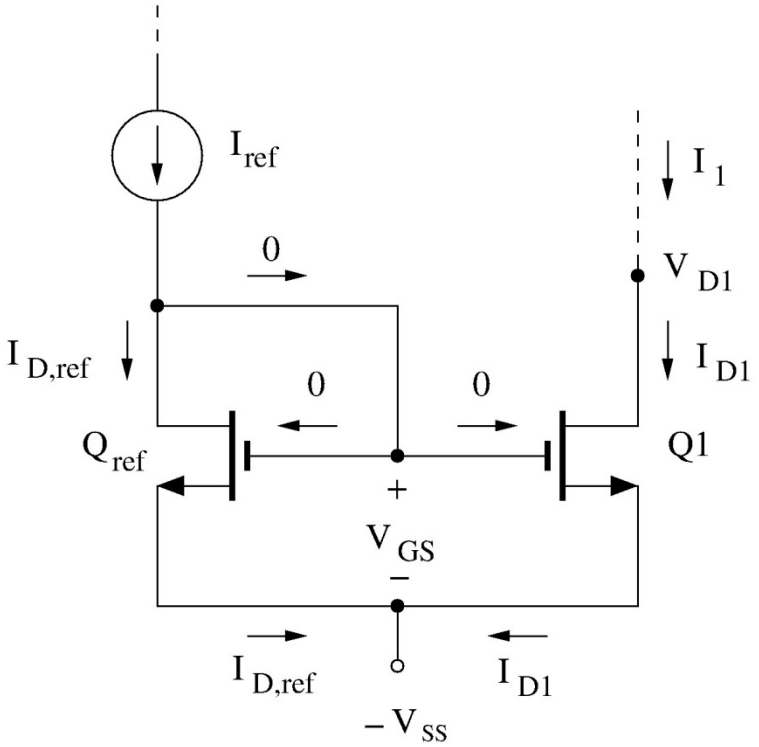
3) V_{GS} is set by
$$I_D = 0.5\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)^2$$

4) $V_S = V_G - V_{GS} = -V_{GS}$

5) $V_{DS} = V_D - V_S$

Current Mirrors or Current Steering Circuits are used as current sources for biasing ICs

Identical MOS:
Same μC_{ox} and V_t



- **Qref is always in saturation since**

$$V_{DS,ref} = V_{GS,ref} > V_{GS,ref} - V_t$$

- $V_{GS,ref} = V_{GS1} = V_{GS}$
- $V_{OV,ref} = V_{OV1} = V_{OV}$

$$I_{ref} = I_{D,ref} = 0.5\mu_n C_{ox}\left(\frac{W}{L}\right)_{ref} V_{OV}^2$$

$$I_1 = I_{D1} = 0.5\mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{OV}^2$$

$$\frac{I_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}}$$

- **Circuit works as long as Q1 is in saturation:** $V_{DS1} > V_{OV} = V_{GS} - V_t$

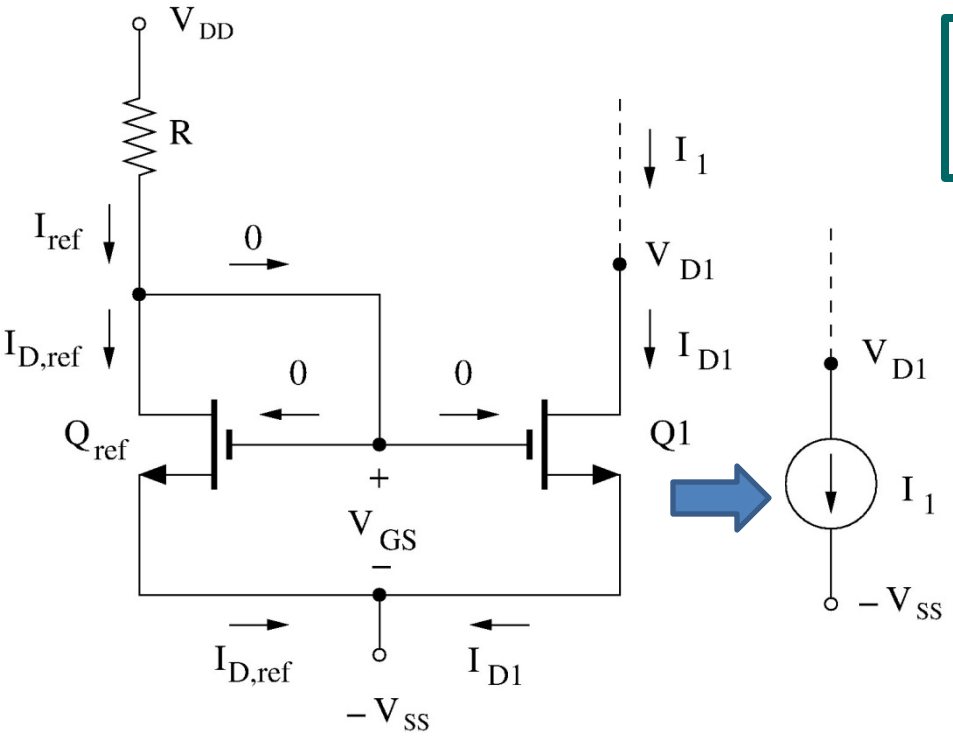
An implementation of a Current Mirror

Identical MOS:
Same μC_{ox} and V_t

$$\text{DS-KVL}: V_{DD} = RI_{ref} + V_{GS} - V_{SS}$$

$$RI_{ref} + V_{GS} = V_{DD} + V_{SS}$$

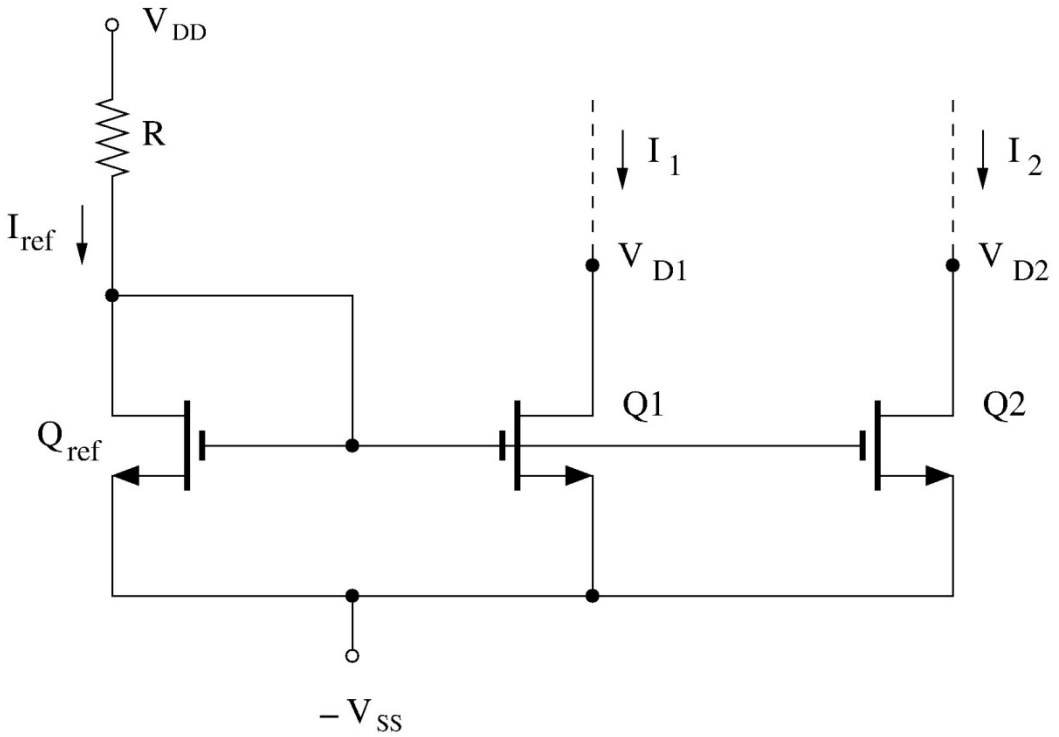
$$I_{ref} = I_{D,ref} = 0.5\mu_n C_{ox}(W/L)_{ref}\,(V_{GS} - V_t)^2$$



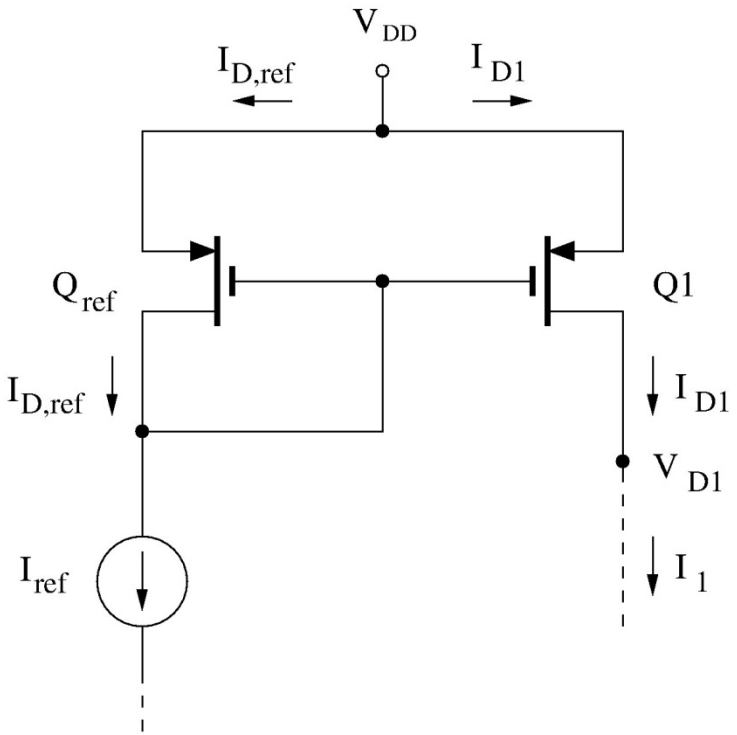
The above 2 equations uniquely set Qref Bias point ($I_{D,ref}$ and $V_{GS,ref} = V_{DS,ref}$)

- Current mirror: $\dfrac{I_1}{I_{ref}} = \dfrac{(W/L)_1}{(W/L)_{ref}}$
- **Since I_1 = constant regardless of voltage, this is a current source!**
- **Note:** Circuit works as long as Q1 is in saturation.

Examples of Current Steering circuits



Current steering circuit can bias several transistors

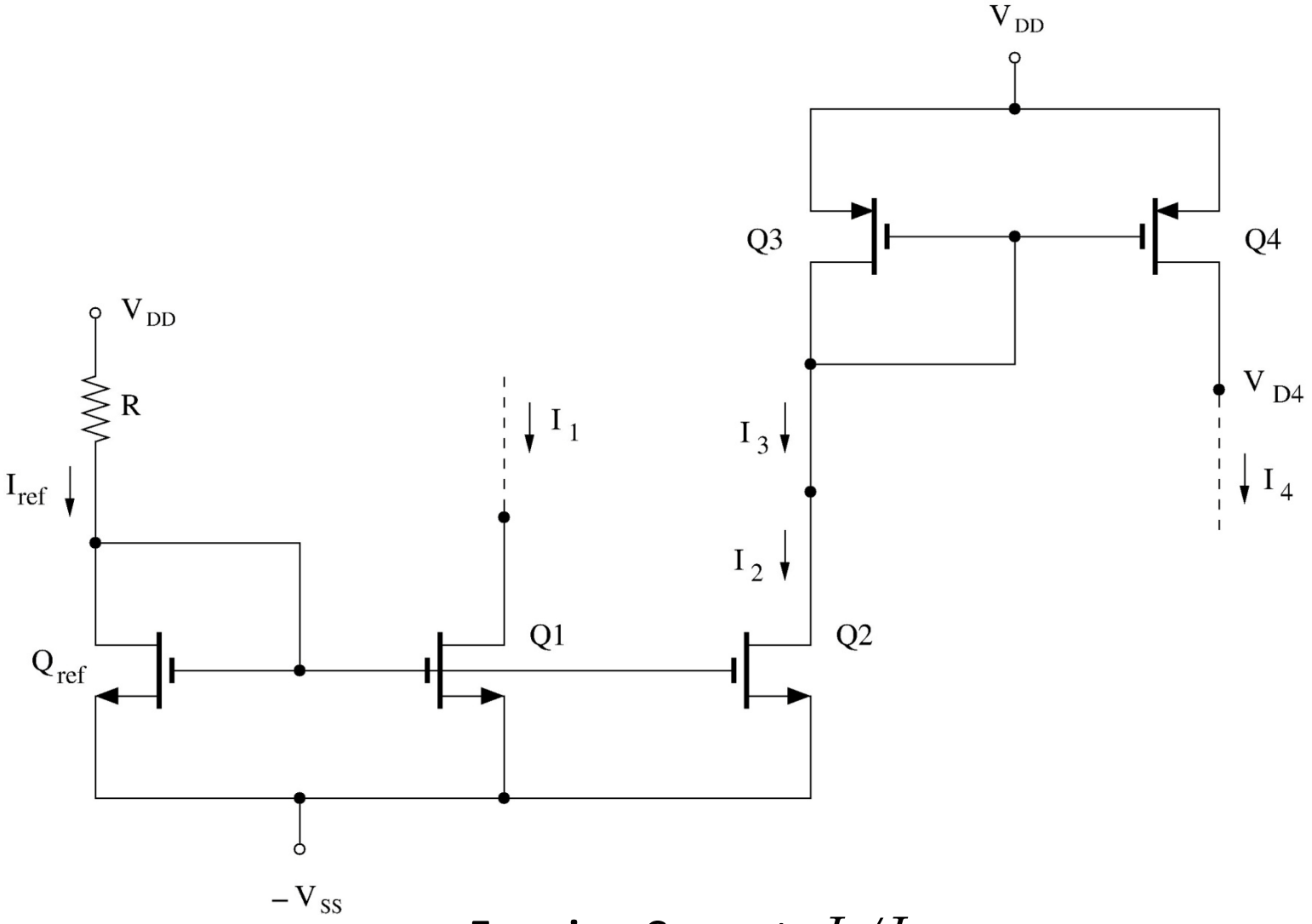


A PMOS current mirror

$$\frac{I_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}} \qquad \frac{I_2}{I_{ref}} = \frac{(W/L)_2}{(W/L)_{ref}}$$

$$\frac{I_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}}$$

An implementation of current steering circuit to bias several transistors in an IC



Exercise: Compute I_4 / I_{ref}

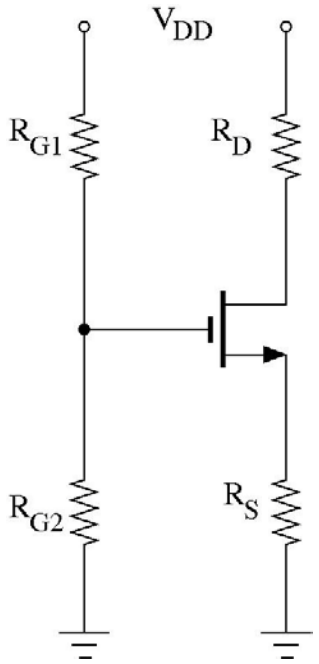
Discrete MOS Amplifiers

- We will use MOS Fundamental Amplifier Configurations and Elementary R Forms to find the response of discrete MOS amplifiers
- **First, a few observations.**

Stable Bias circuits for discrete MOS amplifiers

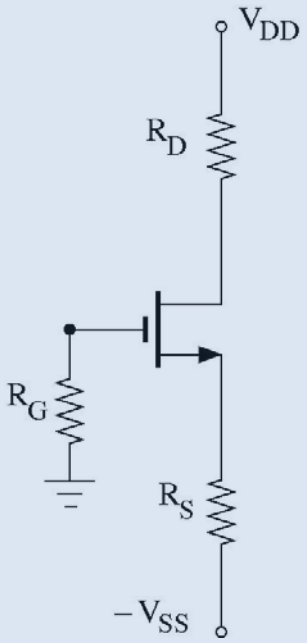
One power supply

$$V_{GS} = V_G - R_S I_D$$

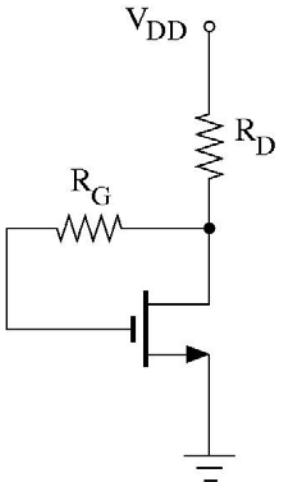


Two power supplies

$$V_{GS} = V_{SS} - R_S I_D$$



Drain Feedback



Will Discuss later

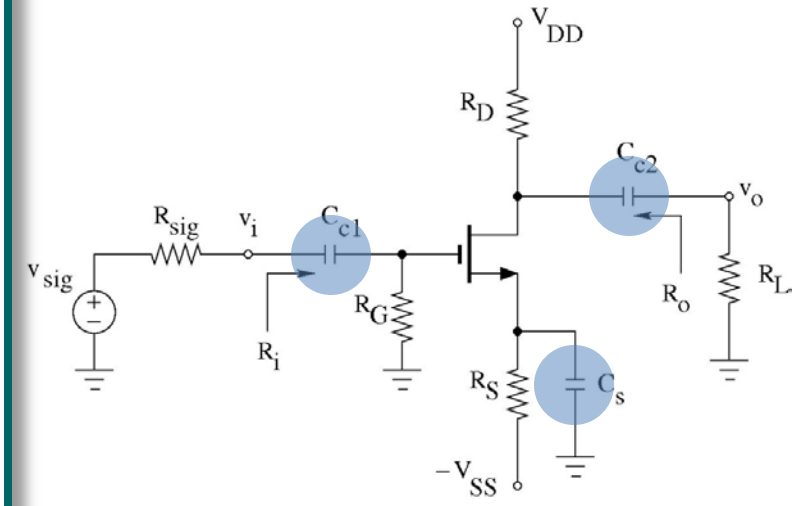
Identical signal circuit for

$$R_G = R_{G1} \parallel R_{G2}$$

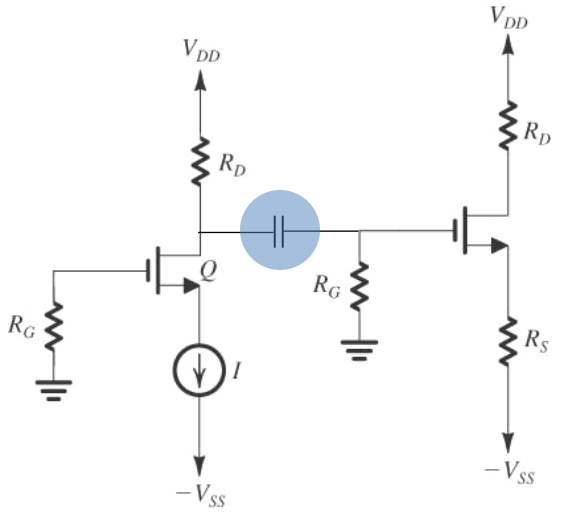
We will do analysis for this configuration

Signal is typically coupled to discrete amplifiers via coupling capacitors

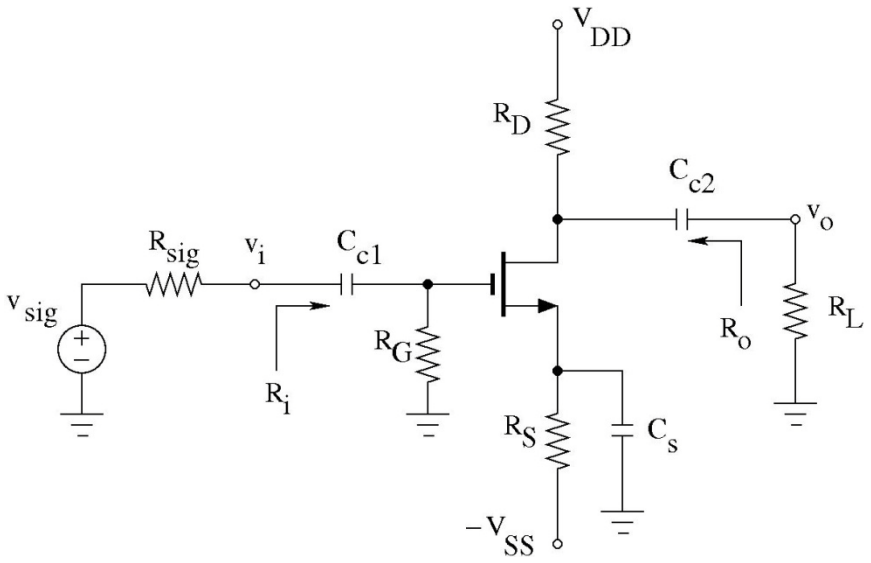
- Capacitors are open circuits for Bias (DC)
- We assume that the signal is at sufficiently high frequencies, such that "large" capacitors can be approximated as shorts ($|Z| = 1/\omega C$ is small)
  - A lower cut-off frequency for amplifier
- These capacitors can be added at input, output, and between amplifier stages.
- These capacitor can also be used to "by-pass" resistors needed for bias but not for signal.



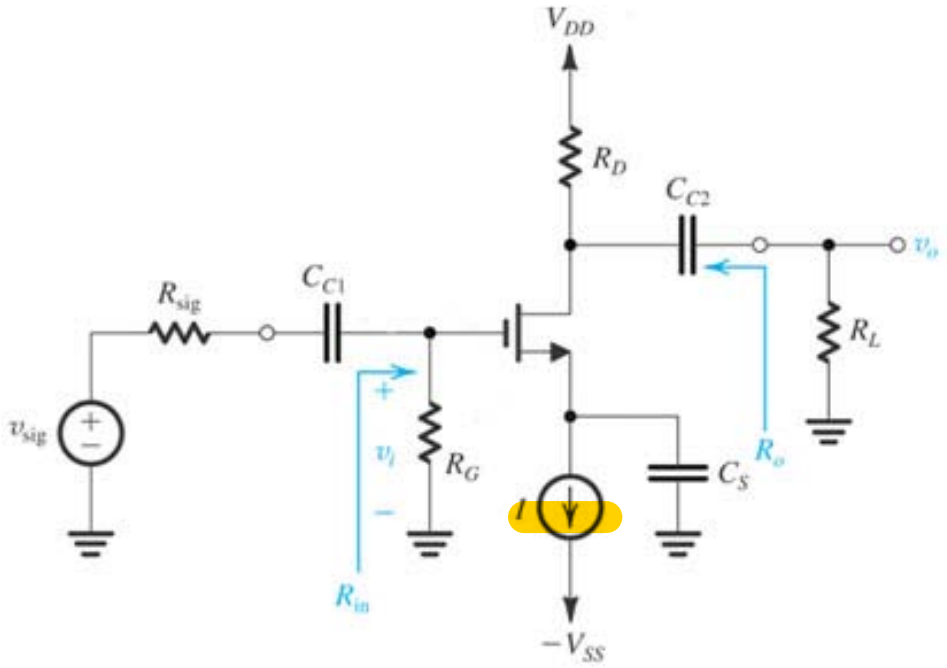
- Note: In general, one should NOT assume that all capacitors are short. We will see the impact of various capacitors later when we discuss frequency response of amplifiers.



Real Circuit



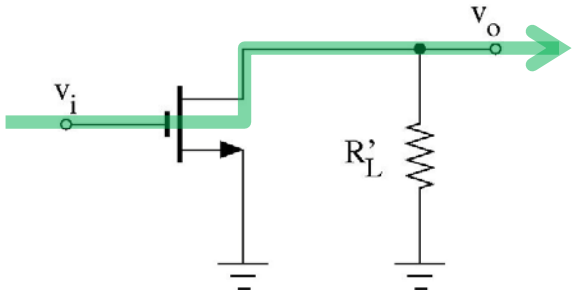
Test book uses current source for biasing (not a practical discrete circuit)



The analysis method introduced here, however, apply to any discrete bias case.

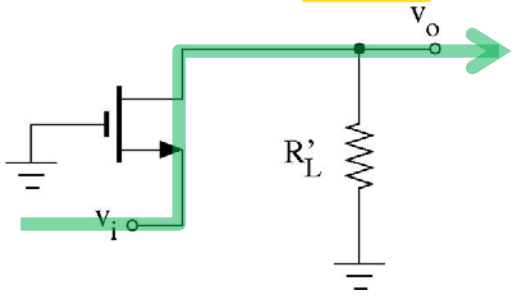
The best way to identify the type of amplifier is to follow the signal

Common Source



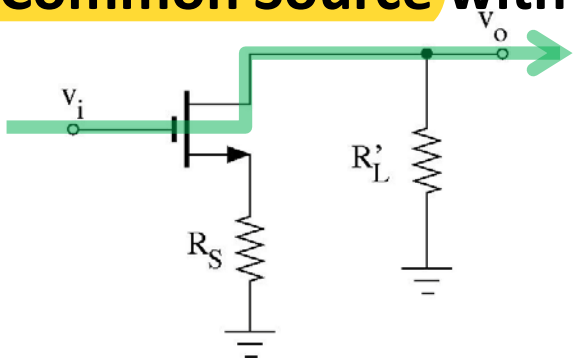
Input at the GATE
Output at the DRAIN

Common Gate



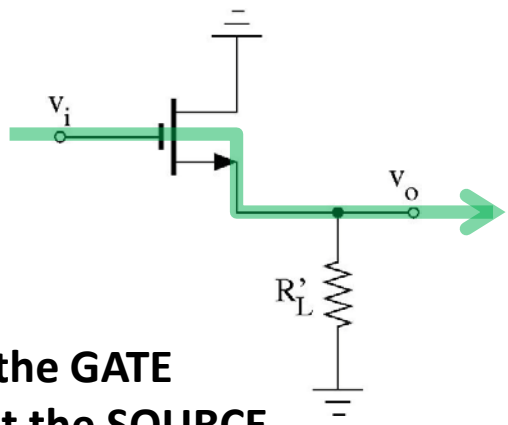
Input at the SOURCE
Output at the DRAIN

Common Source with RS



Input at the GATE
Output at the DRAIN

Common Drain/Source Follower



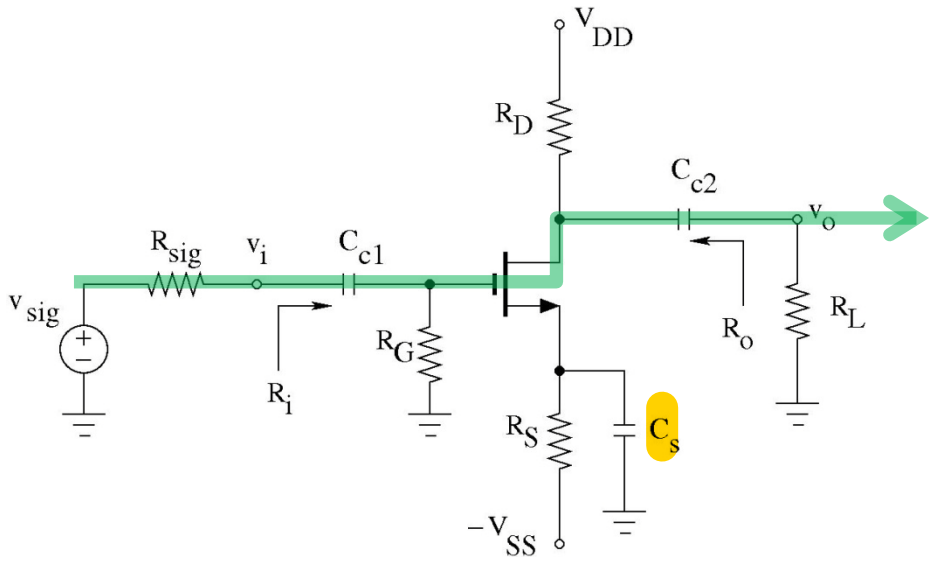
Input at the GATE
Output at the SOURCE

Analysis Steps

Note: We should solve the complete circuit (i.e., include v_{sig}, R_{sig} , R_L in our analysis).

- Compute Bias point.
  - All capacitors are open circuits
  - Compute g_m and r_o
- Draw signal circuit (with MOS intact).
  - Low-frequency Caps are short, high-frequency Caps are open (high-frequency caps discussed later)
- Indentify fundamental amplifier configuration and compute proper amplifier gain (v_o/v_i) and the circuit gain (v_o/v_{sig})
- Use elementary R forms to find R_i and R_o
  - In general R_i will depend on R_L and R_o depends on R_{sig}

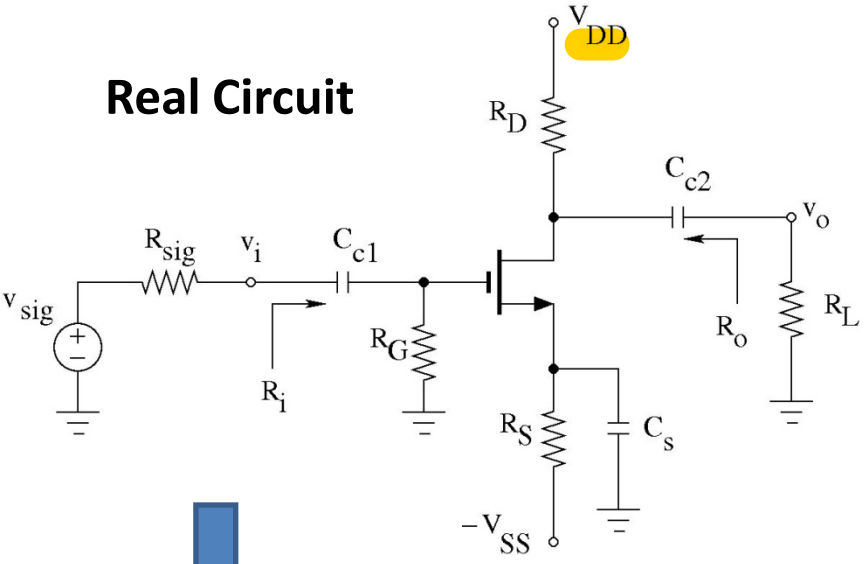
Discrete Common-source Amplifier



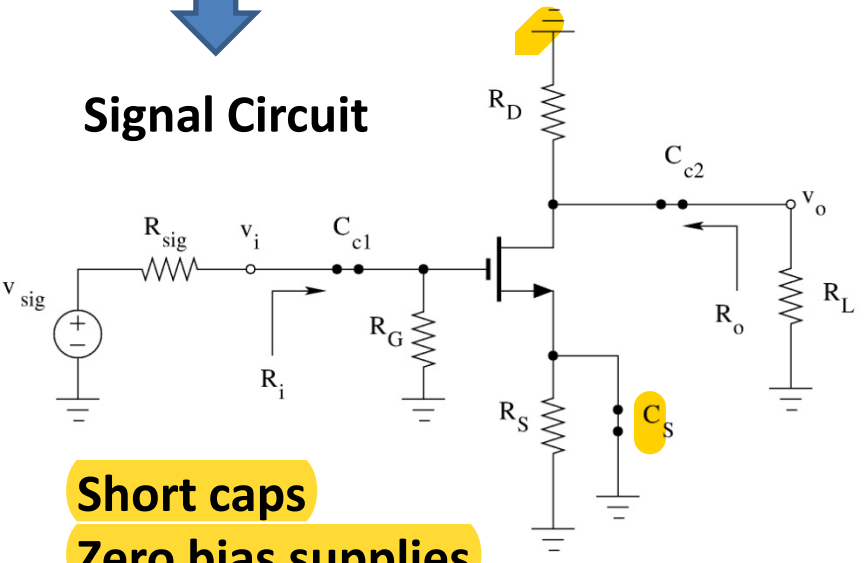
- This is a common-source amplifier (input at the gate and output at the drain).
- Bias calculations are NOT done here as we have done that before.
- Note $\frac{v_i}{v_{sig}} = \frac{R_i}{R_i + R_{sig}}$ (this is true for ALL circuits)

Derivation of small-signal circuit for Discrete CS Amplifier

Real Circuit

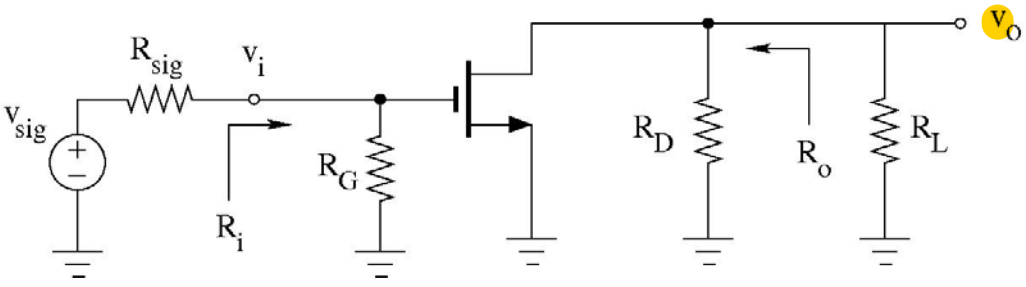


Signal Circuit



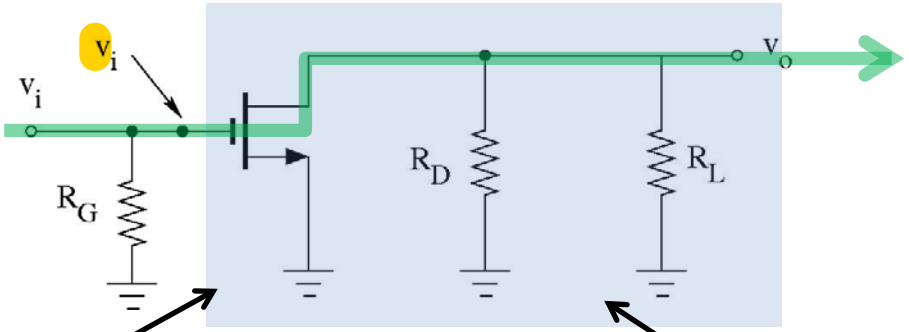
Short caps

Zero bias supplies



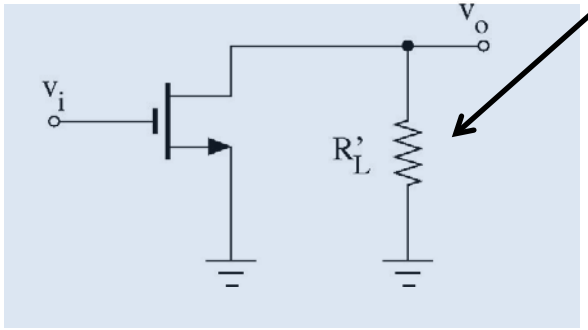
Rearrange

Discrete CS Amplifier – Gain



- ✓ Signal input at the gate
- ✓ Signal output at the drain
- ✓ No R_S

Fundamental CS form



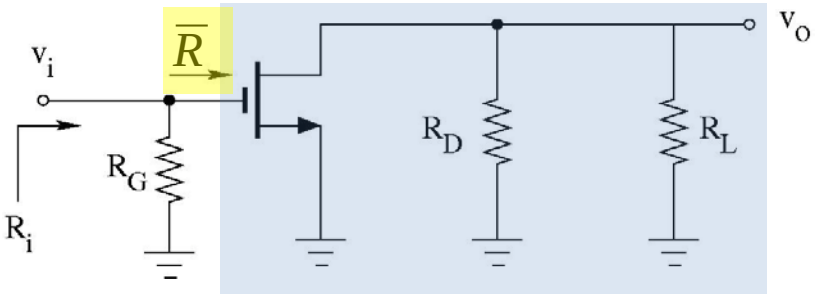
$$R'_L = R_D \parallel R_L$$

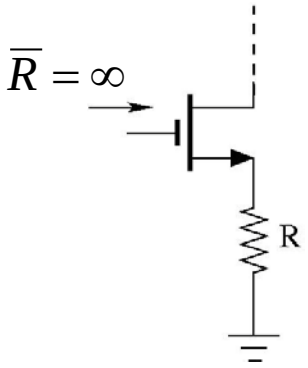
$$\frac{v_o}{v_i} = -g_m(r_o \parallel R_D \parallel R_L)$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i}$$

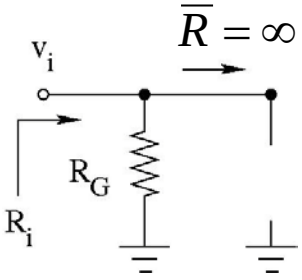
Discrete CS Amplifier – R_i

- ✓ Replace transistor with its equivalent resistance
- ✓ Looking into the gate





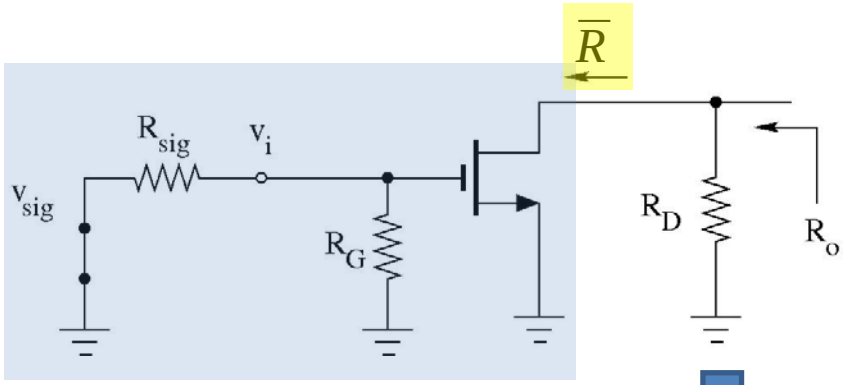
Elementary R Configuration

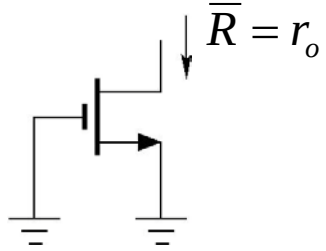


$$R_i = R_G$$

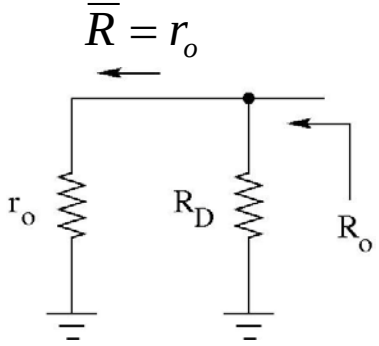
Discrete CS Amplifier – R_o

- ✓ Set $v_{sig} = 0$
- ✓ Replace transistor with its equivalent resistance
- ✓ Since $i_g = 0$, R_{sig} and R_G can be removed ($v_g = 0$)
- ✓ Looking into the drain





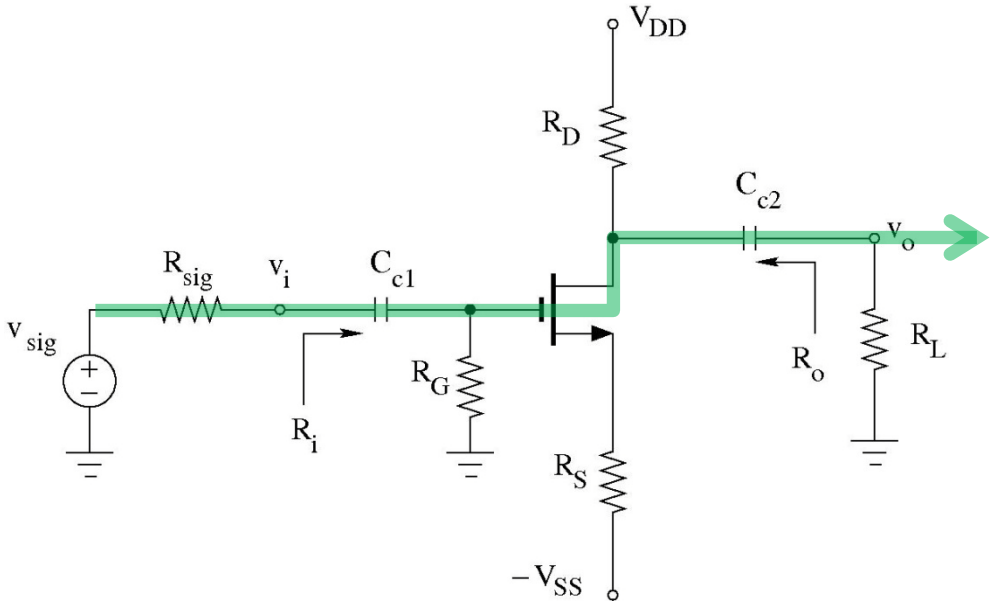
Elementary R Configuration



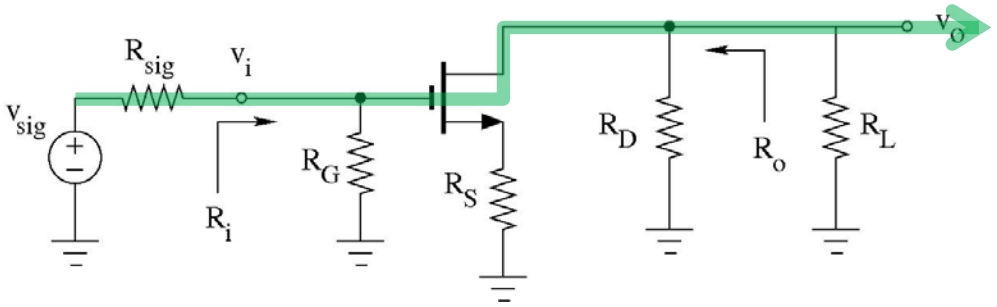
$$R_o = R_D \| r_o$$

Discrete CS Amplifier with R_S

Real Circuit

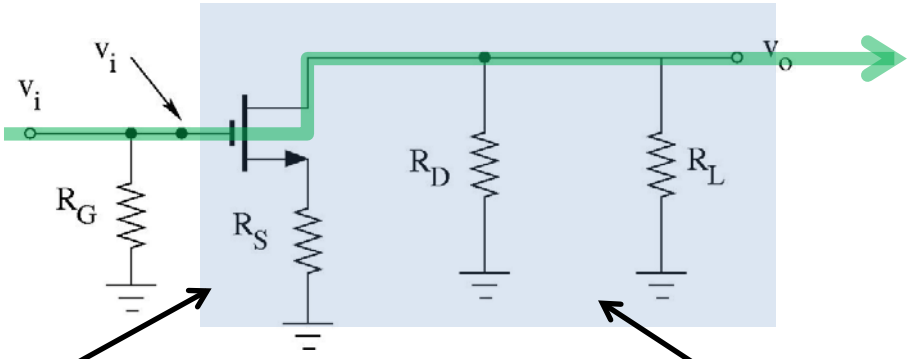


Signal Circuit



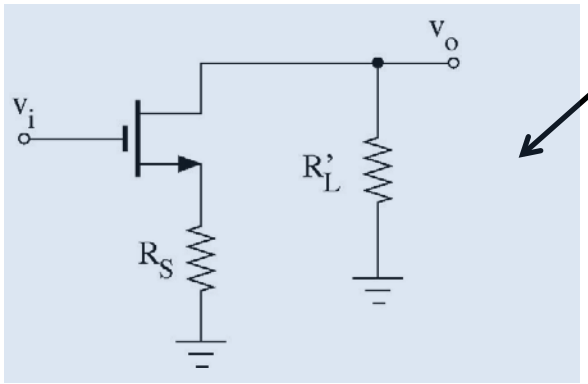
Short caps
Zero bias supplies

Discrete CS Amplifier with R_S – Gain



- ✓ Signal input at the gate
- ✓ Signal output at the drain
- ✓ R_S !

Fundamental CS form with R_S



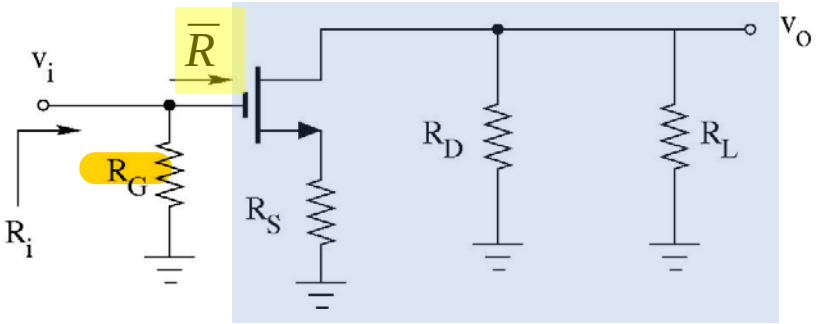
$$R'_L = R_D \parallel R_L$$

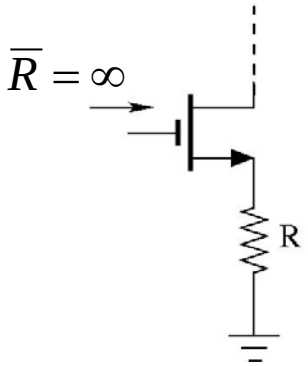
$$\frac{v_o}{v_i} = -\frac{g_m(R_D \parallel R_L)}{1+g_m R_S+(R_D \parallel R_L)/r_o}$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i+R_{sig}} \times \frac{v_o}{v_i}$$

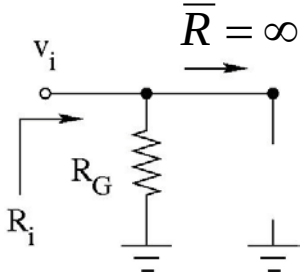
Discrete CS Amplifier with $R_s - R_i$

- ✓ Replace transistor with its equivalent resistance
- ✓ Looking into the gate





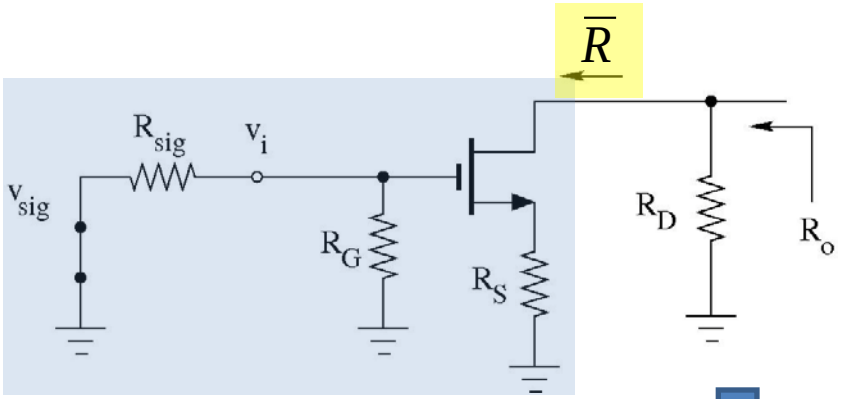
Elementary R Configuration

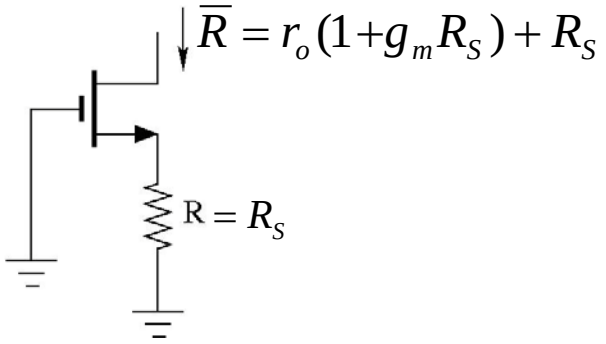


$$R_i = R_G$$

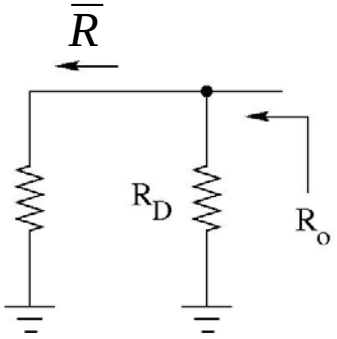
Discrete CS Amplifier with $R_S - R_o$

- ✓ Set $v_{sig} = 0$
- ✓ Replace transistor with its equivalent resistance
- ✓ Since $i_g = 0$, R_{sig} and R_G can be removed ($v_g = 0$)
- ✓ Looking into the drain





Elementary R Configuration

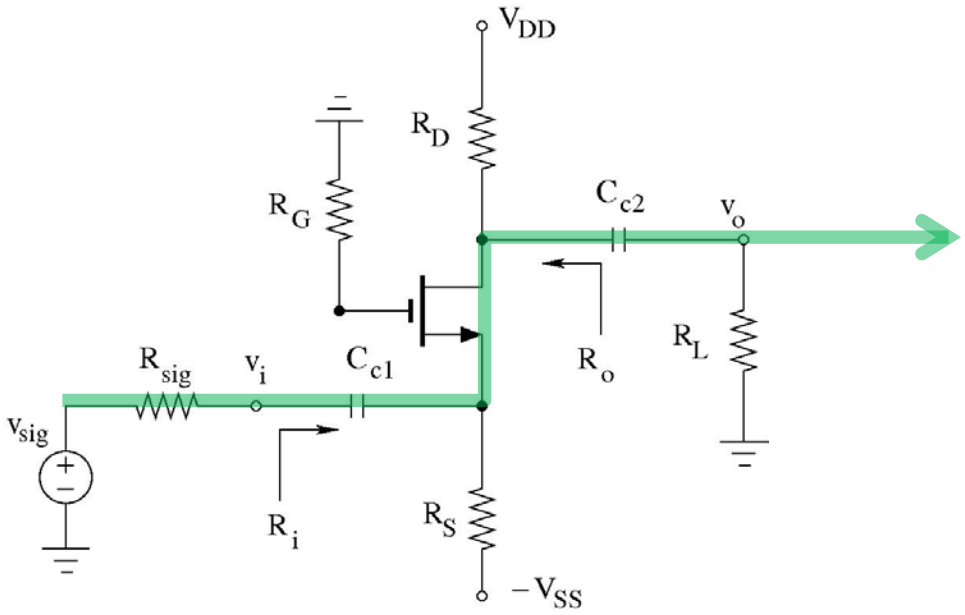


$$\overline{R} = r_o(1+g_m R_S) + R_S$$

$$R_o = R_D \,\|\, [r_o(1+g_m R_S) + R_S]$$

Discrete CG Amplifier

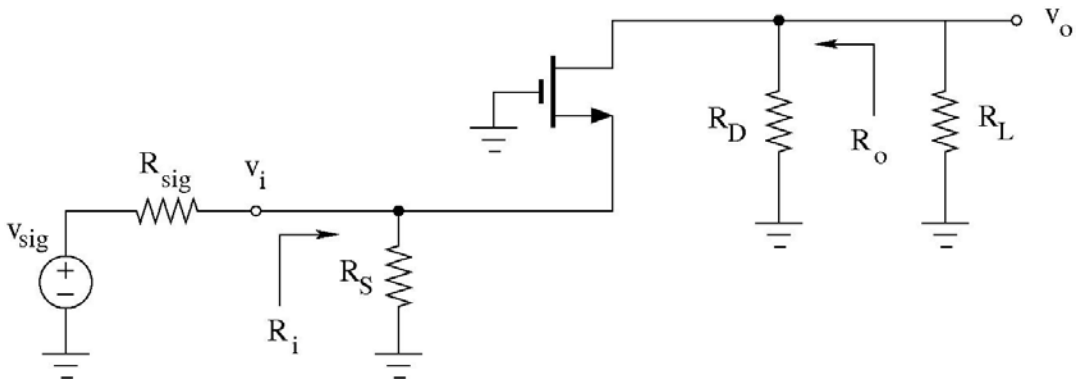
Real Circuit



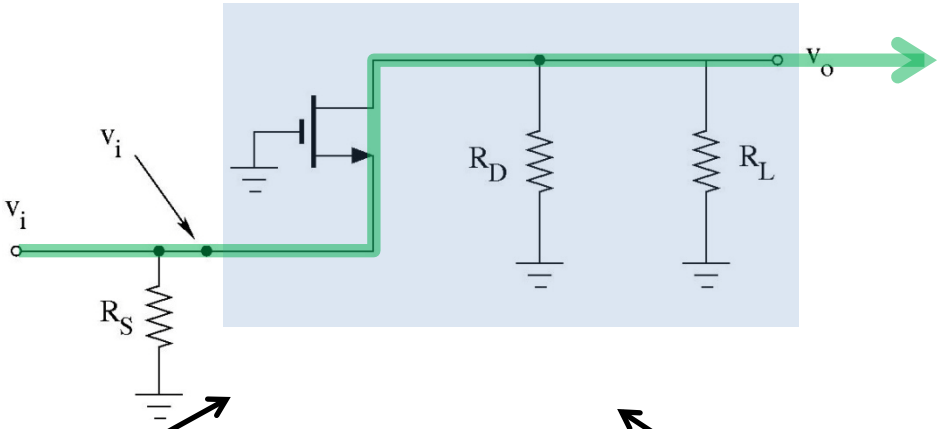
Short caps

Zero bias supplies

Signal Circuit

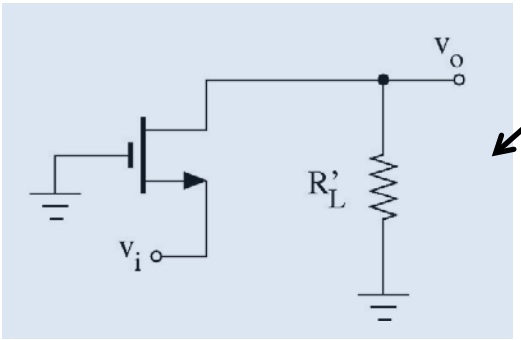


Discrete CG Amplifier – Gain



- ✓ Signal input at the source
- ✓ Signal output at the drain

Fundamental CG form



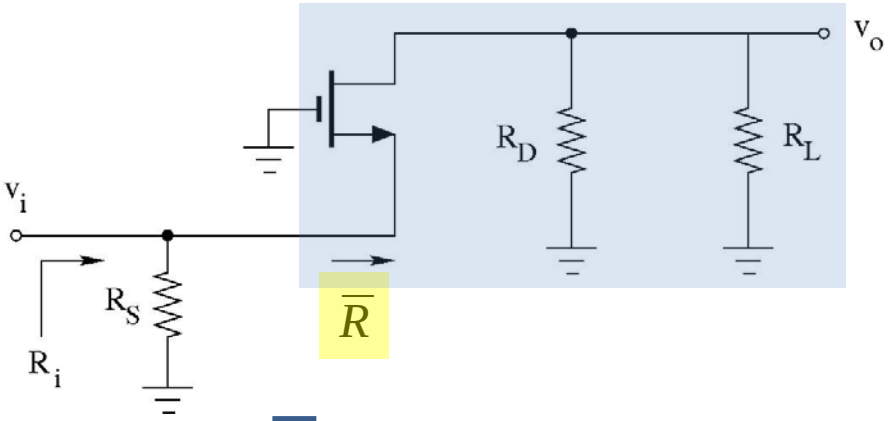
$$R_L' = R_D \parallel R_L$$

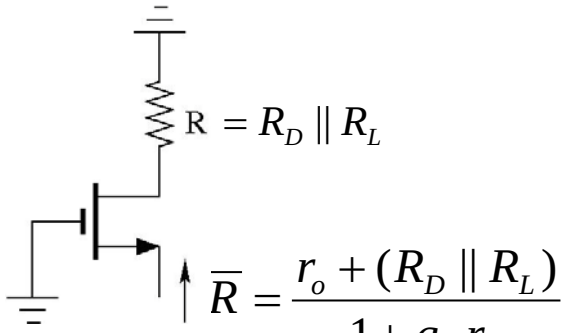
$$\frac{v_o}{v_i} = +g_m(r_o \parallel R_D \parallel R_L)$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i}$$

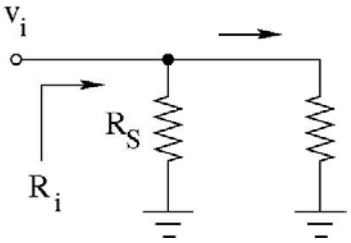
Discrete CG Amplifier – R_i

- ✓ Replace transistor with its equivalent resistance
- ✓ Looking into the source





Elementary R Configuration

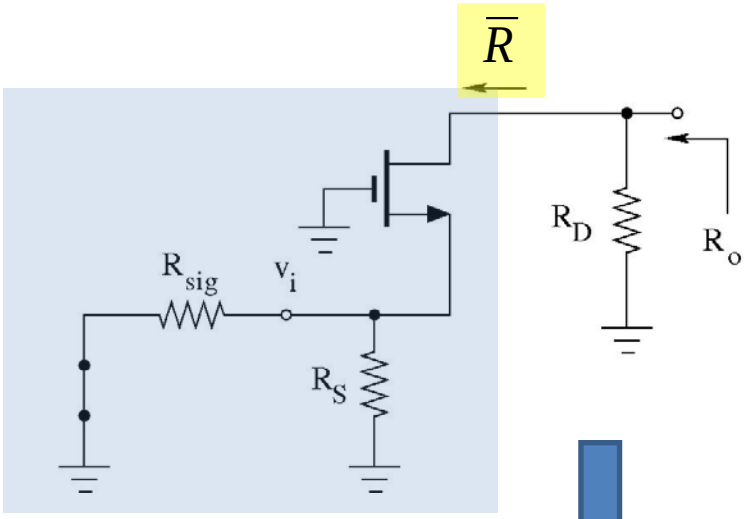


$$\overline{R} = \frac{r_o + (R_D \parallel R_L)}{1 + g_m r_o}$$

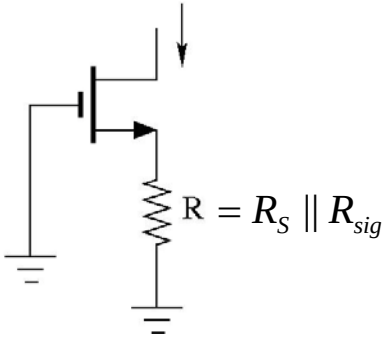
$$R_i = R_S \parallel \left[\frac{r_o + (R_D \parallel R_L)}{1 + g_m r_o} \right]$$

Discrete CG Amplifier – R_o

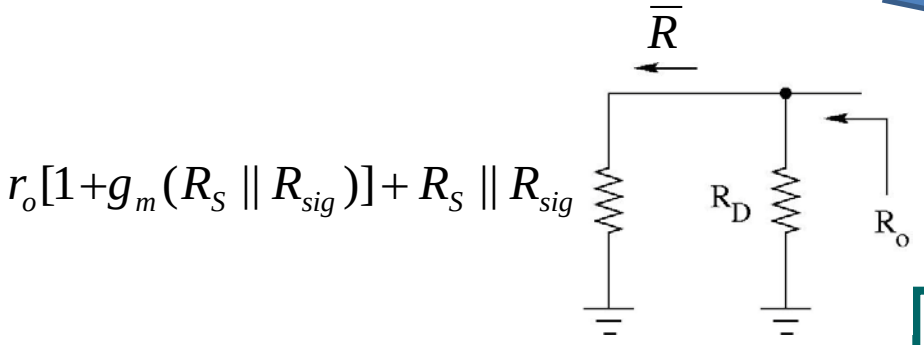
- ✓ Set $v_{sig} = 0$
- ✓ Replace transistor with its equivalent resistance
- ✓ Looking into the drain



$$\overline{R} = r_o[1+g_m(R_S \parallel R_{sig})] + R_S \parallel R_{sig}$$



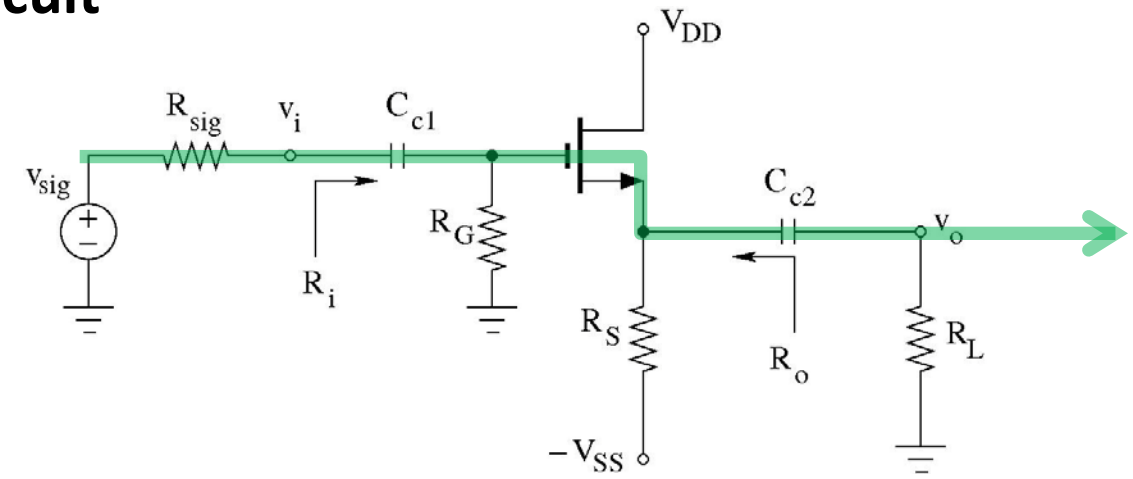
Elementary R Configuration



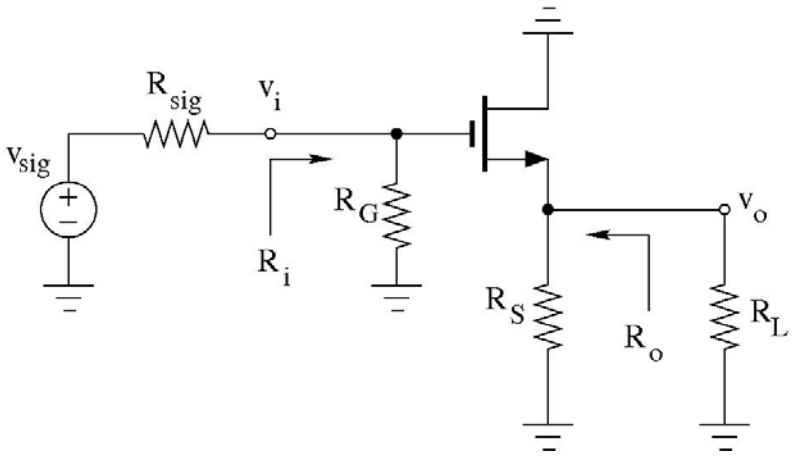
$$R_o = R_D \parallel \{r_o[1+g_m(R_S \parallel R_{sig})] + R_S \parallel R_{sig}\}$$

Discrete CD Amplifier (Source Follower)

Real Circuit

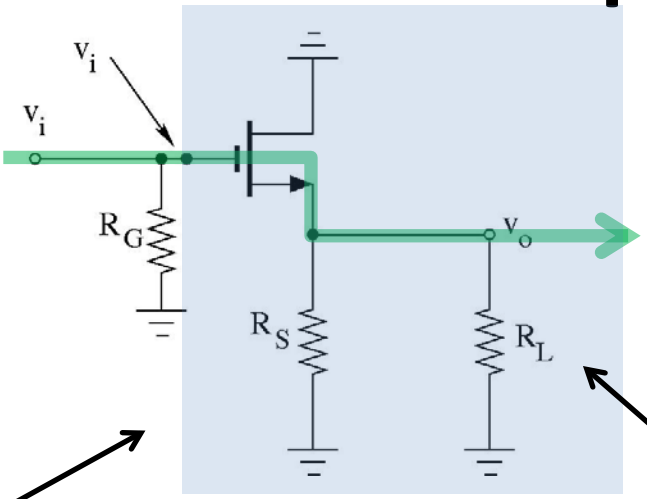


Signal Circuit



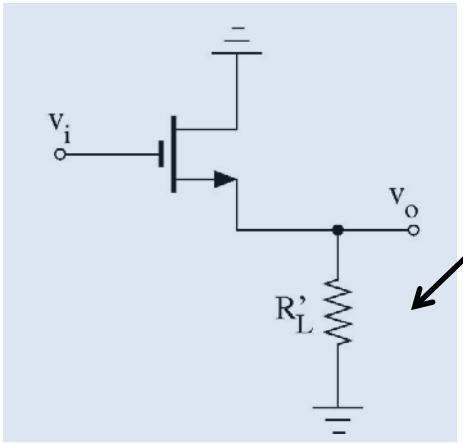
Short caps
Zero bias supplies

Discrete CG Amplifier – Gain



✓ Signal input at the gate
✓ Signal output at the source

Fundamental CS form



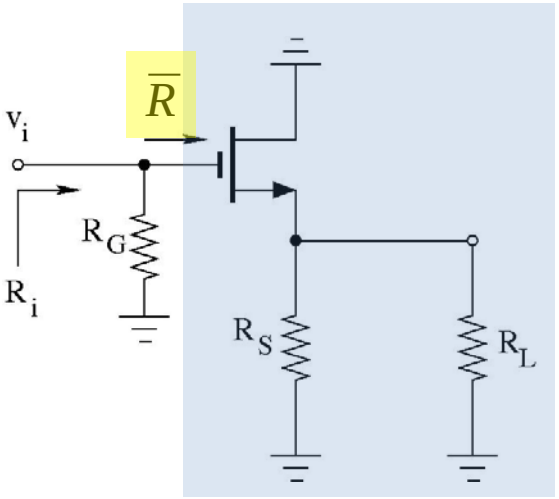
$$R_L' = R_S \parallel R_L$$

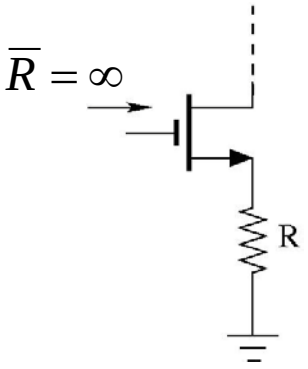
$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)}$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i}$$

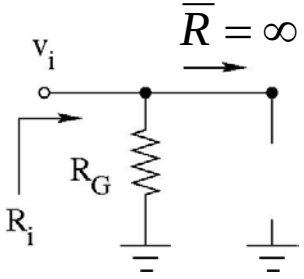
Discrete CG Amplifier – R_i

- ✓ Replace transistor with its equivalent resistance
- ✓ Looking into the gate





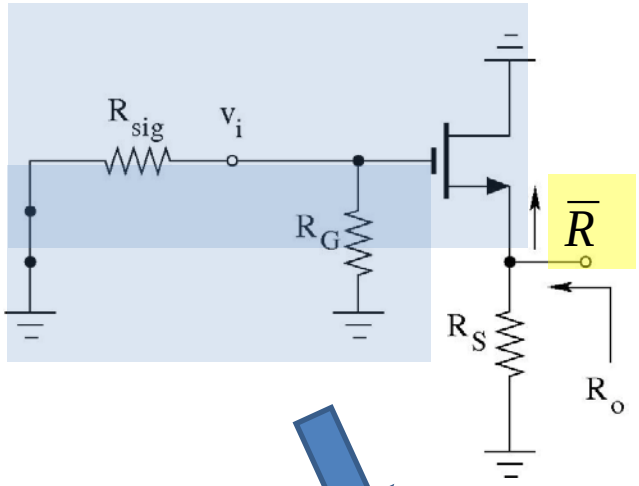
Elementary R Configuration

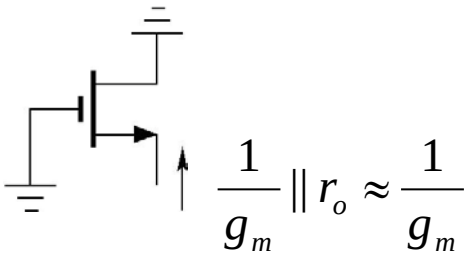


$$R_i = R_G$$

Discrete CG Amplifier – R_o

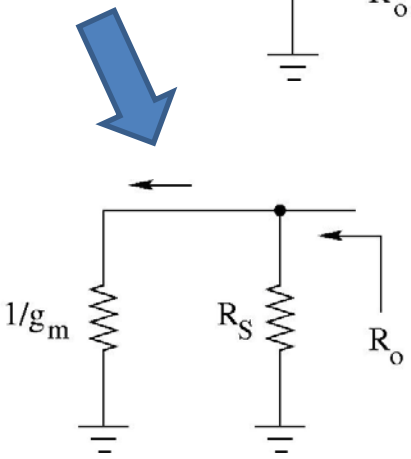
- ✓ Set $v_{sig} = 0$
- ✓ Replace transistor with its equivalent resistance
- ✓ Since $i_g = 0$, R_{sig} and R_G can be removed ($v_g = 0$)
- ✓ Looking into the source





$$\frac{1}{g_m} \| r_o \approx \frac{1}{g_m}$$

Elementary R Configuration



$$R_o = R_S \| \frac{1}{g_m}$$