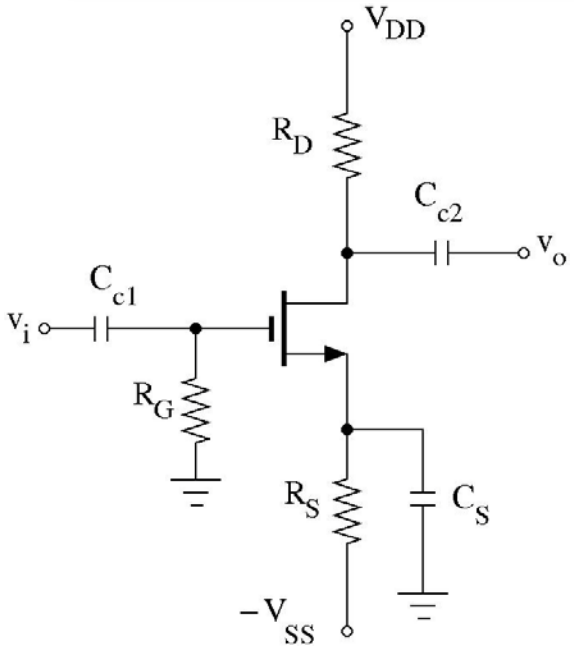
5. Active Loads and IC MOS Amplifiers

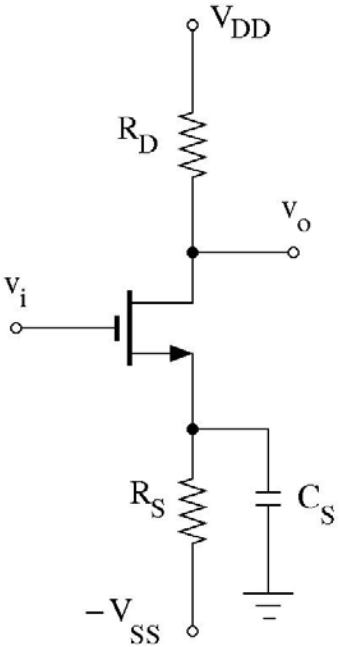
Sedra & Smith Sec. 7 (MOS portion)

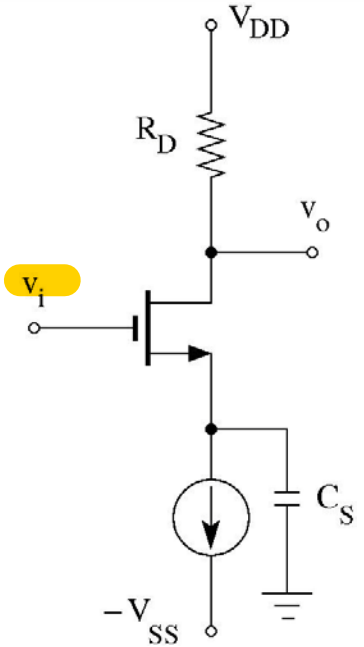
(S&S 5th Ed: Sec. 6 MOS portion & ignore frequency response)

Progress towards an IC relevant amplifier

- Resistors and capacitors take a lot of space on ICs:
  - Minimize (i.e., very few) R & C and small sizes (e.g., nF or smaller)





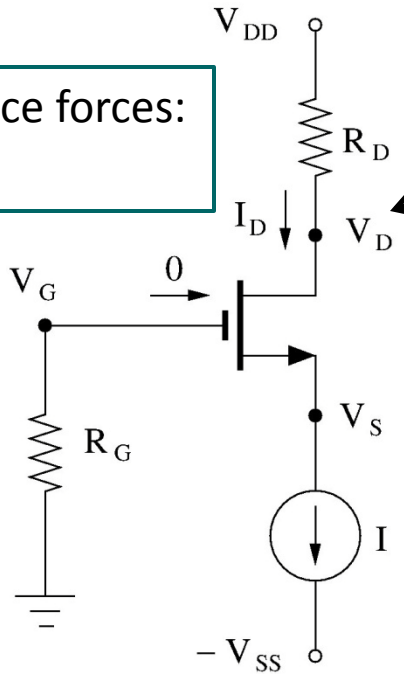


- Get rid of coupling capacitors by direct coupling between stages (makes biasing design complicated)
- v_i and v_o include DC bias components

- Replace Rs with a current source
- Still need to get rid of C_s
- What to do about R_D?

Biasing in ICs

- Resistors take too much space on the chip. So, source degeneration with R_S is NOT implemented in ICs.
- Recall that the goal of a good bias is to ensure I_D and V_{DS} would not change (e.g., due to temperature variation). One can force I_D to be constant using a current source.



1) Current source forces:
$I_D = I$

2) $V_D = V_{DD} - R_D I_D$

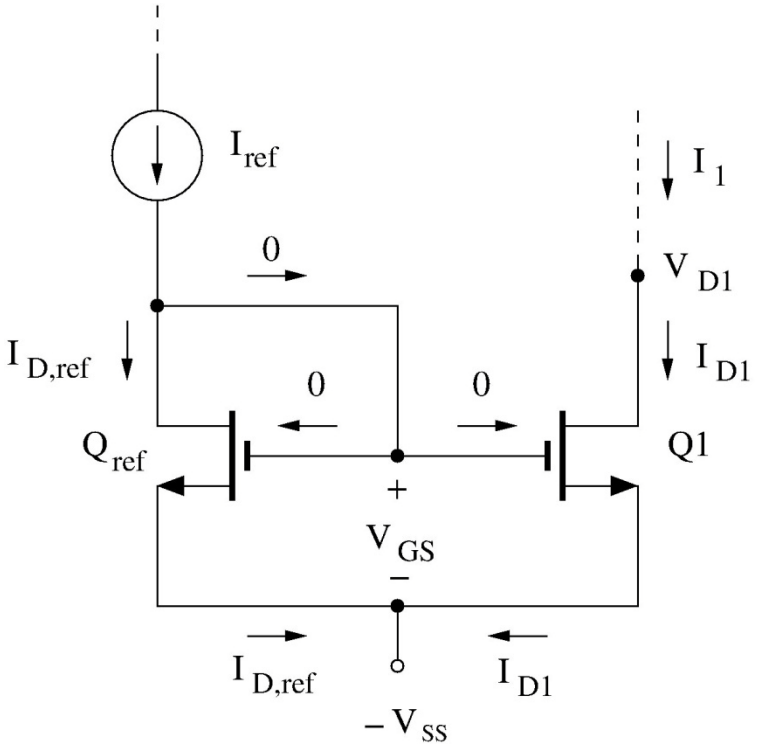
3) V_{GS} is set by
$I_D = 0.5\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)^2$

4) $V_S = V_G - V_{GS} = -V_{GS}$

5) $V_{DS} = V_D - V_S$

Current Mirrors or Current Steering Circuits are used as current sources for biasing ICs

Identical MOS:
Same μC_{ox} and V_t



- **Qref is <u>always</u> in saturation since**

$$V_{DS,ref} = V_{GS,ref} > V_{GS,ref} - V_t$$

- $V_{GS,ref} = V_{GS1} = V_{GS}$
- $V_{OV,ref} = V_{OV1} = V_{OV}$

$$I_{ref} = I_{D,ref} = 0.5\mu_n C_{ox}\left(\frac{W}{L}\right)_{ref} V_{OV}^2$$

$$I_1 = I_{D1} = 0.5\mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{OV}^2$$

$$\frac{I_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}}$$

- **Circuit works as long as Q1 is in saturation:** $V_{DS1} > V_{OV} = V_{GS} - V_t$

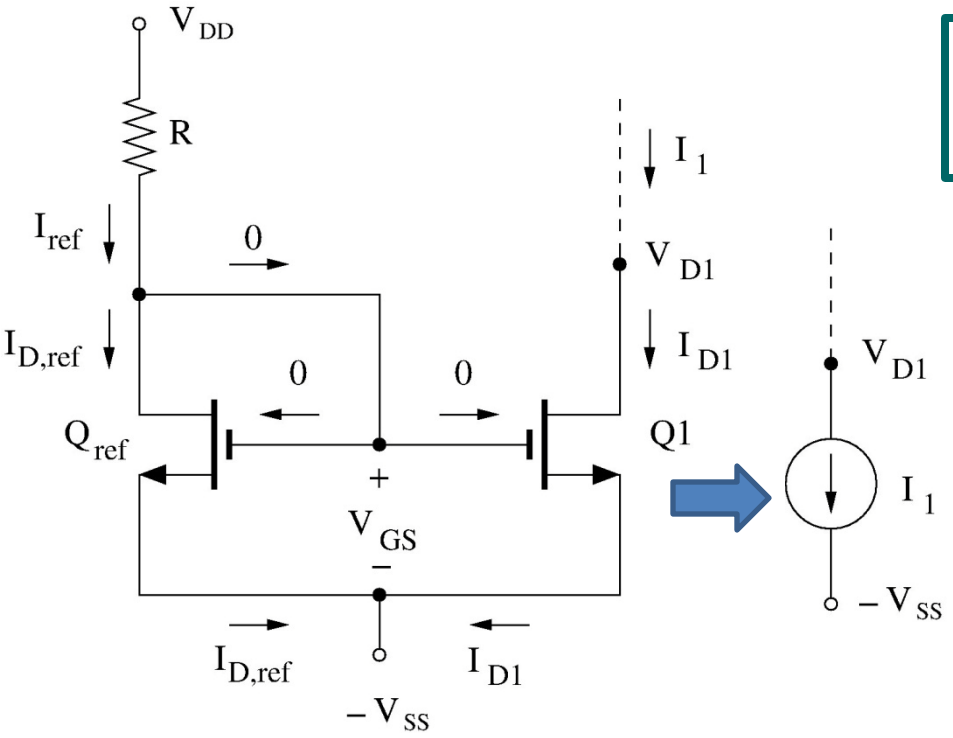
An implementation of a Current Mirror

Identical MOS:
Same μC_{ox} and V_t

$$\text{DS-KVL}: V_{DD} = RI_{ref} + V_{GS} - V_{SS}$$

$$RI_{ref} + V_{GS} = V_{DD} + V_{SS}$$

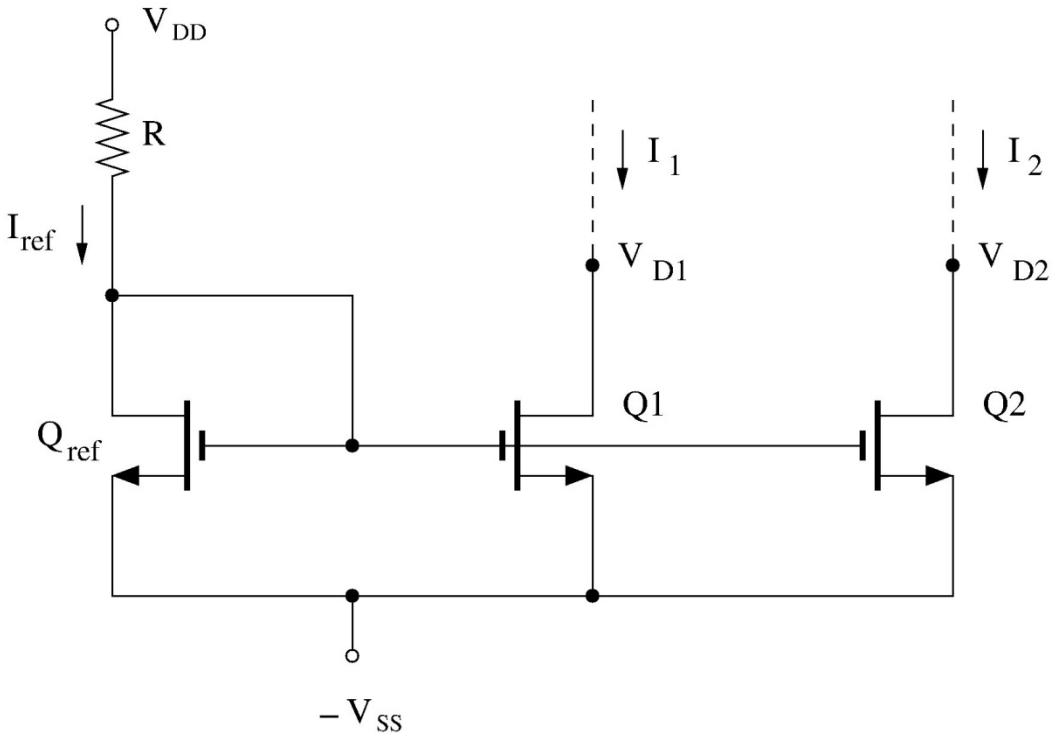
$$I_{ref} = I_{D,ref} = 0.5\mu_n C_{ox}(W/L)_{ref}\,(V_{GS} - V_t)^2$$



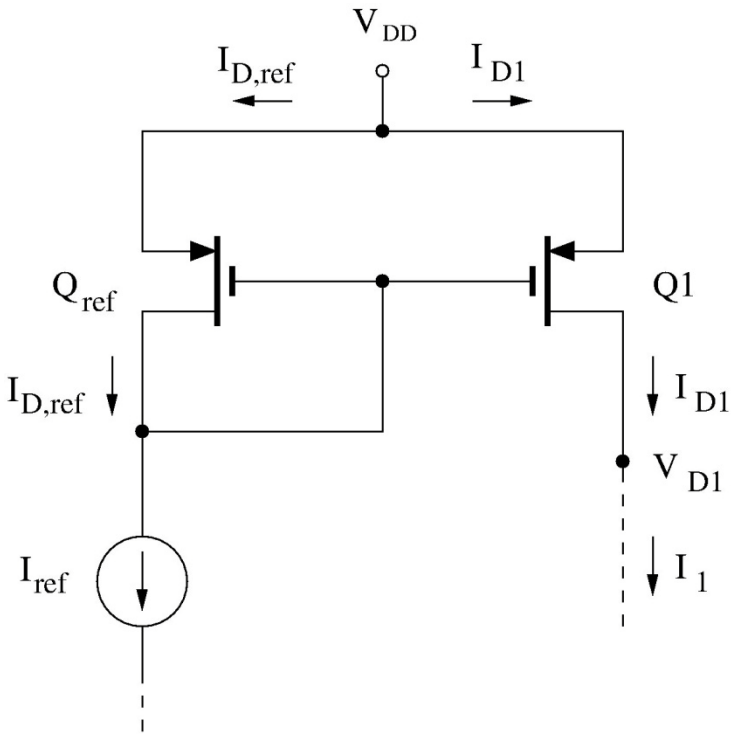
The above 2 equations uniquely set Qref Bias point ($I_{D,ref}$ and $V_{GS,ref} = V_{DS,ref}$)

- Current mirror: $\dfrac{I_1}{I_{ref}} = \dfrac{(W/L)_1}{(W/L)_{ref}}$
- **Since I_1 = constant regardless of voltage, this is a current source!**
- **Note:** Circuit works as long as Q1 is in saturation.

Examples of Current Steering circuits



Current steering circuit can bias several transistors

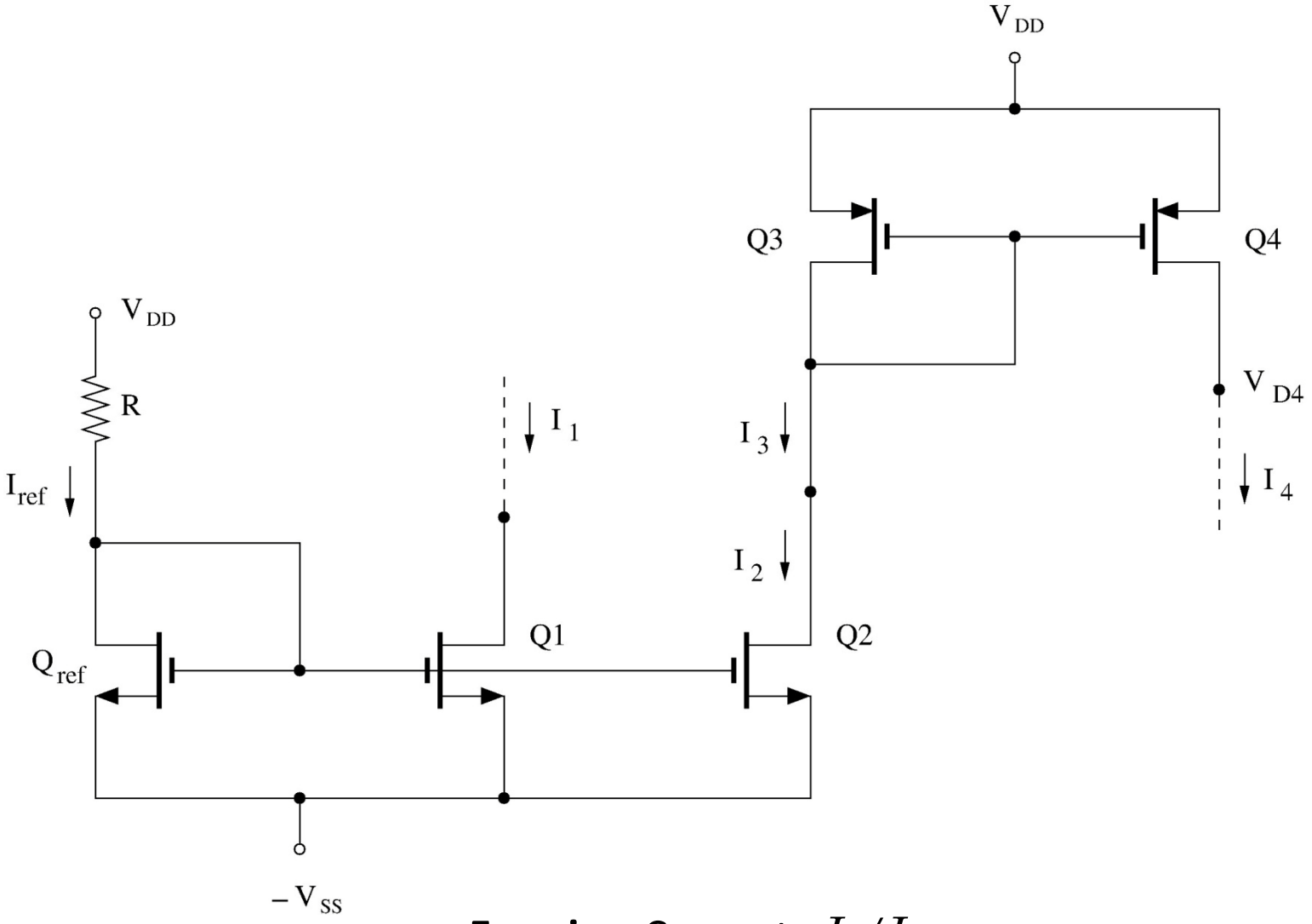


A PMOS current mirror

$$\frac{I_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}} \qquad \frac{I_2}{I_{ref}} = \frac{(W/L)_2}{(W/L)_{ref}}$$

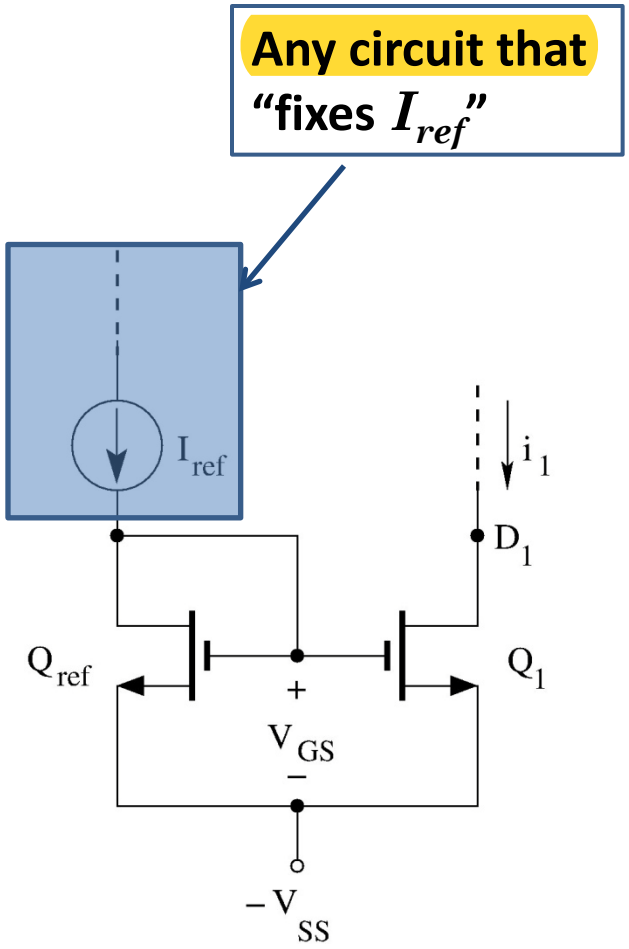
$$\frac{I_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}}$$

An implementation of current steering circuit to bias several transistors in an IC



Exercise: Compute I_4 / I_{ref}

Current steering circuits are not "ideal" current sources!



If we do NOT ignored Channel width modulation:

$$v_{DS,ref} = v_{GS,ref} = v_{GS} \Rightarrow \text{Q}_{ref} \text{ in saturation}$$

$$i_{D,ref} = \frac{1}{2}\mu_n C_{ox}(W/L)_{ref}\,(v_{GS} - V_t)^2(1+\lambda v_{GS})$$

$$i_{D,ref} = I_{ref} \Rightarrow \text{uniquely sets } v_{GS}$$

$$i_1 = i_{D1} = \frac{1}{2}\mu_n C_{ox}(W/L)_1\,(v_{GS} - V_t)^2(1+\lambda v_{DS1})$$

$$\frac{i_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}} \times \frac{(1+\lambda v_{DS1})}{(1+\lambda v_{GS})}$$

Channel width modulation is important in the signal response.

	Ignoring channel width modulation	**Keeping channel width modulation**
	$i_{D1} = I_{ref} \times \frac{(W/L)_1}{(W/L)_{ref}}$	$i_{D1} = I_{ref} \times \frac{(W/L)_1}{(W/L)_{ref}} \times \frac{(1+\lambda v_{DS1})}{(1+\lambda V_{GS})}$
Bias (v_{ds1}=0):	$I_{D1} = I_{ref} \times \frac{(W/L)_1}{(W/L)_{ref}}$	$I_{D1} = I_{ref} \times \frac{(W/L)_1}{(W/L)_{ref}} \times \frac{(1+\lambda V_{DS1})}{(1+\lambda V_{GS})}$

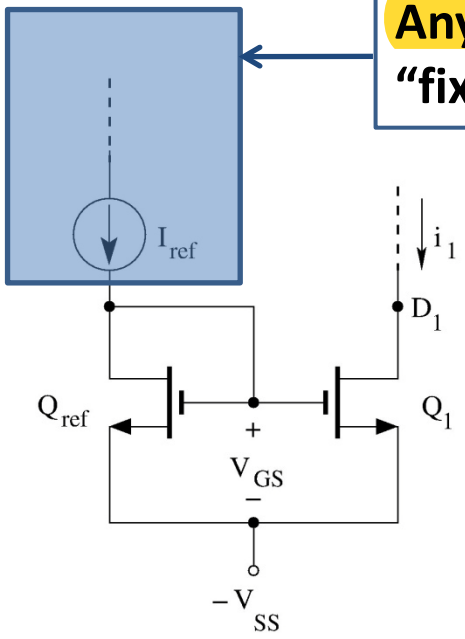
One can usually ignore channel width modulation in biasing calculations because λ is small (See Exercise 3 of the Problem Set)

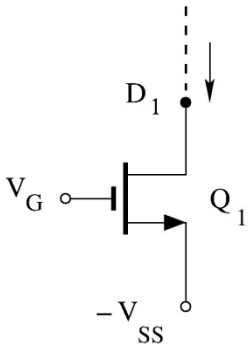
Signal (v_{ds1}≠0): $i_{d1} = 0$ (open circuit) $\quad i_{d1} = f(v_{ds1})$ (an element)

One cannot ignore channel width modulation in signal response (We need to find the small signal model).

Small signal Model of Current Mirrors: Using Elementary R Forms

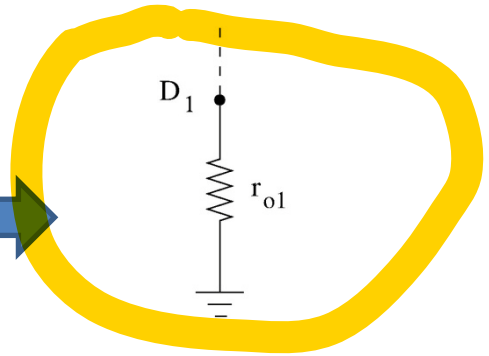
Any circuit that "fixes I_{ref}"





V_{GS} = const.

Small Signal Model



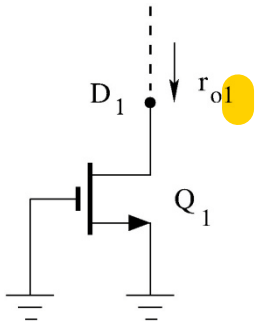
$V_{DS,ref} = V_{GS,ref} = V_{GS} \Rightarrow$ Q_{ref} in saturation

$$i_{D,ref} = \frac{1}{2}\mu_n C_{ox}(W/L)_{ref}(V_{GS} - V_t)^2(1 + \lambda V_{GS})$$

$i_{D,ref} = I_{ref} \Rightarrow$ uniquely sets V_{GS}

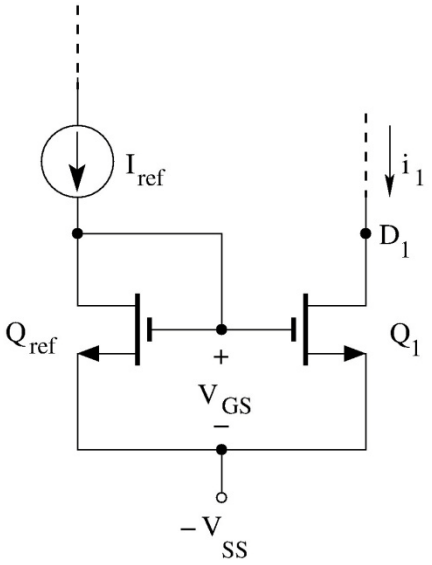
$V_G = V_{GS} - V_{SS} = const.$

Elementary R form



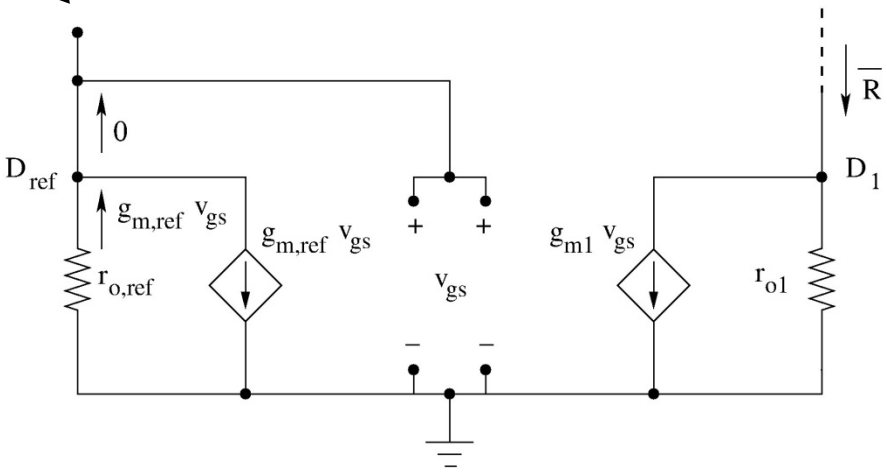
Small signal Model of Current Mirrors: Using MOS SSM Model

Real Circuit



Ideal current source becomes open circuit

Small Signal Model



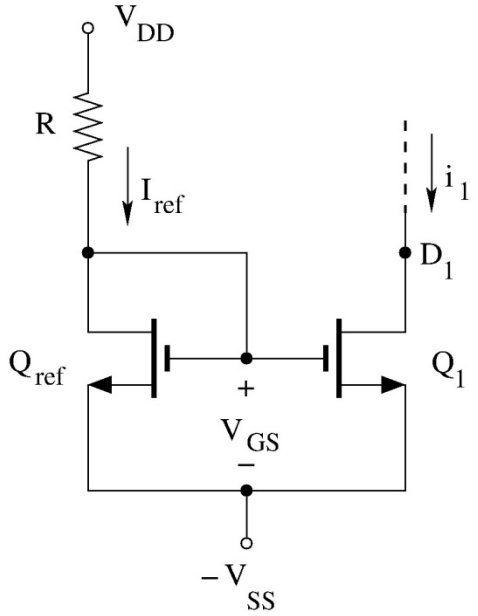
KCL at Dref : $g_{m,ref} v_{gs}$ flows in $r_{o,ref}$

$$v_{D,ref} = v_{gs} = -g_{m,ref} v_{gs} r_{o,ref} \Rightarrow (1 + g_{m,ref} r_{o,ref}) v_{gs} = 0 \Rightarrow v_{gs} = 0$$

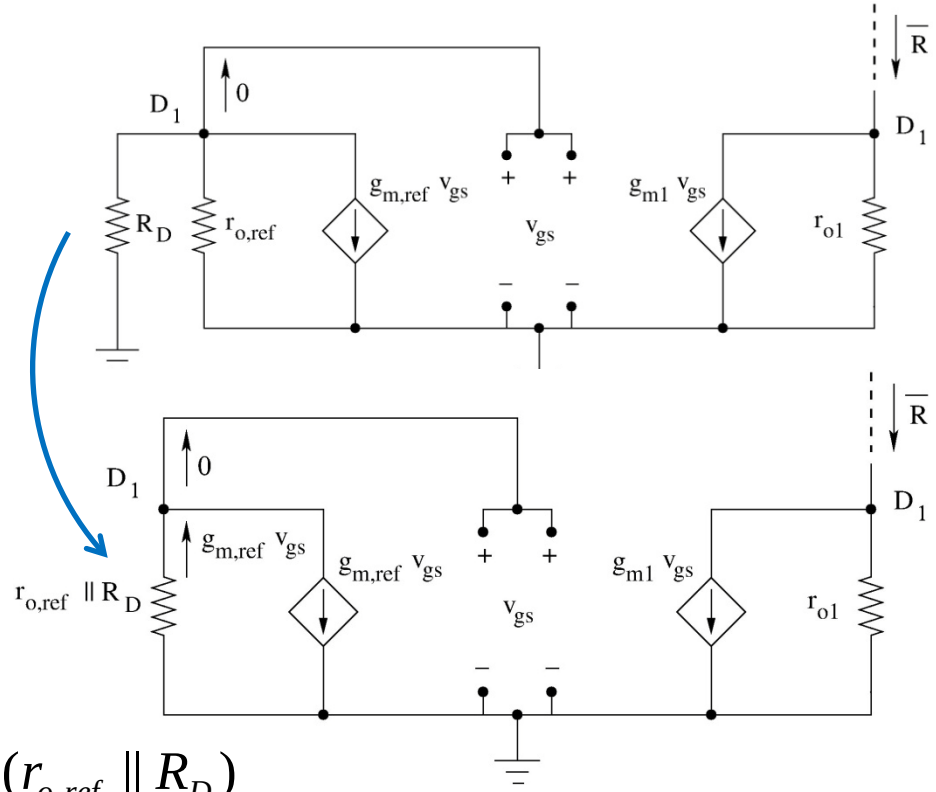
$v_{gs} = 0 \Rightarrow g_{m1} v_{gs}$ current source is an open circuit $\Rightarrow$ $\boxed{\overline{R} = r_{o1}}$

But what happens if we replace I_{ref} ideal current source with "practical" elements?

Practical Circuit



Small Signal Model



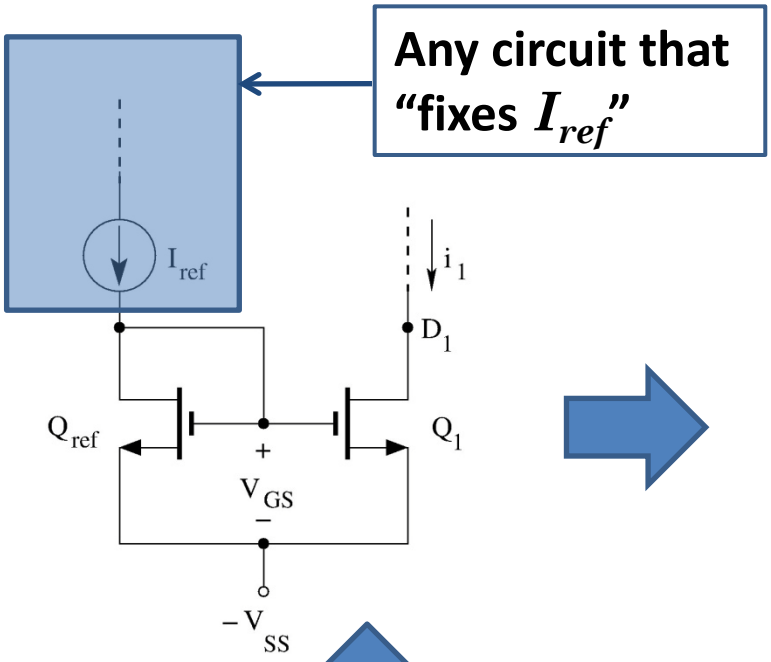
KCL at Dref : $g_{m,ref} v_{gs}$ flows in $(r_{o,ref} \parallel R_D)$

$$v_{D,ref} = v_{gs} = -g_{m,ref} v_{gs} r_{o,ref} \Rightarrow [1 + g_{m,ref}(r_{o,ref} \parallel R_D)] v_{gs} = 0 \Rightarrow v_{gs} = 0$$

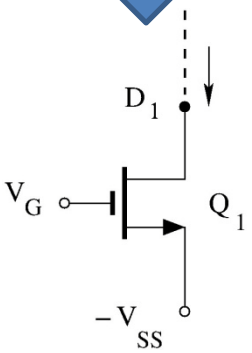
$v_{gs} = 0 \Rightarrow g_{m1} v_{gs}$ current source is open circuit

$$\overline{R} = r_{o1}$$

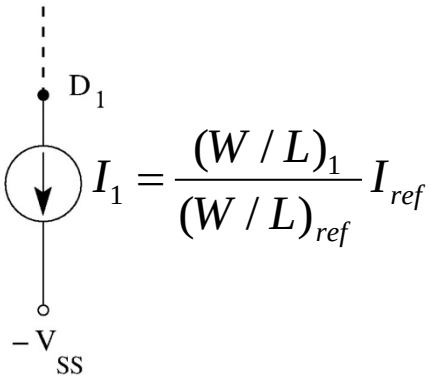
Summary of MOS Current Steering Circuit



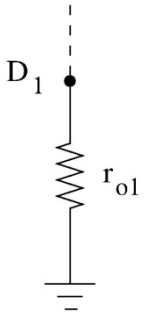
Equivalent circuit



Bias Model

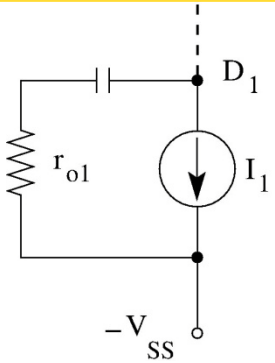


Small Signal Model



"Intuitive" Model

Signal current goes through this leg (∞ capacitor)



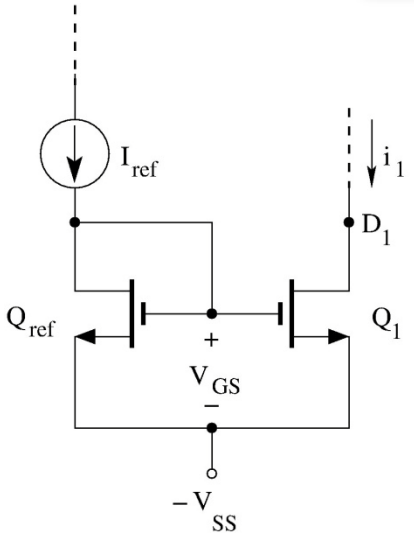
Bias current goes through this leg

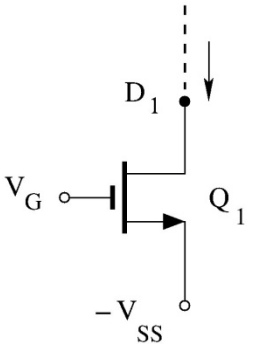
Summary of MOS Current Steering Circuit

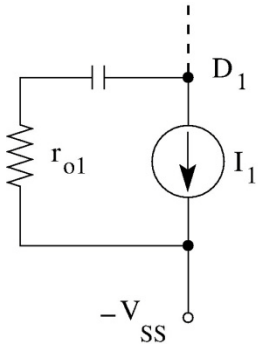
It is sufficient to only consider Q1 in circuit calculations

“Intuitive” Model

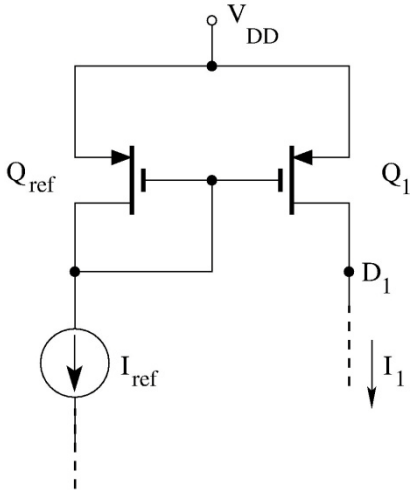
NMOS Version:

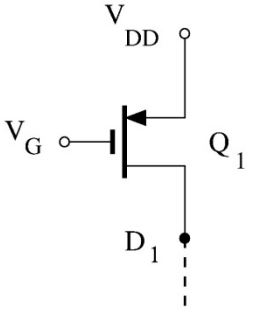


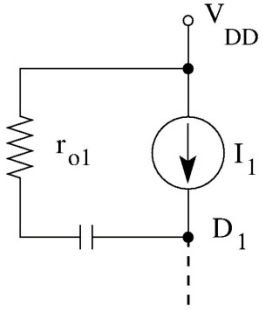




PMOS Version:

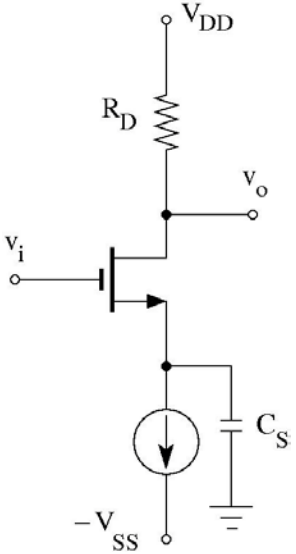


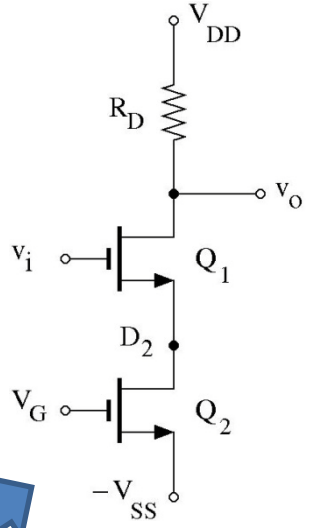




Biasing a CS Stage: Can we place a current mirror in the source circuit?

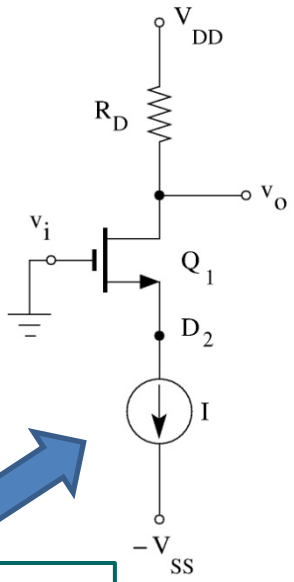
Typical bias of a discrete CS amplifier





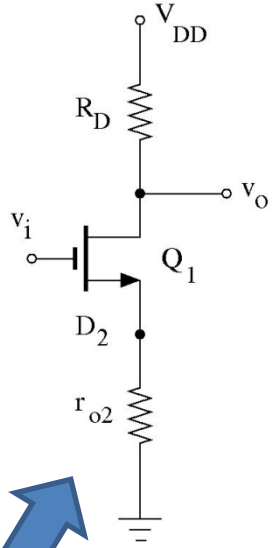
Current mirror

Bias



Bias works fine!

Small Signal

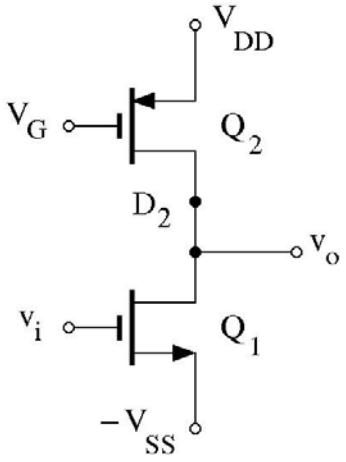


- **Placing a current mirror in the source circuit will not Work!**

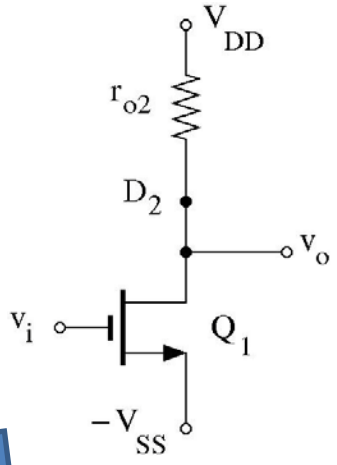
- A large R (r_{o2}) in the source circuit reduces the gain by about $g_{m1}\, r_{o2}$

$$A_v = -\frac{g_{m1}R'_L}{1+R'_L/r_{o1}} \quad \text{versus} \quad A_v = -\frac{g_{m1}R'_L}{1+g_{m1}r_{o2}+R'_L/r_{o1}}$$

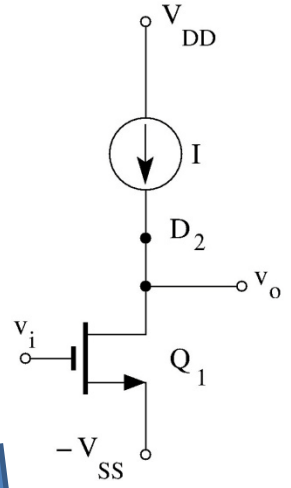
We need to Bias a CS Stage by placing a current mirror in the drain circuit!



Signal



Bias



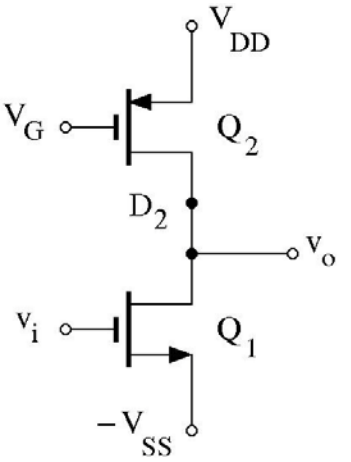
Current mirror provides a large R_D and a high gain:

$$A_v = -g_{m1}(r_{o1} \| r_{o2})$$

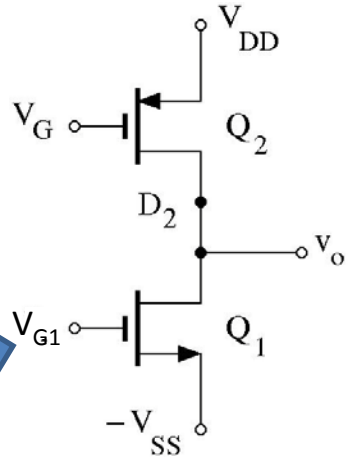
- Current mirror sets $I_D = I$
- However, a precise bias voltage should be applied to the gate of Q1 (corresponding to the I_D set by the current source)
  - Several ways to do this

Important Point

- Bias is the state of the system with no signal.
  - We set $v_i = 0$ (or $v_{sig} = 0$) to find the bias values
- In directly-coupled amplifier (see Problem Set 4, Exercise 6), a combination of bias voltage and input signal is applied to the amplifier.
- For example, in the circuit shown , a combination of signal (v_i) and a bias voltage (V_{G1}) is applied to the gate of Q1.
- As we are mostly interested in the signal response, the convention is NOT to show the bias voltage at the input on the circuit.
  - A bias voltage of (V_{G1}) is implied!
  - You should NOT connect G1 to the ground (i.e., setting $v_i = 0$) to find the bias point.



Bias



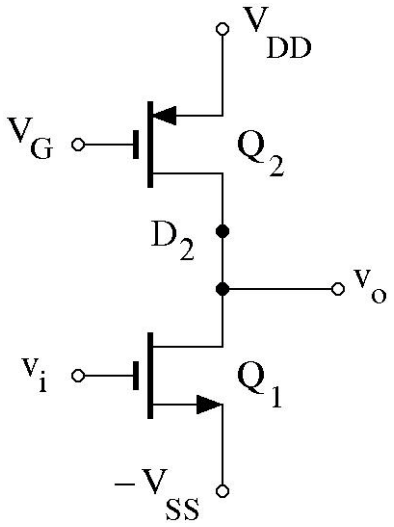
Bias point of CS amp with current mirror

- Ignore Channel Width Modulation,
  - Fast and relatively accurate method to find bias point, g_{m1} , r_{o1} and r_{o2}
  - Cannot find V_{DS1} and V_{DS2}

Q2: $V_{SG2} = V_{DD} - V_G$

$V_{OV2} = V_{SG2} - |V_{tp}|$

$$I_{D2} = 0.5\mu_p C_{ox}\left(\frac{W}{L}\right)_2 V_{OV2}^2$$



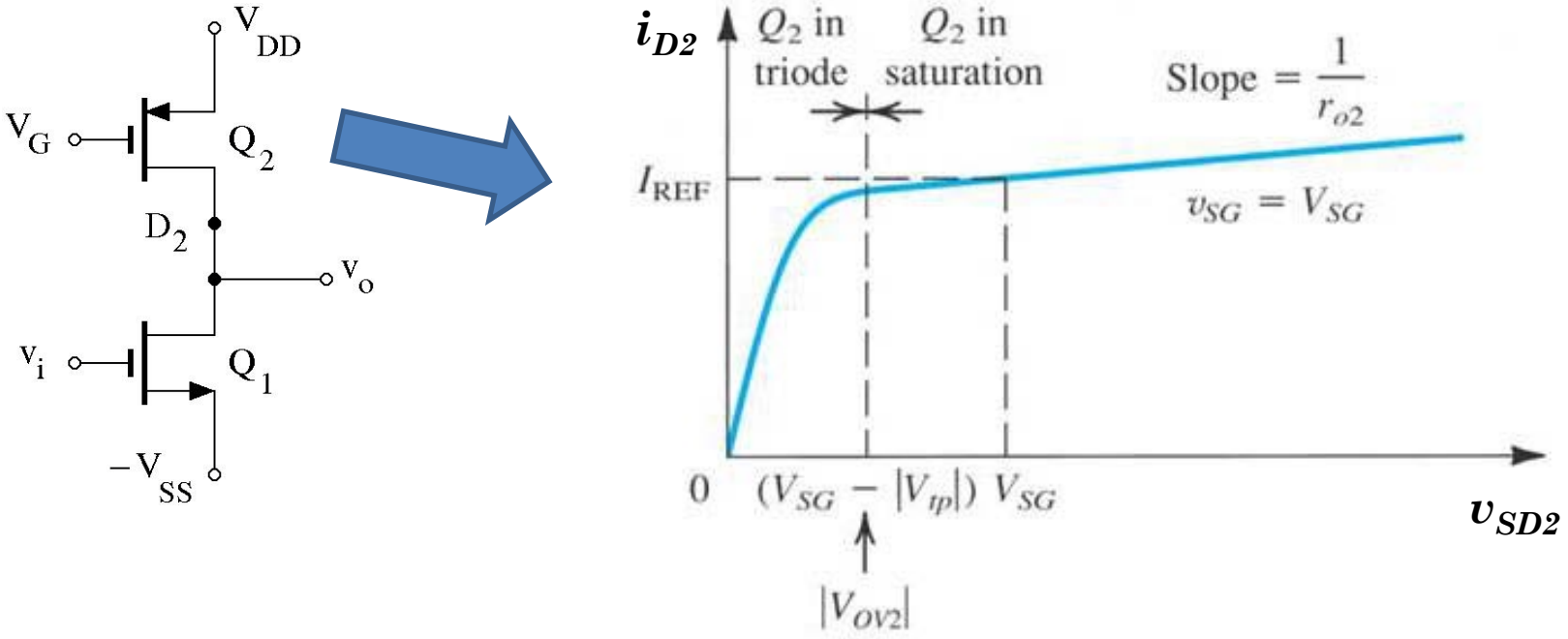
Q1: $I_{D1} = I_{D2}$

$$I_{D1} = 0.5\mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{OV1}^2 = I_{D2}$$

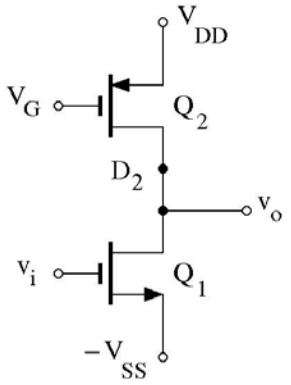
$$V_{OV1} = \left(\frac{\mu_p C_{ox}(W/L)_2}{\mu_n C_{ox}(W/L)_1}\right)^{1/2} V_{OV2}$$

Bias point of CS amp with current mirror

- Include Channel Width Modulation,
  - Lengthy Analysis (see Exercise 3 of Problem set)
  - Gives V_{DS1} and V_{DS2}
  - We can gain insight with load-line analysis

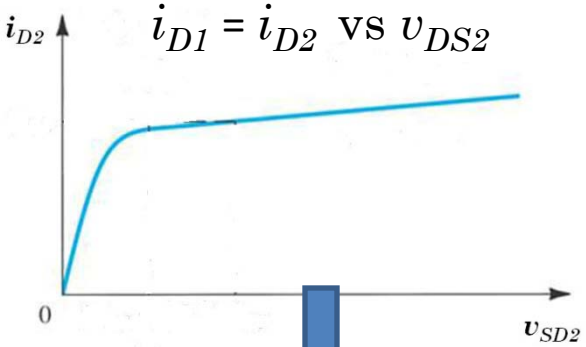


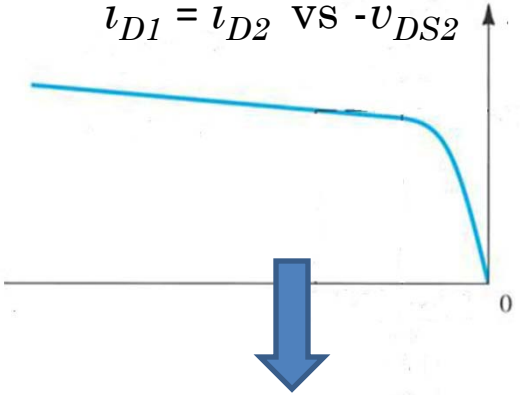
Bias point of CS amp with current mirror

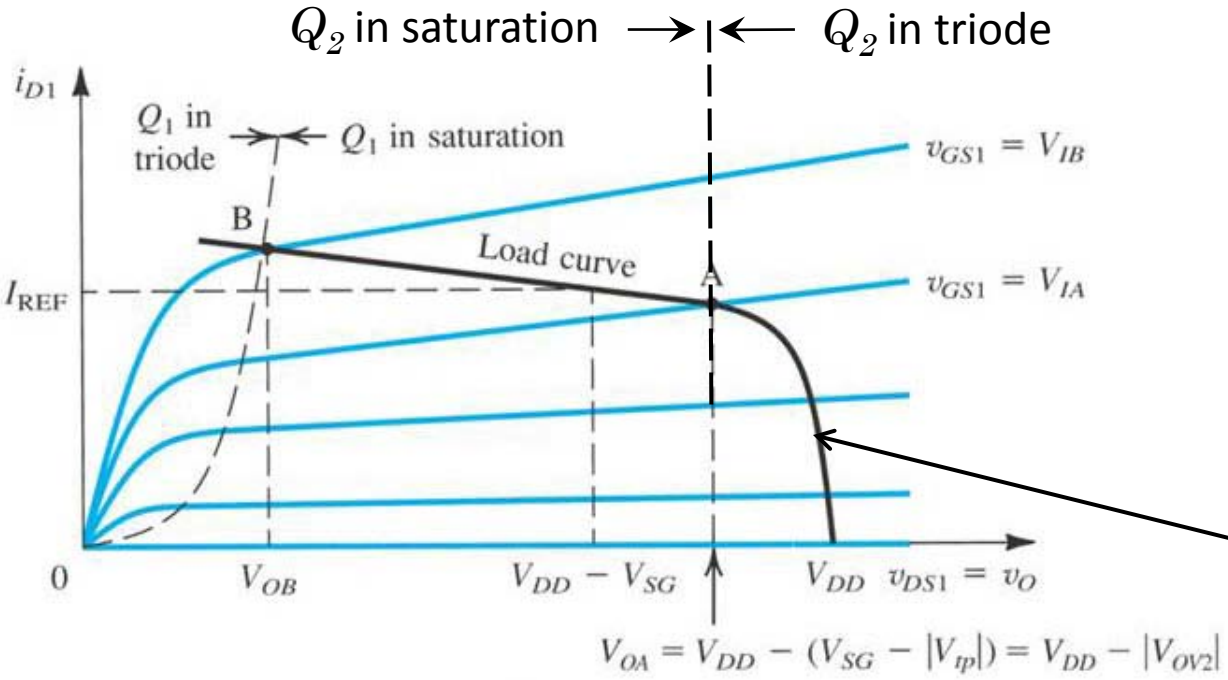


Setting V_{ss} = 0 (For simplicity), the load line (or load curve!) equation for Q1 is $i_{D1} = i_{D2} = f(v_{DS1})$

Note: $v_{DS1} = V_{DD} - v_{DS2}$



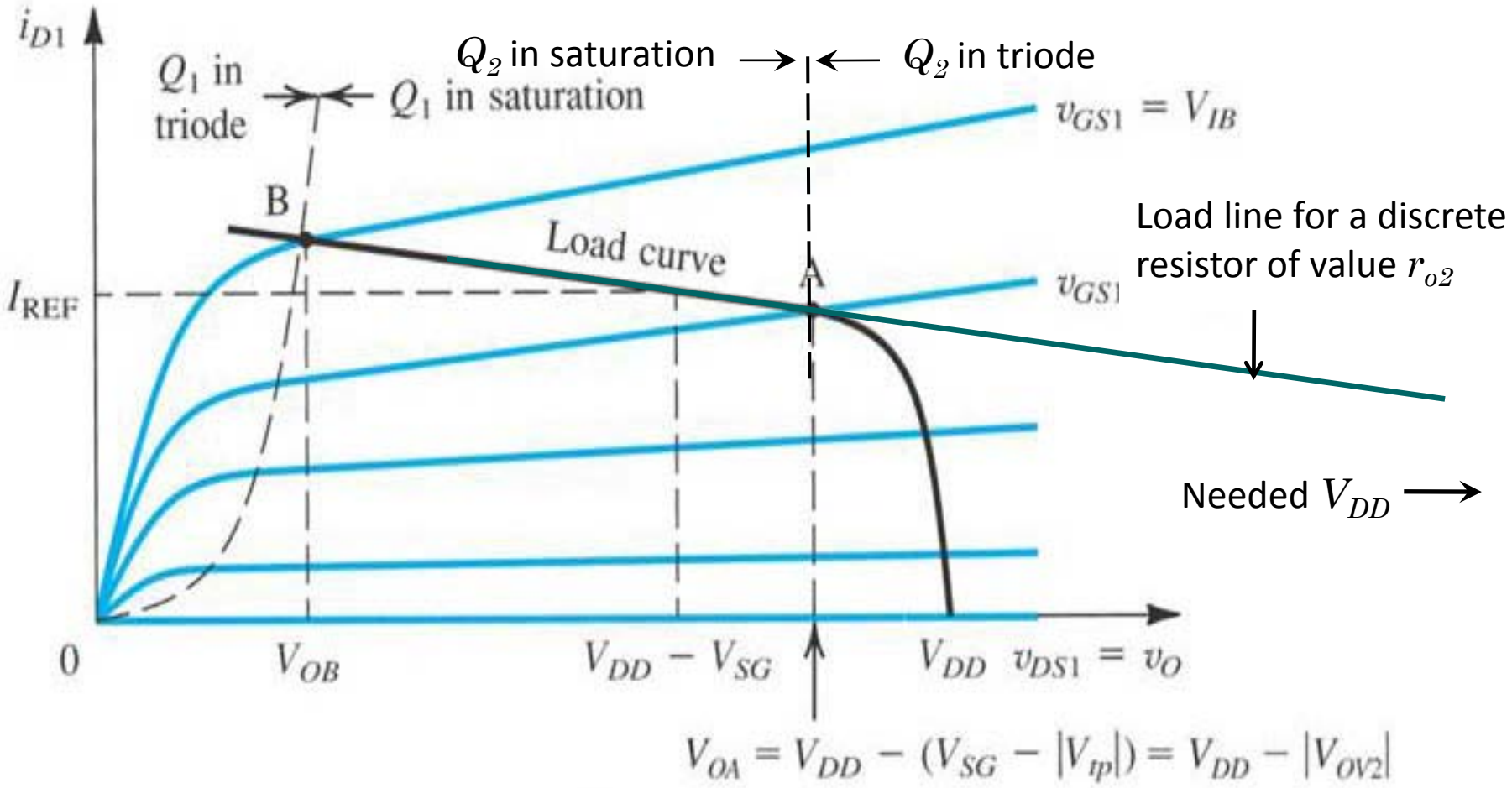




$i_{D1} = i_{D2}$ vs $V_{DD} - v_{DS2}$

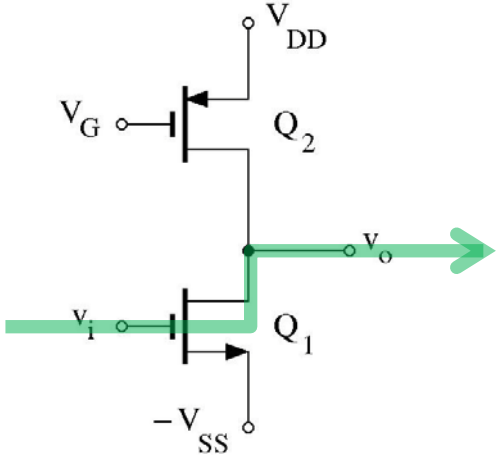
Biasing CS amp with current mirror allows a very large R_D without increasing V_{DD}

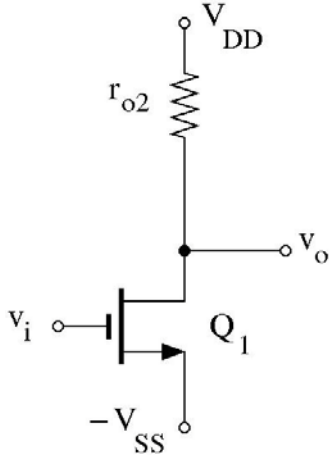
$$A_v = -g_{m1}(r_{o1} \| R_D) = -g_{m1}(r_{o1} \| r_{o2})$$



Basic gain cell (CS configuration) in ICs

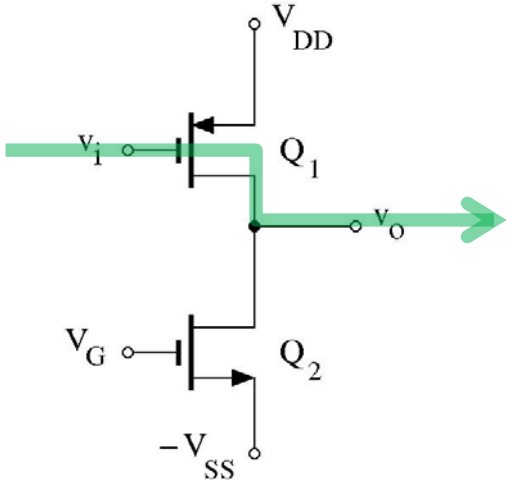
NMOS Version:

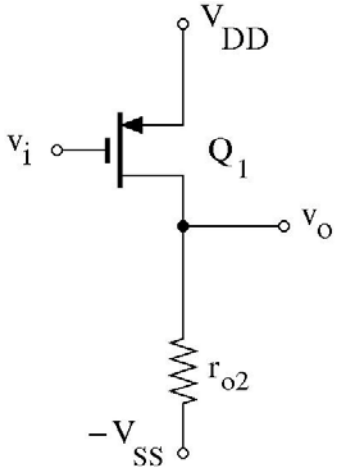




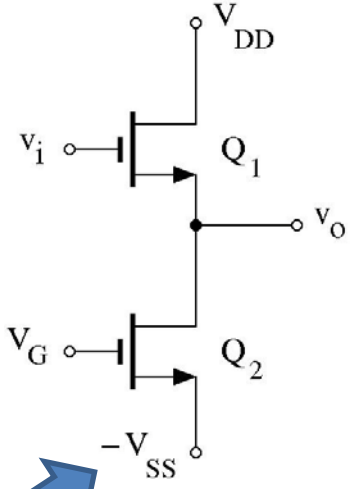
$$A_v = -g_{m1}(r_{o1} \| r_{o2})$$

PMOS Version:

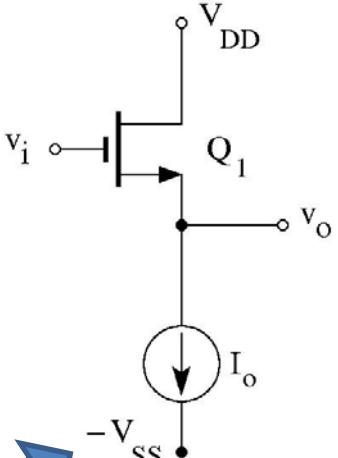




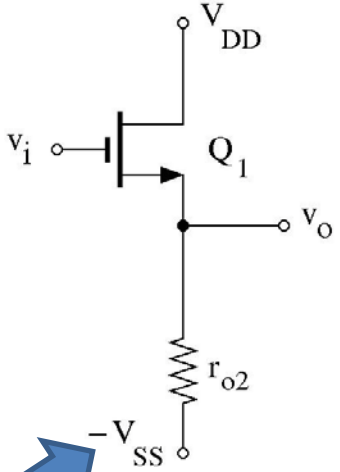
Biasing a Source Follower in ICs



Current mirror



Bias works fine!

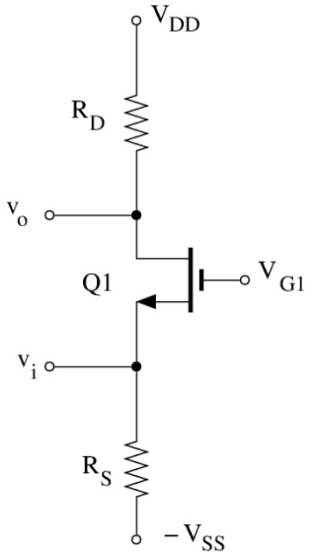


Small signal OK

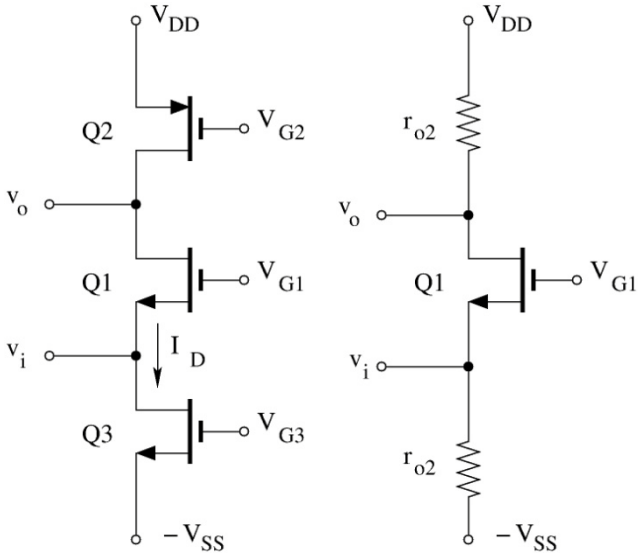
- **Common-Drain (Source Follower) stages are biased with current mirror in the source circuit (as above)**
- **A bias voltage is applied to the gate of Q1 (not shown)!**

Common Gate Amplifiers in ICs

Discrete CG Amp



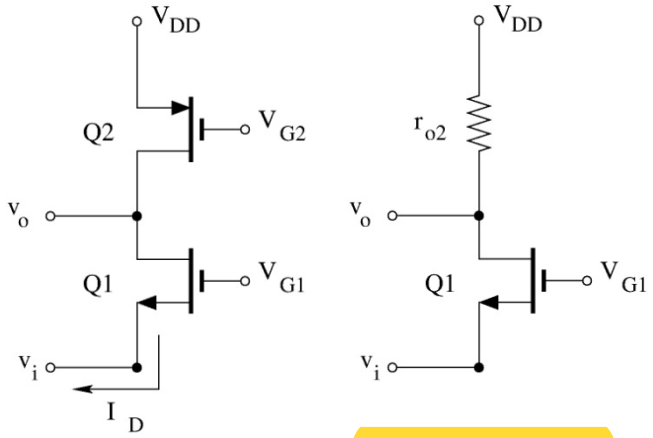
CG Amp with Active Load
(Stand-alone)



Signal circuit

(See Exercise 5 of Problem set)

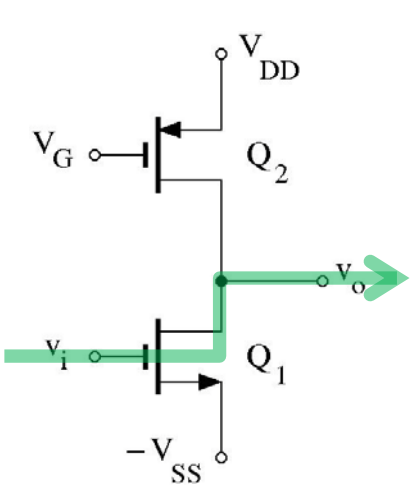
CG Amp with Active Load
(e.g. Cascode Amp.)



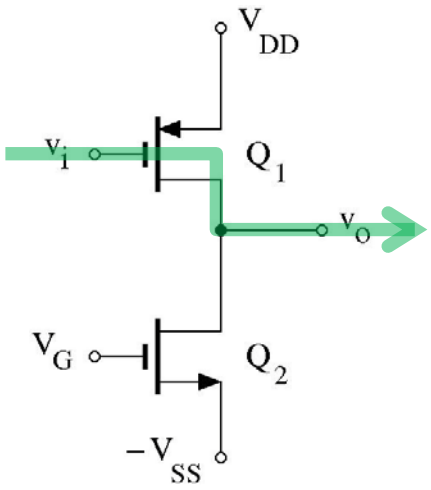
Signal circuit

(See Lecture Set 6)

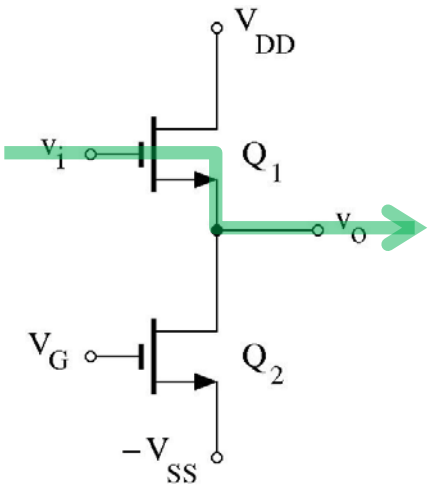
CS and CD MOS amplifiers with active load (Summary)



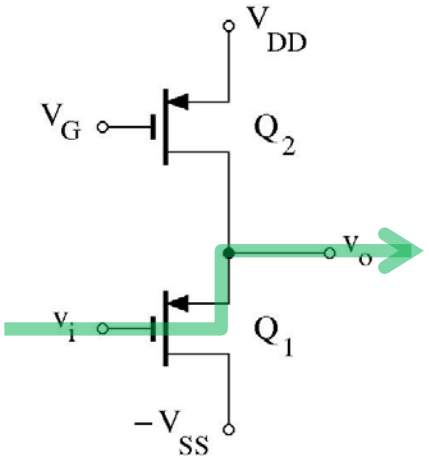
NMOS CS Amp



PMOS CS Amp

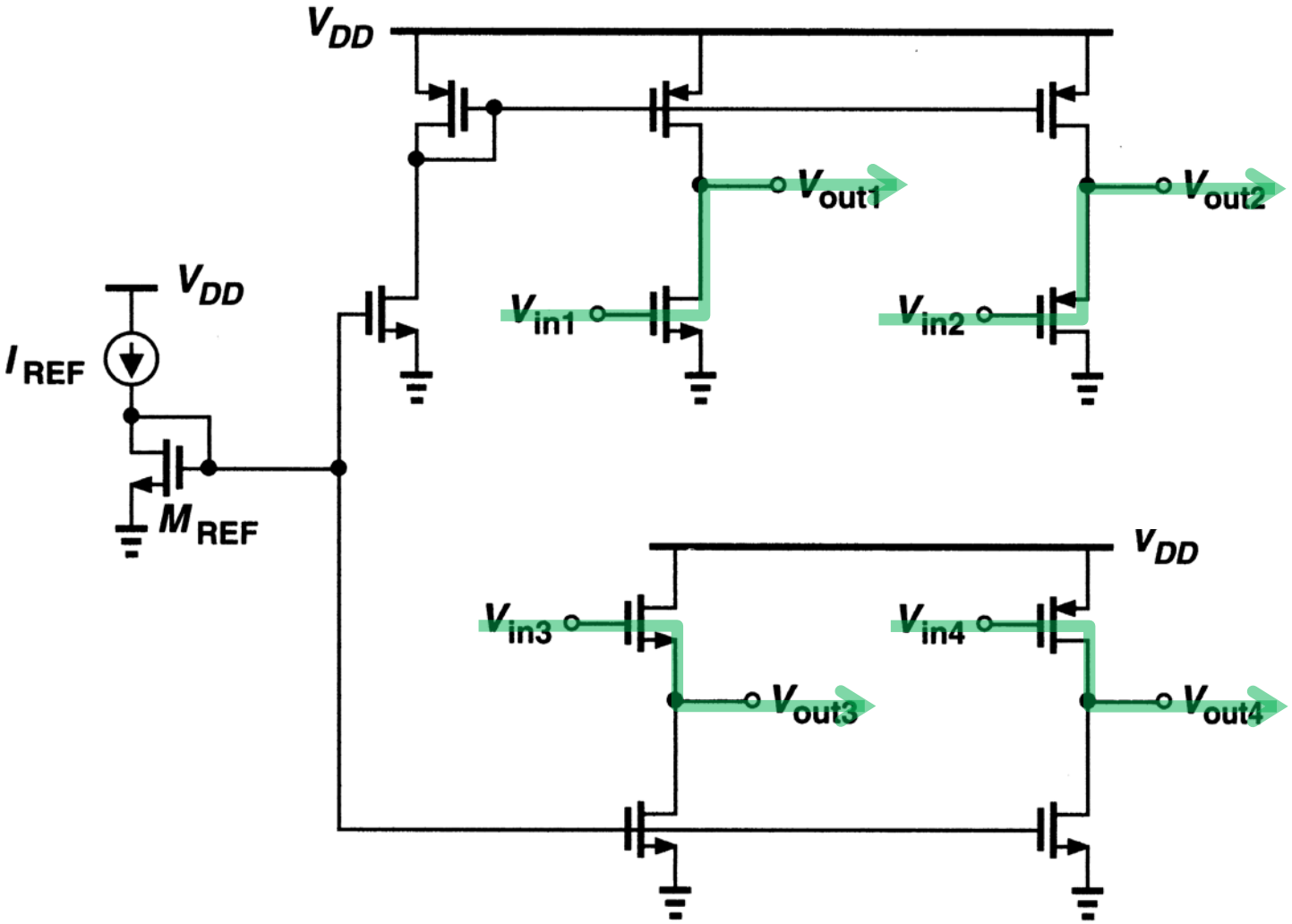


NMOS CD Amp



PMOS CD Amp

Implementation of CS and Follower configurations on IC



Implementation of CS and Follower configurations on IC