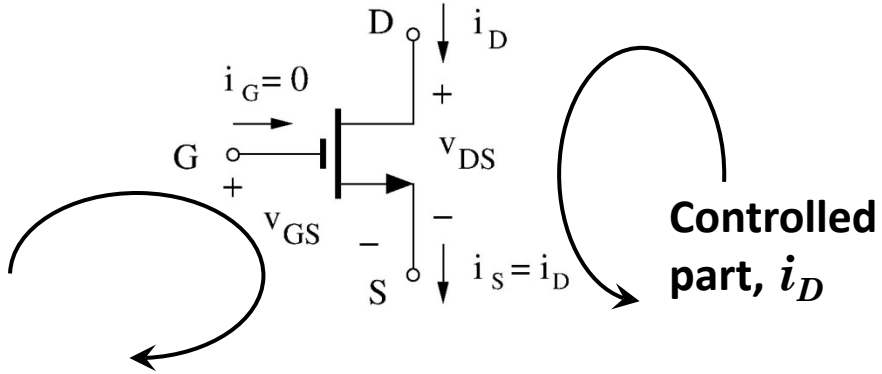
1. MOS: Device Operation and Large Signal Model

Sedra & Smith (6th Ed): Sec. 5.1-5.3
Or Sedra & Smith (5th Ed): Sec. 4.1-4.3
ECE65 Lecture notes: Intro to MOS

Operational Basis of a Field-Effect Transistor (1)

- Transistors acts as valves or gate in which the "main" current flowing through the transistor is controlled by another "small" current or voltage.
- In a Field Effect Transistor, current flowing across the semiconductor is controlled by an electric field perpendicular to the current

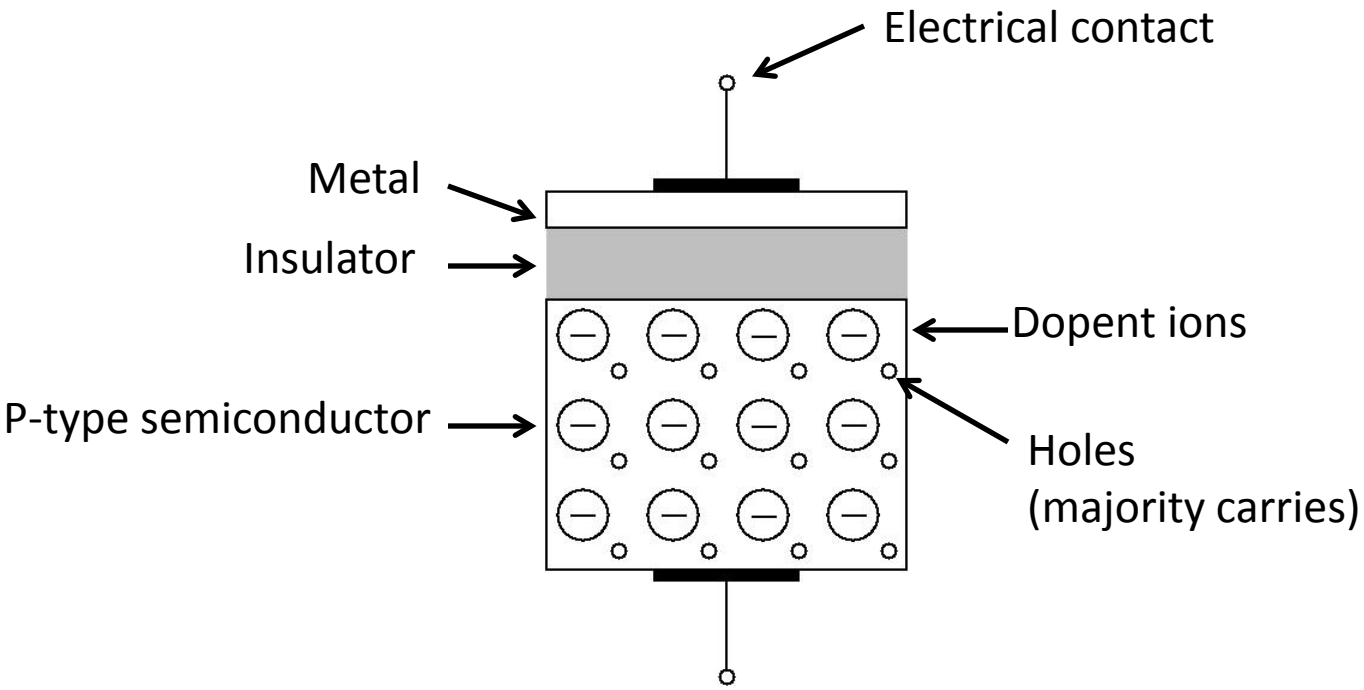


Controller part:
v_{GS} **(or** V_{OV} **)**

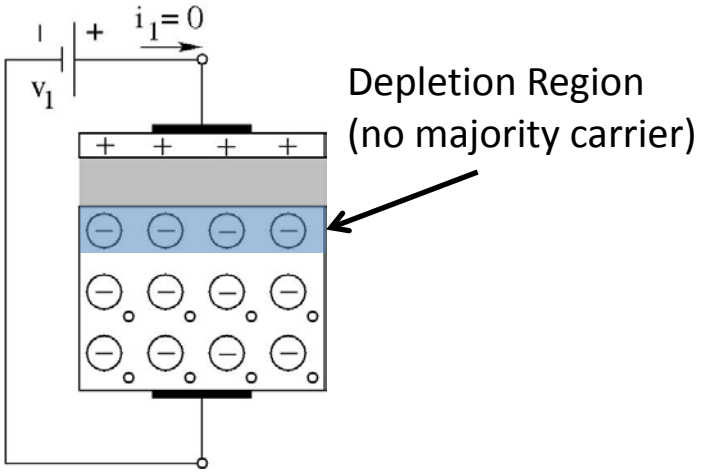
Controlled part, i_D

Operational Basis of a Field-Effect Transistor (2)

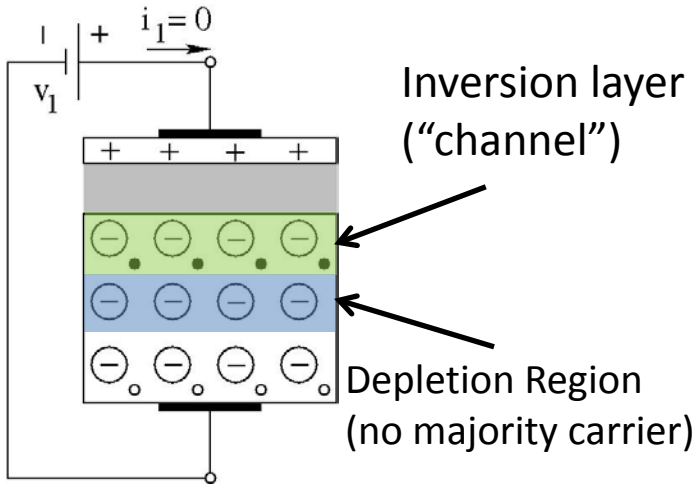
To see how an electric field can control the current flow, consider the **hypothetical** semiconductor below: (constructed similar to a parallel plate capacitor)



Operational Basis of a Field-Effect Transistor (3)



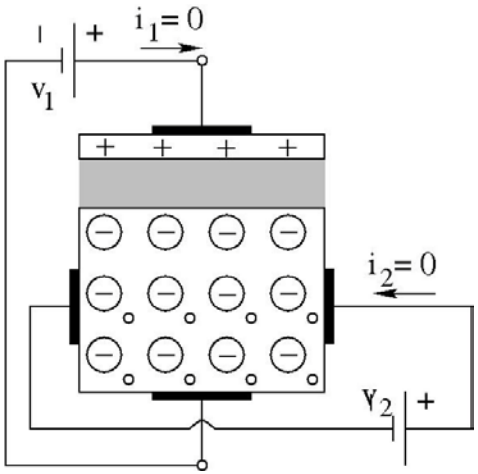
- If we apply a voltage v_1 between electrodes, a charge $Q = C\,v_1$ will appear on each capacitor plate.
  - The electric field is strongest at the interface with the insulator and charge likes to accumulate there.
- Holes are pushed away from the insulator interface forming a "depletion region".
- Depth of depletion region increases with v_1.



- If we increase v_1 above a threshold value (V_t), the electric field is strong enough to "pull" free electrons to the insulator interface. As the holes are repelled in this region, a "channel" is formed which contains electrons in the conduction band ("inversion layer").
- **Inversion layer is a "virtual" n-type material.**

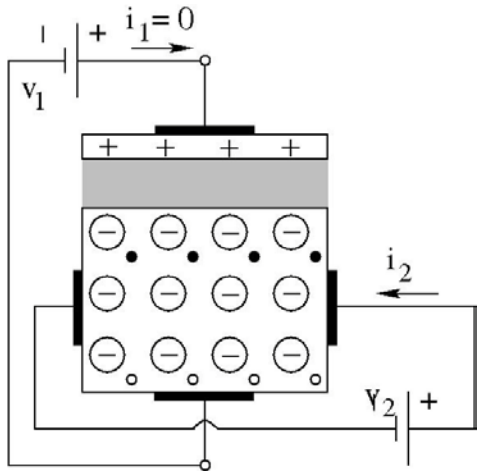
Operational Basis of a Field-Effect Transistor (4)

- We apply a voltage across the p-type semiconductor: (Assume current flows only in the n-type material, ignore current flowing in the p-type semiconductor)



No inversion layer $(v_1 < V_t)$:

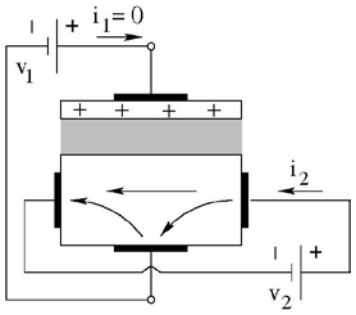
- No current will flow



With inversion layer $(v_1 > V_t)$:

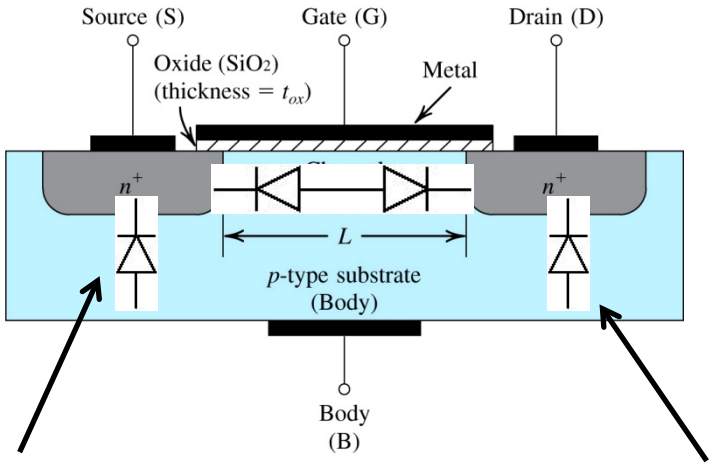
- A current will flow in the channel
- Current will be proportional to electron charge in the channel or $(v_1 - V_t)$
- **Magnitude of Current i_2 is controlled by voltage v_1 (a Transistor!)**

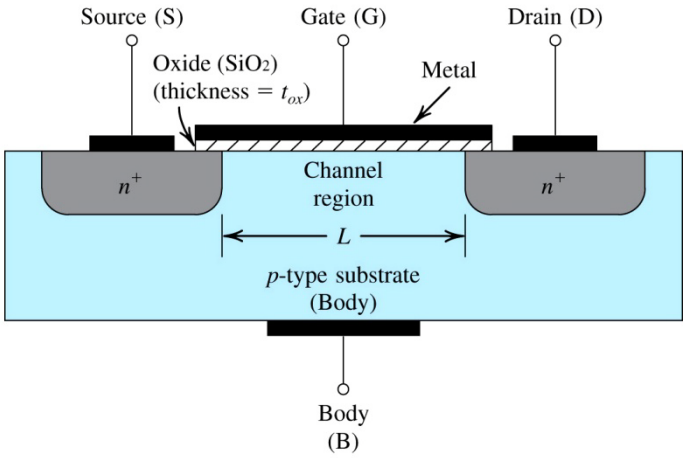
Operational Basis of a Field-Effect Transistor (5)



- We need to eliminate currents flowing in the p-type, i.e., current flows only in the "channel" which is a virtual n-type.

- Make the terminals of n-type material (set up diodes between terminals & p-type "body")
- Heavy doping of the n-type terminals provides a source of free electrons for the channel.
- Make insulator layer as thin as possible to increase the electric field.

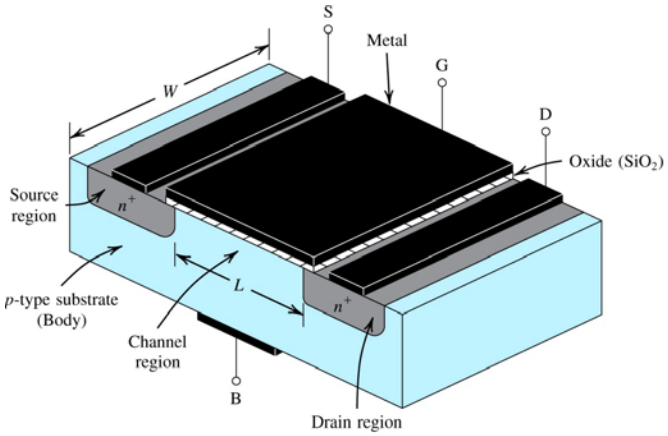




- Body-source and body-drain junctions should always be in reverse bias for FET to work!

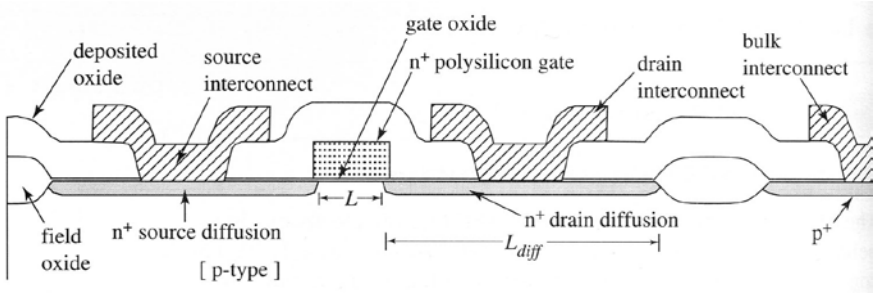
Channel width (L) is the smallest feature on the chip surface

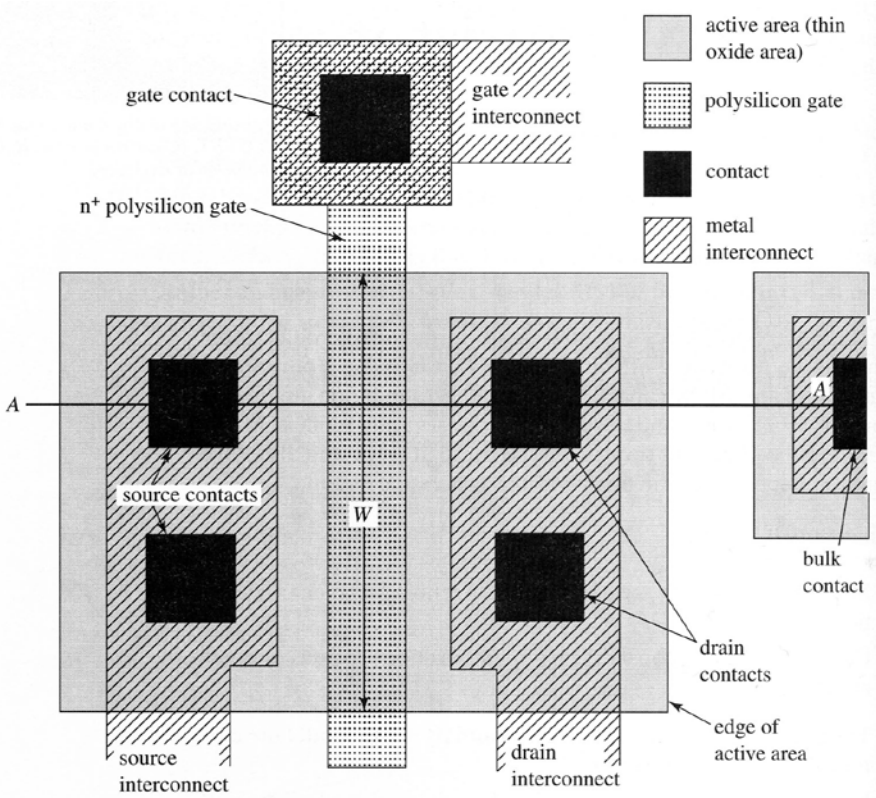
MOSFET "cartoons" for deriving MOSFET characteristics



MOSFET (or MOS): Metal-oxide field effect transistor
NMOS: n-channel enhancement MOS

MOSFET implementation on a chip





NMOS i-v Characteristics (1)

- To ensure that body-source and body-drain junctions are reversed bias, we assume that Body and Source are connected to each other and $v_{DS} \geq 0$.
  - *We will re-examine this assumption later*

- Without a channel, no current flows ("Cut-off").
- For $v_{GS} > V_{tn}$, a channel is formed. The total charge in the channel is

$$|Q| = CV = C_{ox}WL\,(v_{GS}\text{-}V_{tn})$$

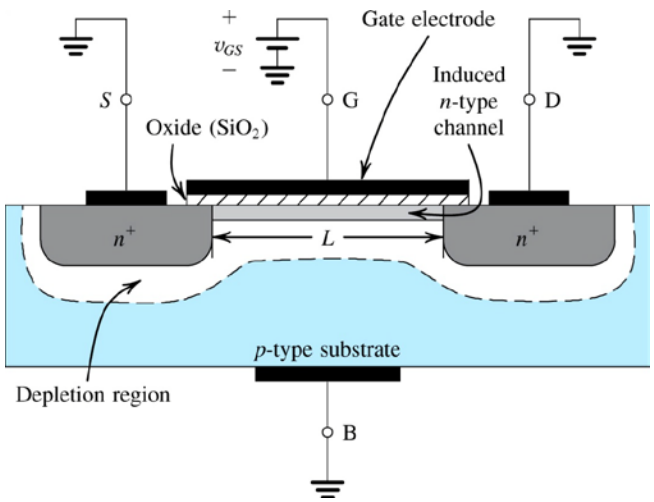
$$C = C_{ox}\,W\,L$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}: \text{ Capacitance per unit area}$$

$$t_{ox}: \text{ Thickness of insulator}$$

$$\varepsilon_{ox}: \text{ permitivity of insulator}$$

$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.45\times10^{-11}\ \text{F/m (for SiO}_2\text{)}$$



NMOS i-v Characteristics (2)

- **We now apply a <u>small</u> voltage v_{DS} between drain and source.**

- <u>A channel is formed when</u> $v_{GS} > V_{tn}$
- Electrons (in the n-channel) move from source to drain with a velocity:

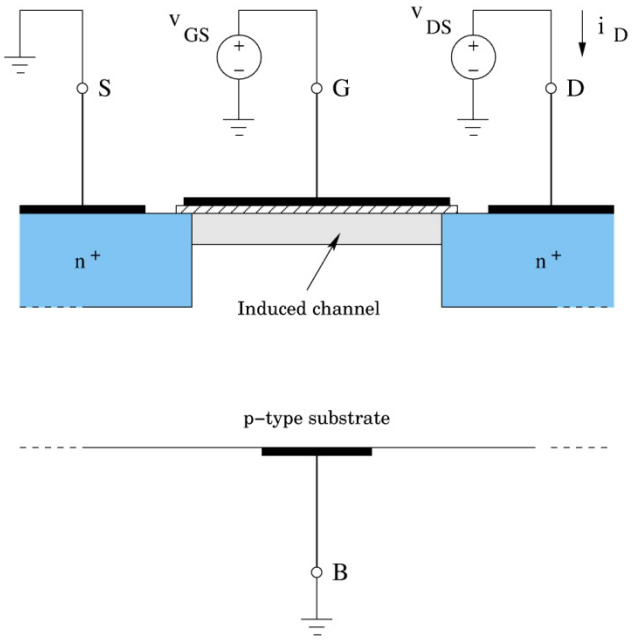
$$v_{drift} = \mu_n |E| = \mu_n \frac{v_{DS}}{L}$$

- The resulting current is

$$i_D = \frac{dq}{dt} = \frac{dQ}{dx} \times \frac{dx}{dt} = \frac{|Q|}{L} \times v_{drift} = \mu_n \frac{|Q|}{L^2} v_{DS}$$

$$|Q| = C_{ox} WL\,(v_{GS} - V_{tn})$$

$$i_D = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_{tn}) v_{DS}$$



Assumes a uniform channel depth which is correct for $v_{DS} << v_{GS} - V_{tn}$

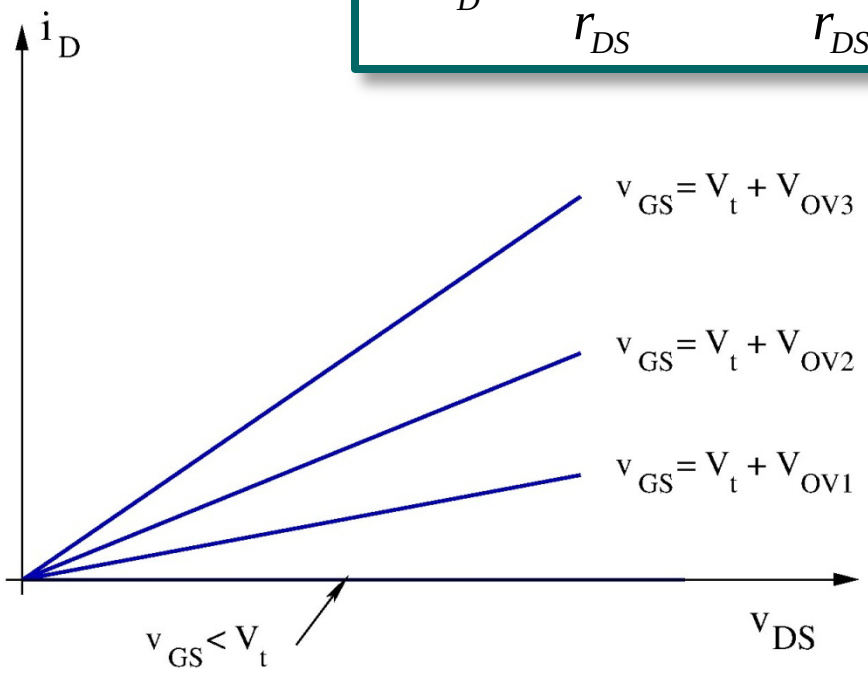
NMOS i-v Characteristics (3)

Overdrive Voltage: $V_{OV} = v_{GS} - V_{tn}$

- When $V_{OV} > 0$ ($v_{GS} > V_{tn}$) and $v_{DS} << V_{OV}$

$$i_D = \mu_n C_{ox} \frac{W}{L} V_{OV} v_{DS}$$

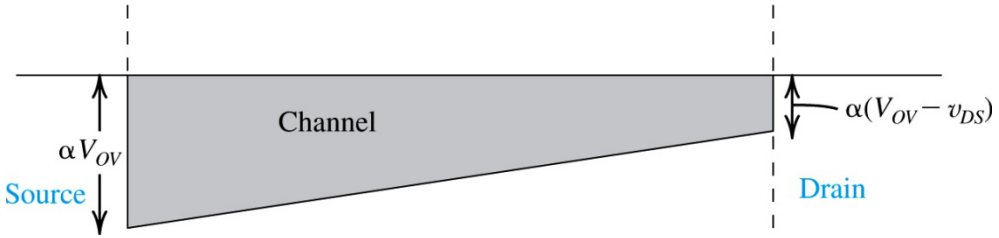
$$i_D = \frac{v_{DS}}{r_{DS}} \text{ with } \frac{1}{r_{DS}} = g_{DS} = \mu_n C_{ox} \frac{W}{L} V_{OV}$$

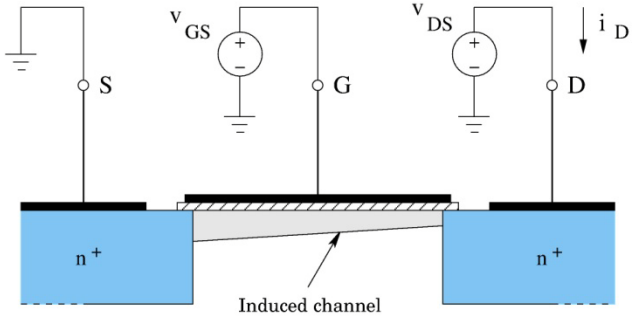


MOS acts as a resistance whose conductivity is controlled by V_{OV} (or v_{GS}).

NMOS i-v Characteristics (4)

- When v_{DS} is increased the channel becomes narrower near the drain (local depth of the channel depends on the difference between V_{OV} and local voltage).



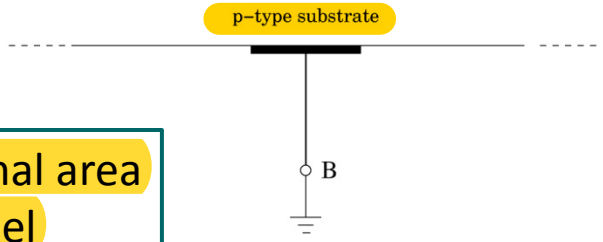


$$i_D = \mu_n \frac{Q}{L^2} v_{DS}$$

$$Q = C_{ox} WL\,(V_{ov} - 0.5 v_{DS})$$

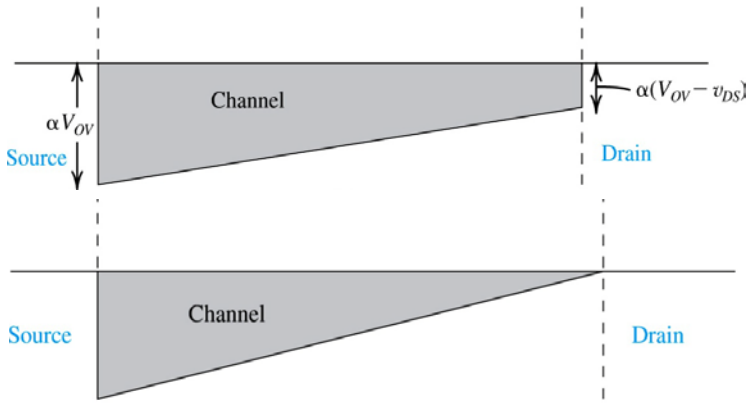
$$i_D = \mu_n C_{ox} \frac{W}{L}\left[V_{OV} v_{DS} - 0.5 v_{DS}^2\right]$$

Cross sectional area of the channel



NMOS i-v Characteristics (5)

- When $v_{DS} = V_{OV}$, the channel depth becomes zero at the drain (Channel is "pinched off").



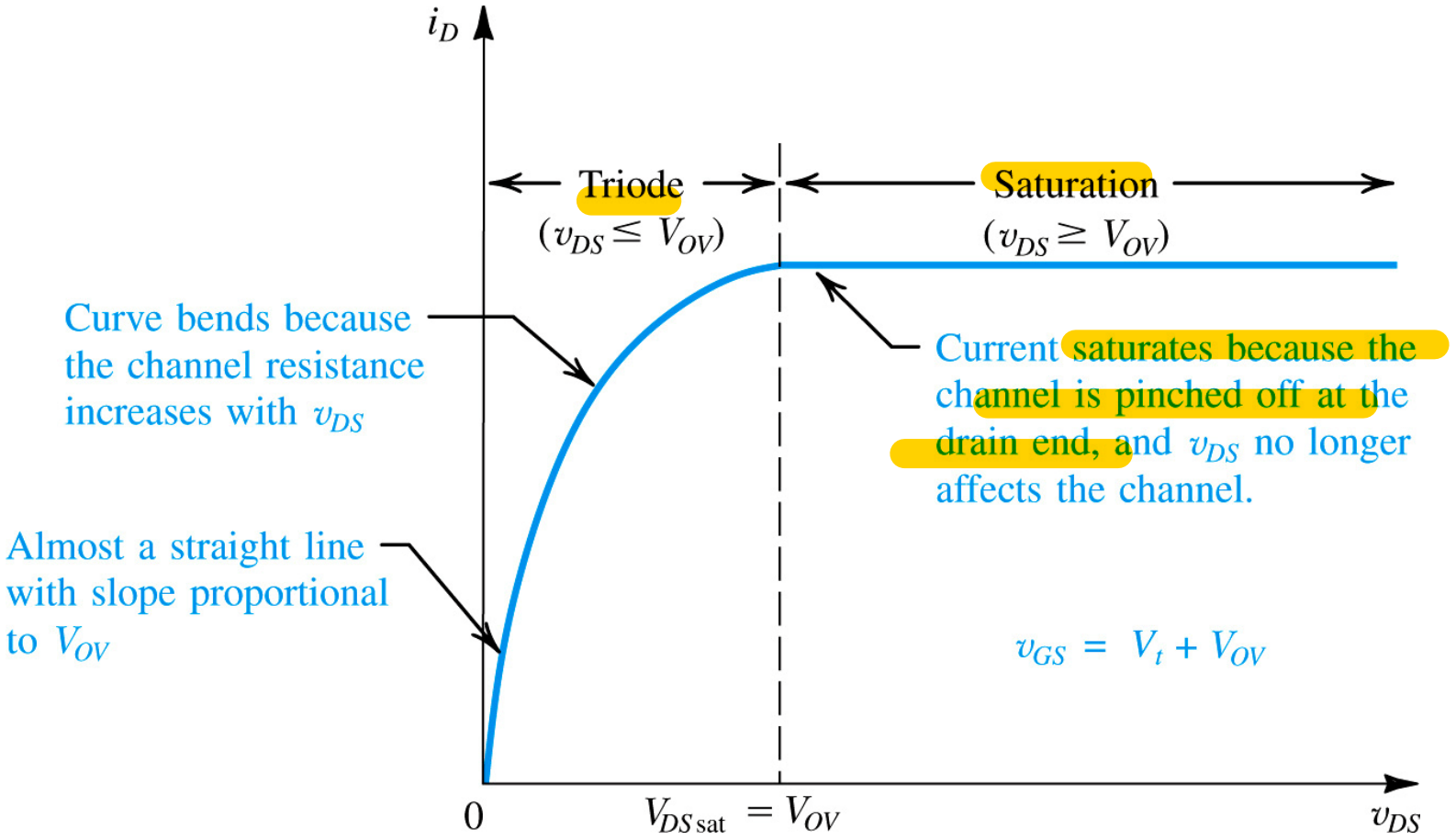
$$i_D = \mu_n C_{ox} \frac{W}{L}\left[V_{OV} v_{DS} - 0.5 v_{DS}^2\right] = \mu_n C_{ox} \frac{W}{L}\left[V_{OV} V_{OV} - 0.5 V_{OV}^2\right]$$

$$i_D = 0.5 \mu_n C_{ox} \frac{W}{L} V_{OV}^2$$

- When v_{DS} is increased further, $v_{DS} > V_{OV}$, the location of channel pinch-off remains close to the drain and i_D remains approximately constant.

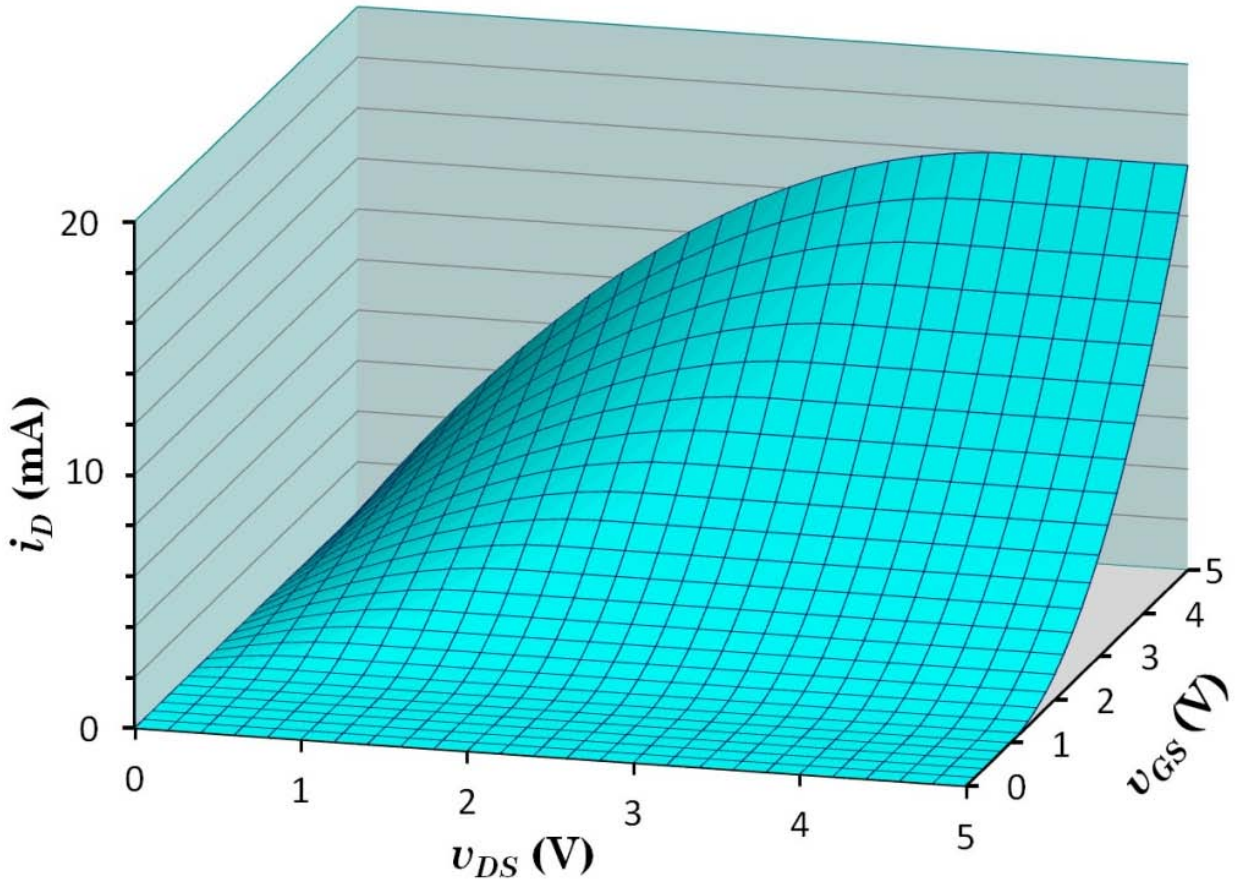
NMOS i-v Characteristics (6)

For a given v_{GS} (or V_{OV})



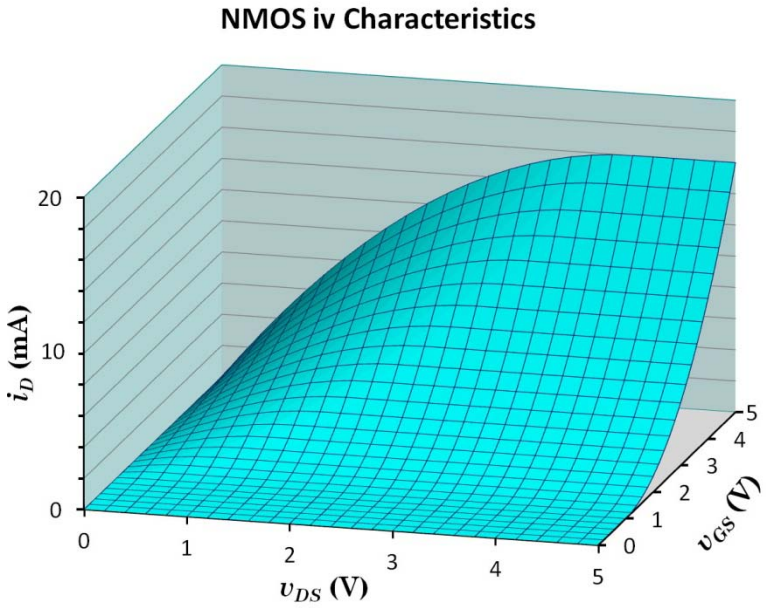
NMOS i-v Characteristics Plot (1)

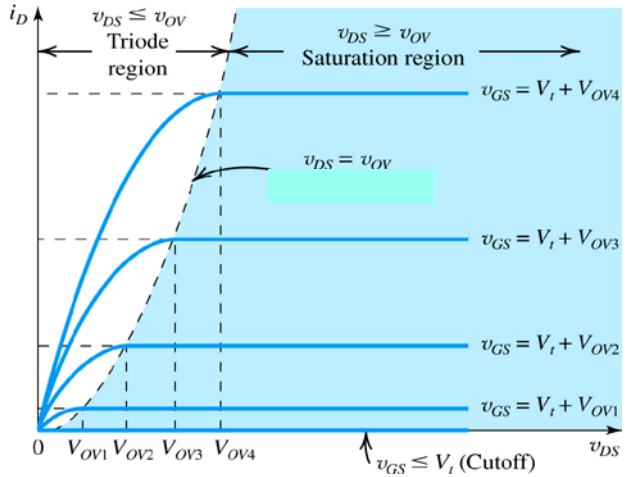
- NMOS i-v characteristics $i_D = f(v_{GS}, v_{DS})$ is a surface



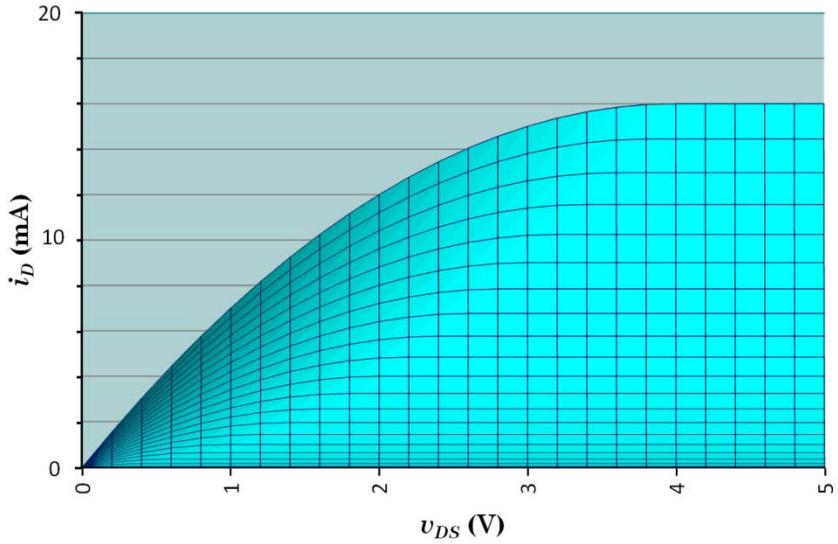
* Plot for $V_{t,n} = 1$ V and $\mu_n C_{ox}\,(W/L) = 2.0$ mA/V^2

NMOS i-v Characteristics Plot (2)



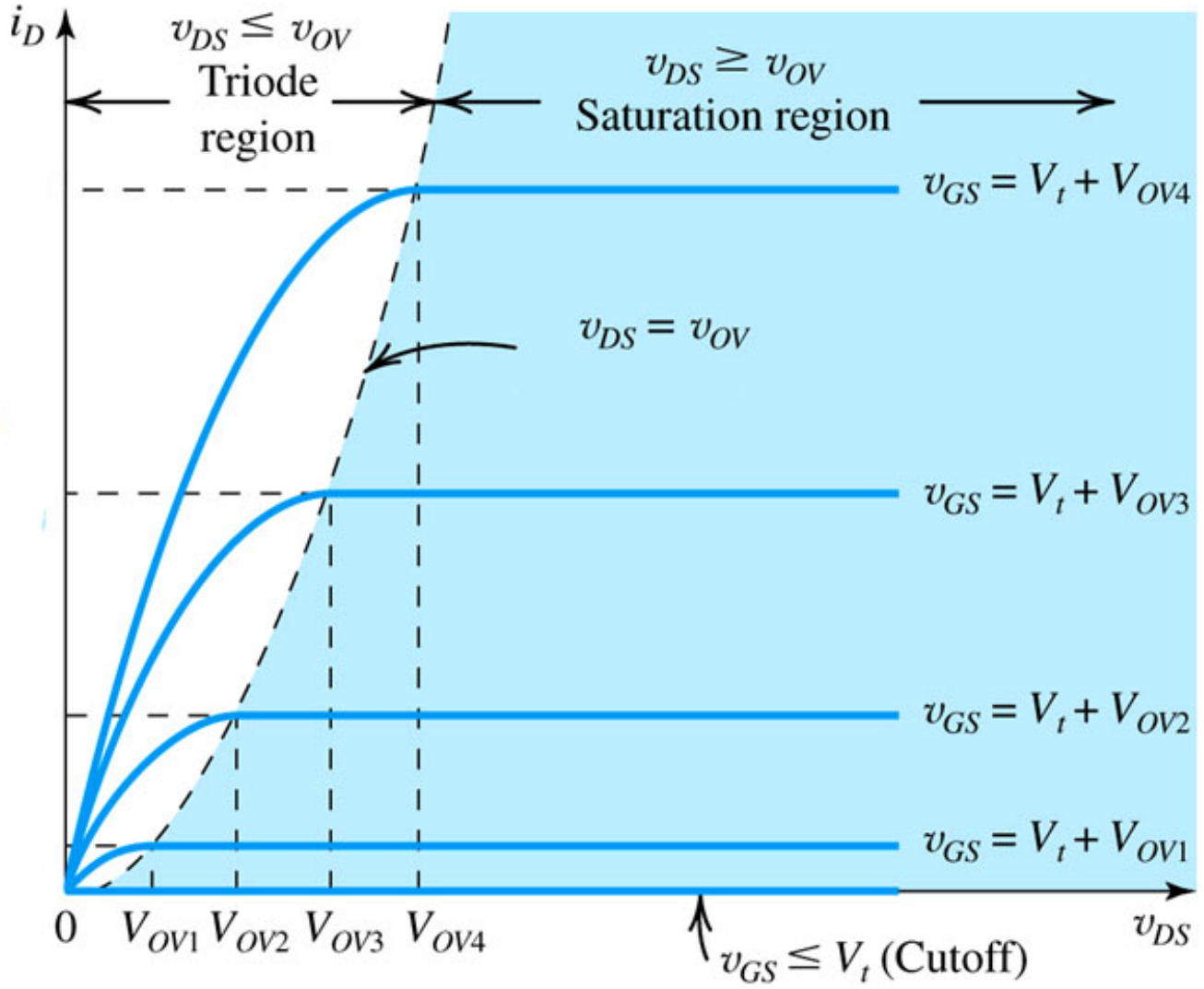


Looking at surface with v_{GS} axis pointing out of the paper*



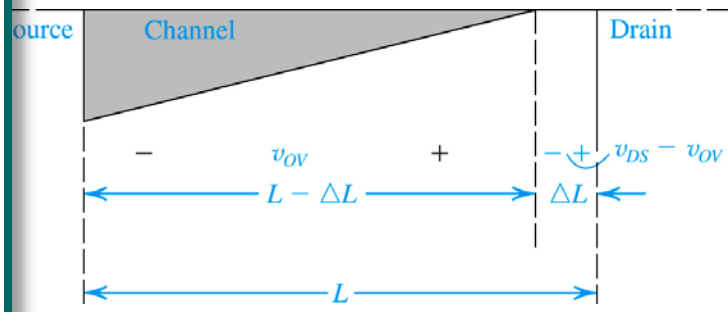
*Note: surface is truncated (i.e., $v_{GS} < 5$ V)

NMOS i-v Characteristics Plot (3)



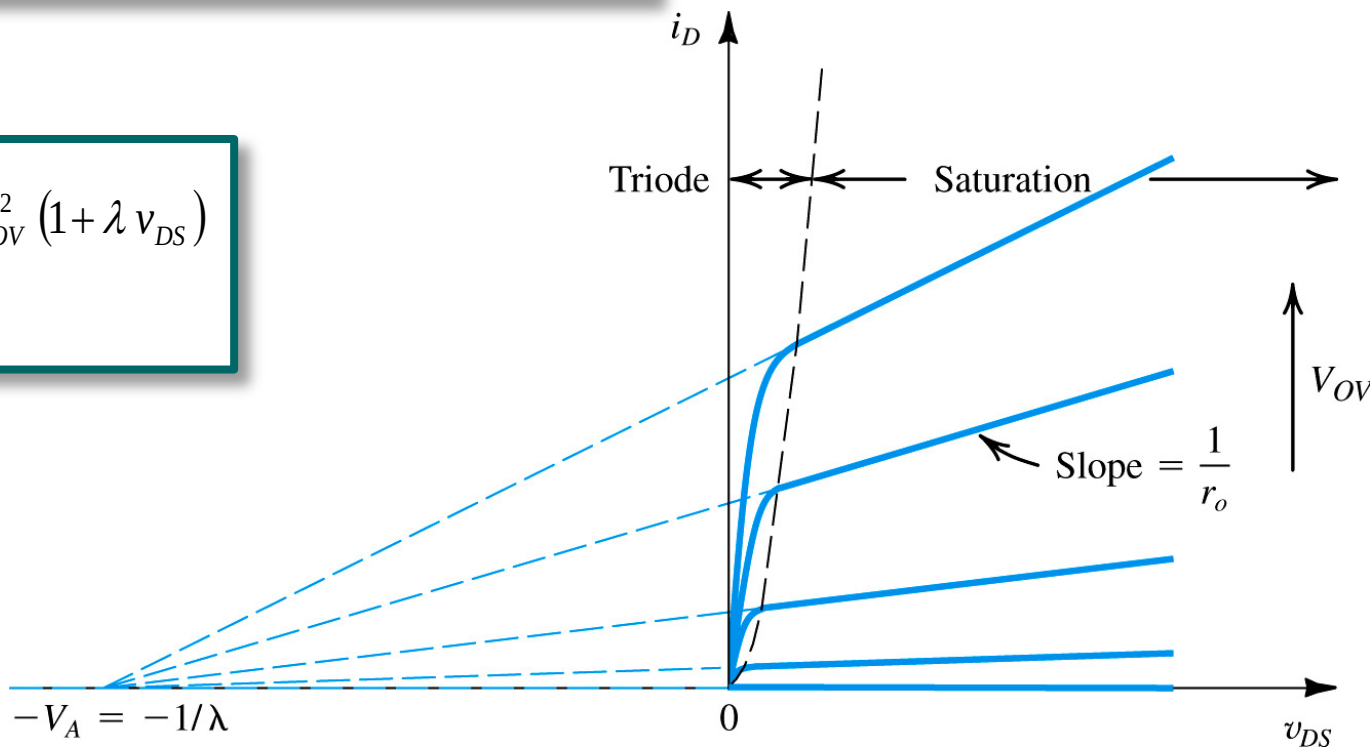
Channel-Width Modulation

- The expression we derived for saturation region assumed that the pinch-off point remains at the drain and thus i_D remains constant.
- In reality, the pinch-off point moves "slightly" away from the drain: Channel-width Modulation



$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2\left(1+\lambda v_{DS}\right)$$

$$\lambda = 1/V_A$$



Body Effect

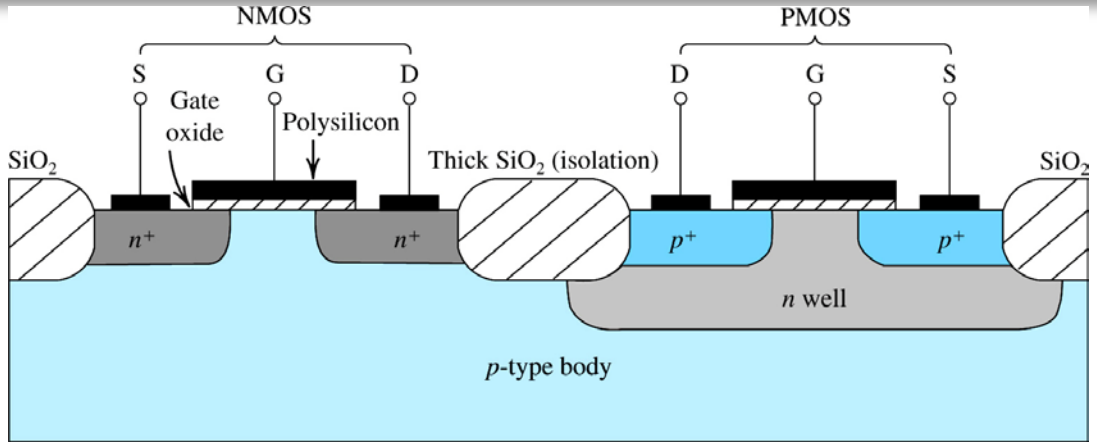
- Recall that Drain-Body and Source-Body diodes should be reversed biased.
  - We assumed that Source is connected to the body ($v_{SB} = 0$) and $v_{DS} = v_{DB} > 0$
- In a chip (same body for all NMOS), it is impossible to connect all sources to the body (all NMOS sources are connected together.
- Thus, the body (for NMOS) is connected to the largest negative voltage (negative terminal of the power supply).
- Doing so, changes the threshold voltage (called "Body Effect")

$$V_{tn} = V_{tn,0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

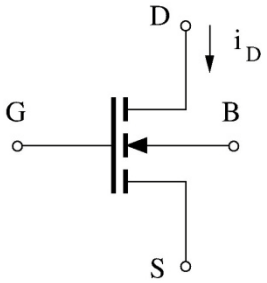
- **In this course we will ignore body effect as well as other second-order effects such as velocity saturation.**

P-channel Enhancement MOS (PMOS)

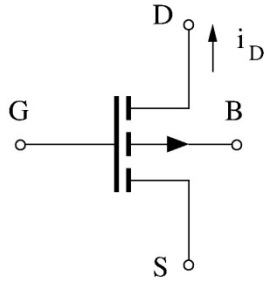
- A PMOS can be constructed analogous to an NMOS: (n-type body), heavily doped p-type source and drain.
- A virtual "p-type" channel is formed in a P-MOS (holes are carriers in the channel) by applying a negative v_{GS}.
- i-v characteristic equations of a PMOS is similar to the NMOS with the exception:
  - Voltages are negative (we switch the terminals to have positive voltages: use v_{SG} instead of v_{GS}).
  - Use mobility of holes, μ_p , instead of μ_n in the expression for i_D



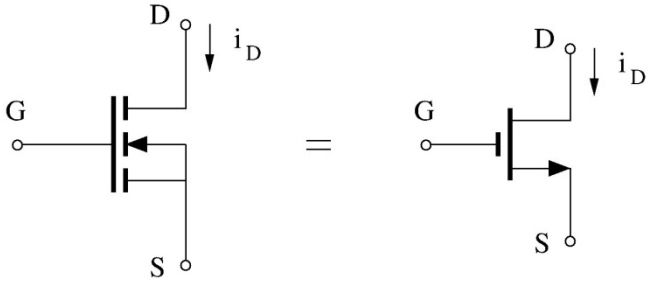
MOS Circuit symbols and conventions

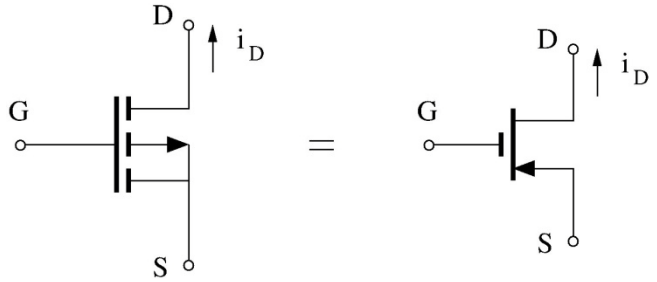


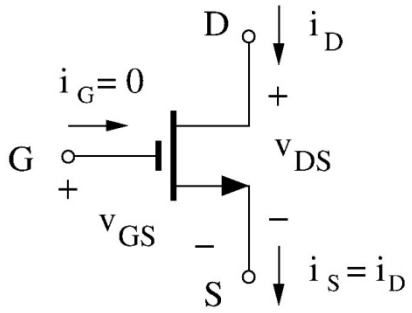
NMOS

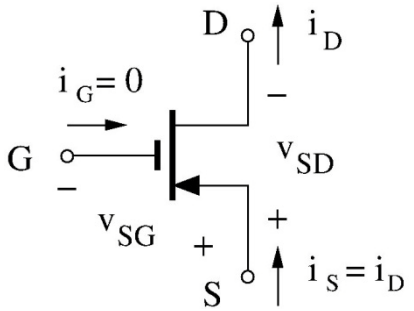


PMOS









MOS i-v Characteristics Equations

NMOS $(V_{OV} = v_{GS} - V_{tn})$

Cut-Off :	$V_{OV} \le 0$	$i_D = 0$
Triode :	$V_{OV} \ge 0$ and $v_{DS} \le V_{OV}$	$i_D = 0.5\mu_n C_{ox} \frac{W}{L}\left[2V_{OV}v_{DS} - v_{DS}^2\right]$
Saturation :	$V_{OV} \ge 0$ and $v_{DS} \ge V_{OV}$	$i_D = 0.5\mu_n C_{ox} \frac{W}{L} V_{OV}^2 \left[1 + \lambda v_{DS}\right]$

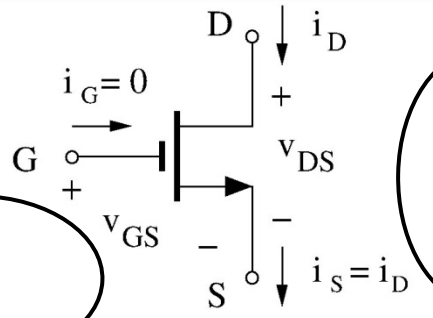
PMOS $(V_{OV} = v_{SG} - \mid V_{t,p} \mid)$*

Cut-Off :	$V_{OV} \le 0$	$i_D = 0$
Triode :	$V_{OV} \ge 0$ and $v_{SD} \le V_{OV}$	$i_D = 0.5\mu_p C_{ox} \frac{W}{L}\left[2V_{OV}v_{SD} - v_{SD}^2\right]$
Saturation :	$V_{OV} \ge 0$ and $v_{SD} \ge V_{OV}$	$i_D = 0.5\mu_p C_{ox} \frac{W}{L} V_{OV}^2 \left[1 + \lambda v_{SD}\right]$

*Note: S&S defines $\mid V_{OV} \mid = v_{SG} - \mid V_{tp} \mid$ and uses $\mid V_{OV} \mid$ in the PMOS formulas.

To Solve MOS Circuit: (with Large Signal Model)

1. **Hypothesis:** assume one of the modes of operation for the MOSFET
2. **Solve:** Use the equations for the selected mode to solve the circuit
3. **Check:** at the end perform the check for the selected mode to verify the hypothesis
4. **Redo:** if the hypothesis check fails, try another hypothesis and start over



Controller part:
Circuit connected to GS sets v_{GS} (or V_{OV})

Controlled part:
i_D & v_{DS} are set by transistor state (& outside circuit)