CSE 4207 CT 4 Assignment
Roll No: 1603014

Assignment Problem:
Category: A
Word Size = 7 bits
ALU Operations = OR XOR AND ((A or B), SHR

Solution:
Video:

Have you uploaded the video?	YES/NO
Check List 1: Have you explained the design using testbenches to prove that your circuit is working correctly and giving correct results?	YES
Check List 2: Have you shown full synthesis results showing all the required info including RTL Synthesis, RTL Floorplan, RTL Power Analysis, GDS and Heatmap (for details, see assignment template doc)?	YES
NB: Failing to upload video will cause heavy point penalty (5-6 Marks)	
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

HDL Code:

Check List: Have you added all the modules written in verilog including ALU, ALU_OP1, ALU_OP2, CONTROLLER, TOP, TOP_TESTBENCH, ALU_TESTBENCH, CONTROLLER_TESTBENCH?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

`top.v`

```
module TOP #(parameter WIDTH = 8)(
    input [WIDTH-1:0] A,
    input [WIDTH-1:0] B,
    input [4:0] opcode,
    output [WIDTH-1:0] result
);

    wire [4:0] alu_op;

    Controller ctrl (
        .opcode(opcode),
        .alu_op(alu_op)
    );
```

```
    ALU #(WIDTH) alu_unit (
        .A(A),
        .B(B),
        .opcode(alu_op),
        .Y(result)
    );

endmodule
```

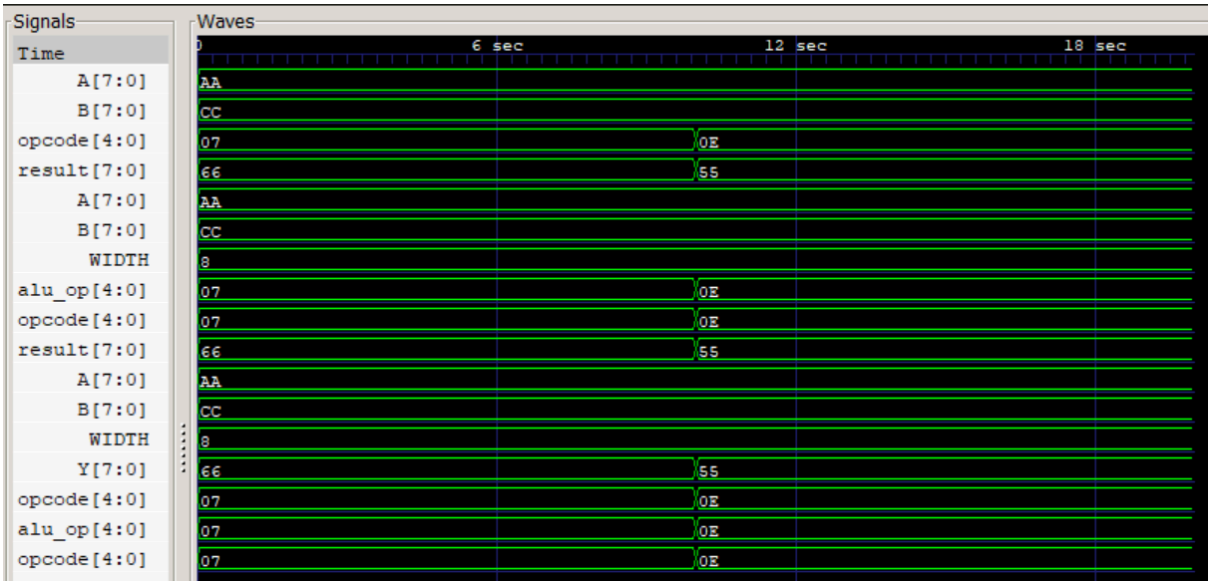
controller.v

```
module Controller (
    input [4:0] opcode,
    output reg [4:0] alu_op
);
    always @(*) begin
        case (opcode)
            5'd7:  alu_op = 5'd7;   // OR XOR AND
            5'd14: alu_op = 5'd14;  // SHR
            default: alu_op = 5'd31; // Invalid opcode
placeholder
        endcase
    end
endmodule
```

RTL Timing Diagram:

Check List: Have you added all the timing diagrams of ALU_TESTBENCH, CONTROLLER_TESTBENCH, TOP_TESTBENCH?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

top_tb.v



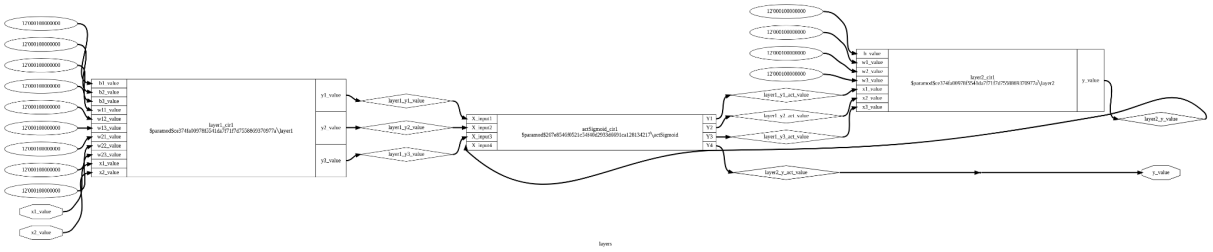
RTL Synthesis (130nm Skywater PDK with OpenLane toolchain):

Check List: Have you added *RTL synthesis summary*, *RTL synthesized design figure* and *Standard cell usage in synthesized design*?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

RTL synthesis summary

Metric	Count
Number of wires	1367
Number of wire bits	1400
Number of public wires	3
Number of public wire bits	36
Number of ports	3
Number of port bits	36
Number of memories	0
Number of memory bits	0
Number of processes	0
Number of cells	1376

RTL synthesized design figure



Standard cell usage in synthesized design

Cell Name	Count	Cell Name	Count
sky130_fd_sc_hd__a2111o_2	9	sky130_fd_sc_hd__a2111oi_2	4
sky130_fd_sc_hd__a2111oi_4	1	sky130_fd_sc_hd__a211o_2	50
sky130_fd_sc_hd__a211oi_2	10	sky130_fd_sc_hd__a21bo_2	6
sky130_fd_sc_hd__a21boi_2	1	sky130_fd_sc_hd__a21o_2	59
sky130_fd_sc_hd__a21oi_2	69	sky130_fd_sc_hd__a21oi_4	2
sky130_fd_sc_hd__a221o_2	8	sky130_fd_sc_hd__a221oi_2	5
sky130_fd_sc_hd__a22o_2	20	sky130_fd_sc_hd__a22oi_2	2
sky130_fd_sc_hd__a22oi_4	1	sky130_fd_sc_hd__a2bb2o_2	4
sky130_fd_sc_hd__a311o_2	14	sky130_fd_sc_hd__a311oi_2	1
sky130_fd_sc_hd__a311oi_4	1	sky130_fd_sc_hd__a31o_2	43
sky130_fd_sc_hd__a31oi_2	7	sky130_fd_sc_hd__a31oi_4	2
sky130_fd_sc_hd__a32o_2	8	sky130_fd_sc_hd__a32oi_2	1
sky130_fd_sc_hd__a41o_2	2	sky130_fd_sc_hd__and2_2	27
sky130_fd_sc_hd__and2_4	1	sky130_fd_sc_hd__and2b_2	6
sky130_fd_sc_hd__and3_2	38	sky130_fd_sc_hd__and3_4	4
sky130_fd_sc_hd__and3b_2	6	sky130_fd_sc_hd__and4_2	11
sky130_fd_sc_hd__and4b_2	3	sky130_fd_sc_hd__and4bb_2	1
sky130_fd_sc_hd__buf_1	59	sky130_fd_sc_hd__buf_2	51
sky130_fd_sc_hd__buf_4	6	sky130_fd_sc_hd__buf_6	4
sky130_fd_sc_hd__conb_1	5	sky130_fd_sc_hd__inv_2	22
sky130_fd_sc_hd__mux2_2	31	sky130_fd_sc_hd__mux2_4	2
sky130_fd_sc_hd__mux4_2	1	sky130_fd_sc_hd__nand2_2	132
sky130_fd_sc_hd__nand3_2	8	sky130_fd_sc_hd__nand3b_2	1
sky130_fd_sc_hd__nand4_2	2	sky130_fd_sc_hd__nor2_2	134
sky130_fd_sc_hd__nor3_2	1	sky130_fd_sc_hd__nor4_2	1
sky130_fd_sc_hd__o2111a_2	9	sky130_fd_sc_hd__o2111ai_2	6
sky130_fd_sc_hd__o211a_2	53	sky130_fd_sc_hd__o211a_4	1
sky130_fd_sc_hd__o211ai_2	14	sky130_fd_sc_hd__o211ai_4	3
sky130_fd_sc_hd__o21a_2	40	sky130_fd_sc_hd__o21ai_2	46
sky130_fd_sc_hd__o21ba_2	9	sky130_fd_sc_hd__o21bai_2	2
sky130_fd_sc_hd__o221a_2	18	sky130_fd_sc_hd__o221ai_2	3
sky130_fd_sc_hd__o22a_2	24	sky130_fd_sc_hd__o22ai_2	1
sky130_fd_sc_hd__o2bb2a_2	3	sky130_fd_sc_hd__o311a_2	21
sky130_fd_sc_hd__o311a_4	1	sky130_fd_sc_hd__o311ai_2	2
sky130_fd_sc_hd__o311ai_4	1	sky130_fd_sc_hd__o31a_2	19
sky130_fd_sc_hd__o31ai_2	5	sky130_fd_sc_hd__o32a_2	9
sky130_fd_sc_hd__o32ai_2	4	sky130_fd_sc_hd__o41a_2	6
sky130_fd_sc_hd__or2_2	47	sky130_fd_sc_hd__or2_4	5
sky130_fd_sc_hd__or3_2	38	sky130_fd_sc_hd__or3_4	6
sky130_fd_sc_hd__or3b_2	14	sky130_fd_sc_hd__or3b_4	2
sky130_fd_sc_hd__or4_2	16	sky130_fd_sc_hd__or4_4	8
sky130_fd_sc_hd__or4b_2	6	sky130_fd_sc_hd__or4b_4	3
sky130_fd_sc_hd__or4bb_4	1	sky130_fd_sc_hd__xnor2_2	34
sky130_fd_sc_hd__xnor2_4	2	sky130_fd_sc_hd__xor2_2	7

RTL Floorplan (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added RTL Floorplan info?	YES

NB: Failing to add any required info will cause point penalty (1-2 Marks)

General RTL Floorplan Information		
Parameter	Value	Unit
Database Units (DBU)	1000	–
Site Size	(0.460, 2.720)	μm
Die Area (BBox)	(0.000, 0.000) to (400.000, 400.000)	μm
Core Area (BBox)	(10.120, 10.880) to (299.920, 299.200)	μm
Core Area	83555.136	μm^2
Placement Utilization	14.925	%

RTL Power Analysis (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added RTL Power Analysis info?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

Group	Internal Power (mW)	Switching Power (mW)	Leakage Power (mW)	Total Power (mW)	Contribution (%)
Sequential	0.0000	0.0000	0.0000	0.0000	0.0%
Combinational	0.9396	1.6073	0.000005	2.5468	100.0%
Clock	−0.00005	0.0000	0.000006	0.000006	0.0%
Macro	0.0000	0.0000	0.0000	0.0000	0.0%
Pad	0.0000	0.0000	0.0000	0.0000	0.0%
Total	0.9396	1.6073	0.000011	2.5468	100.0%

GDS Layout (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added the GDS Layout figure?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

Heatmap (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added the heatmap?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)