# ECE 385

SP 2022

Experiment #1

**Introductory Experiment**

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Your Lab Section/Day & Time Your TA’s Name

## Purpose of Circuit

The purpose of this lab is to introduce us to the ECE 385 lab and equipment. The lab requires us to design a 2 to 1 MUX using NAND gates. Part A of this lab allow us the observe the glitch that causes by the static hazard in the circuit. In part B of this lab, we need to modify our design from part A to create a glitch-free circuit.

## Written Description of Circuit

1. **Circuit Design Process**

A 2-to-1 mux consists of two inputs A and C, one select input B and one output Z. Depending on the select input B, the output Z will be one of the inputs. In this lab, we will design it as when B is 0, output will be connected to C. When B is 1, output will be connected to A.

1. **Pin Assignment**

|  |  |
| --- | --- |
| Pin | Description |
| A | One of the input for 2 to 1 mux |
| B | Select signal for 2 to 1 mux |
| C | One of the input for 2 to 1 mux |
| Z | Output for the 2 to 1 mux |

1. **K-Maps, State Diagrams, Truth Tables, etc.**

Truth Table K-Map (Part A naive design)

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | Z |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BC  A | 00 | 01 | 11 | 10 |
| 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |

1. **Functions**

By using the K-Map, we find that the Boolean expression is Z = B’C + AB. However, we will find later that this design will have glitch. We’ll need to add another term to create the glitch-free expression: Z = B’C + AB + AC.

## Part b: K – map with redundant term AC

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BCA | 00 | 01 | 11 | 10 |
| 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |

## Logic Diagrams (Do we need to put all the labels and pin numbers on?)

Part A in AND-OR form

Diagram

Description automatically generated

Part A in NAND form

Diagram

Description automatically generated

Part B in AND-OR form

Diagram, schematic

Description automatically generated

Part B in NAND form

Diagram, schematic

Description automatically generated

**Component Layout**

**A picture containing diagram

Description automatically generated Part A Bread Board**

**Part A Schematic**

**Diagram

Description automatically generated**

## Part B Bread Board

## Chart Description automatically generated with medium confidence

## Part B Schematic

## Diagram, schematic Description automatically generated

## Answers to Pre-Lab Questions

## Part A Question:

## Not all groups may observe static hazards because the minimal delay is 0 ns, which means there could be no delays (GG.25), or it is so small to observe. According to Prof. Cheng’s video at 13:00, a small capacitor acts as a delay. It can increase the delay of inverter to see the glitch.

## 

## Answers to Lab Questions

## 

## Lab .2 Truth Table

## 

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | Z |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

## Lab .3 Waveform

## Graphical user interface Description automatically generated

## Lab .4 Glitch

## It does response like part A.

## At the falling edge of the input B, we are more likely to observe a glitch at the output. Because in the falling edge of B, there’s an extra inverter for B’C than BA. In the rising edge of B, by the property of NAND gate, the extra inverter will not have effect on the output Z since when we know (BA)’ = 0, Z will be 1. In the falling edge of B, there’s a bigger window for us to observe glitches.

## 

## Graphical user interface Description automatically generated

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | Z |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

## Answers to Post-Lab Questions

1. Timing Diagram

Chart

Description automatically generated

At the falling edge of edge of B, it takes 60ns for Z to stabilize. At the rising edge of B, it takes 40ns for Z to stabilize. There are potential glitches in the output, Z. For example, if (AB)’ is 1 before (B’C)’ goes to 0, then both (AB)’ and (B’C)’ are 1, which will result output Z to be 0 when it supposes to be 1. Same thing will happen in the rising edge of B. However, at the rising edge of B, there’s a shorter window for glitches to occur than the falling edge.

1. Debouncer at GG.34

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Q | Description |
| 0 | 0 | Forbidden | Invalid |
| 0 | 1 | 1 | Q is set to 1 |
| 1 | 0 | 0 | Q is set to 0 |
| 1 | 1 | No change | No change |

* 1. Figure 17 is basically a SR latch. Table above is the truth table with description. When the SPDT switch is connected to A, D is 0 since it connects to the ground. By the property of NAND gate, output Q will be 1. Once the SPDT switch leaves A, because of the pull-up resistors, both A and B will be pulled to a logic 1. According to the table, there will be no change to the output Q. Once the SPDT switch hit B, G will be 0 and QN = E = 1 by the property of NAND gate. Q will be set to 0 due to both inputs being 1. Once the SPDT switch bounces away from B, again, A and B will be pulled to a logic 1, which will have no change to the current state. Thus, the effect of mechanical contact bounces is eliminated.

**Answer to General Guide Question (Pretty much done)**

**GG.6&7**

**Advantage of Larger Noise Immunity**

The advantage of a larger noise immunity is that even with larger noise from inside and outside of the circuit, the signal would still be valid.

**Why last inverter?**

The reason for the last inverter rather than the first is because the last inverter would have the lowest energy and the most noise since all the inverters would have some noise and they sums up.

**How to calculate the noise immunity?**

From the graph, we see that the inverter operates in the range from 0.35 – 3.5 V. To find the noise immunity for output to be 1, we trace from V\_out = 2 V to V\_in, and we find that V\_in at 1.15 V. Even though the graph starts at 0 V for V\_in, the range of inverter starts at 0.35 V. So, the noise immunity for V\_out to be 1 is 1.15 – 0.35 = 0.8 V. Similarly, the noise immunity for V\_out to be 0 is from 1.35 to 3.5V. Even though the graph extends to 4 V, we know the inverter operates from 0.35 – 3.5 V. So, the noise immunity for V\_out to be 0 is 3.5 – 1.35 = 2.15 V.

**GG.31**

It is bad practice to share resistors because it’s not safe to connect LEDs in parallel. When we share resistors across multiple LEDs, we assume that the characteristics of LEDs are the same. However, in the real world, LEDs do not have the same characteristics and therefore there is a possible case that one LED conducts most of the current while other LEDs barely conduct any current at all.

## Conclusions

I have learned about potential glitches that exist in the Boolean expressions that we learned in ECE 120. For example, if two Boolean functions in the SOP do not overlaps in the K-map, then there’s a potential glitch exists in the output. I also learned about debounce circuit. It is a fascinating design for me to think about. I wonder how people come up with it when the technology is so limited. I also learned about using Fritzing. You can tell from the schematic of part B that I improved a lot from my part A.