

POLITECNICO DI TORINO

Faculty of Electronic Engineering
Master degree course in Electronic Engineering

Master Degree Thesis

Fault tolerant RISC-V architecture with FreeRTOS

Based on cv32e40p core of PULP project



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To my family and Anna.

citazione
Huxley

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acknowledgments

Summary

Abstract

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Chapter 1

Introduction

1.1 General Context

Appendix A

An appendix

Bibliography

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