	Result	Size	Time	Cycles	GPU	SM Frequency	Process	Attributes
Current	660 - brute_force_AL	(1024, 1, 1)x(1024, 1, 1)	2.10 ms	1,228,804	0 - Tesla T4	585.00 Mhz	[19666] exe	

Summary | Details | Source | Context | Comments | Raw | Session

Compare | Tools | View | Export

GPU Speed Of Light Throughput

All

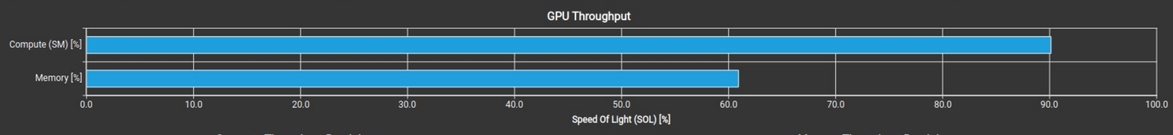
High-level overview of the throughput for compute and memory resources of the GPU. For each unit, the throughput reports the achieved percentage of utilization with respect to the theoretical maximum. Breakdowns show the throughput for each individual sub-metric of Compute and Memory to clearly identify the highest contributor. High-level overview of the utilization for compute and memory resources of the GPU presented as a roofline chart.

Compute (SM) Throughput [%]	90.13	Duration [ms]	2.10
Memory Throughput [%]	60.93	Elapsed Cycles [cycle]	1,228,804
L1/TEX Cache Throughput [%]	62.39	SM Active Cycles [cycle]	1,204,589.27
L2 Cache Throughput [%]	2.14	SM Frequency [Mhz]	585.00
DRAM Throughput [%]	0.88	DRAM Frequency [Ghz]	5.00

High Throughput The kernel is utilizing greater than 80.0% of the available compute or memory performance of the device. To further improve performance, work will likely need to be shifted from the most utilized to another unit. Start by analyzing workloads in the Compute Workload Analysis section.

Roofline Analysis The ratio of peak float (fp32) to double (fp64) performance on this device is 32:1. The kernel achieved 15% of this device's fp32 peak performance and 0% of its fp64 peak performance. See the Kernel Profiling Guide for more details on roofline analysis.

GPU Throughput



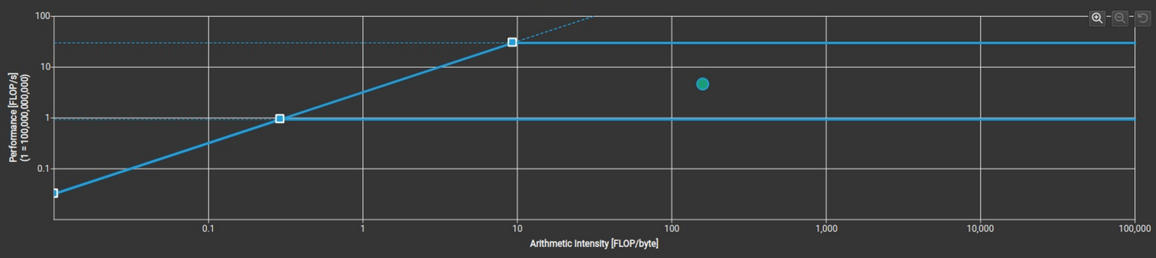
Compute Throughput Breakdown

SM: Inst Executed Pipe Xu [%]	90.13
SM: Issue Active [%]	60.95
SM: Inst Executed [%]	60.95
SM: Inst Executed Pipe Lsu [%]	60.93
SM: Pipe Fma Cycles Active [%]	42.23
SM: Pipe Alu Cycles Active [%]	36.86
SM: Mio Inst Issued [%]	20.40
SM: Mio2rf Writeback Active [%]	14.27
SM: Mio Pq Read Cycles Active [%]	1.40
SM: Mio Pq Write Cycles Active [%]	1.40
SM: Inst Executed Pipe Adu [%]	0.27
IDC: Request Cycles Active [%]	0.14
SM: Inst Executed Pipe Cbu Pred On Any [%]	0.07
SM: Memory Throughput Internal Activity [%]	0
SM: Pipe Tensor Cycles Active [%]	0
SM: Pipe Shared Cycles Active [%]	0
SM: Pipe Fp64 Cycles Active [%]	0
SM: Instruction Throughput Internal Activity [%]	0
SM: Inst Executed Pipe Uniform [%]	0
SM: Inst Executed Pipe Tex [%]	0
SM: Inst Executed Pipe Ipa [%]	0
SM: Inst Executed Pipe Fp16 [%]	0

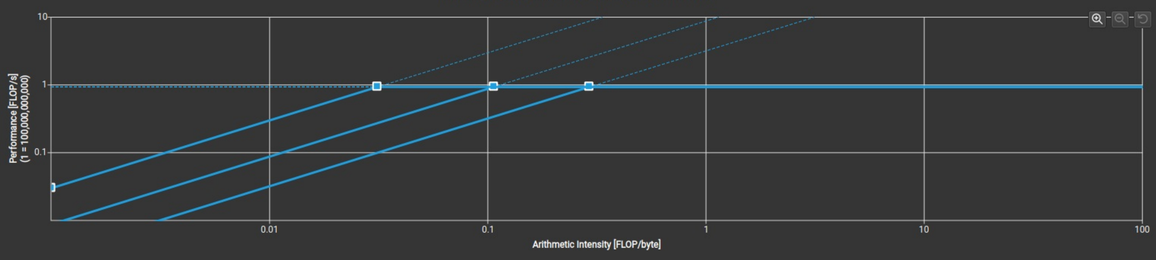
Memory Throughput Breakdown

L1: Lsuin Requests [%]	60.93
L1: Data Pipe Lsu Wavefronts [%]	31.19
L1: Lsu Writeback Active [%]	28.40
L1: Data Bank Reads [%]	8.40
L1: M L1tex2xbar Req Cycles Active [%]	2.45
L2: T Sectors [%]	2.14
L2: Xbar2lts Cycles Active [%]	2.08
DRAM: Cycles Active [%]	0.88
L1: Data Bank Writes [%]	0.74
DRAM: Dram Sectors [%]	0.64
L2: D Sectors [%]	0.61
L2: T Tag Requests [%]	0.55
GPU: Compute Memory Access Throughput Internal Activity [%]	0.54
L1: M Xbar2l1tex Read Sectors [%]	0.36
L2: Lts2xbar Cycles Active [%]	0.30
L2: D Sectors Fill Device [%]	0.02
L1: F Wavefronts [%]	0.00
L1: Texin Sm2tex Req Cycles Active [%]	0.00
L1: Data Pipe Tex Wavefronts [%]	0
GPU: Compute Memory Request Throughput Internal Activity [%]	0
L1: Tex Writeback Active [%]	0
L2: D Atomic Input Cycles Active [%]	0
L2: D Sectors Fill Sysmem [%]	0

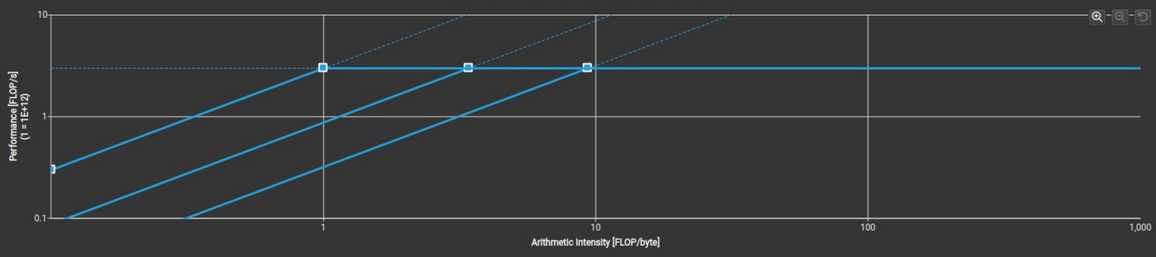
Floating Point Operations Roofline



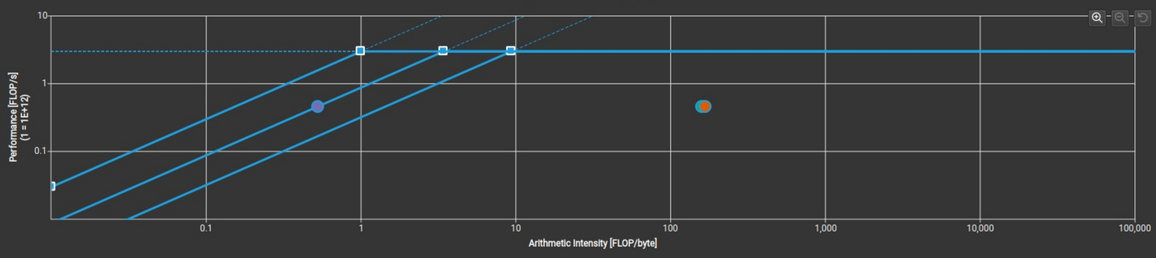
Floating Point Operations Roofline (Double Precision)



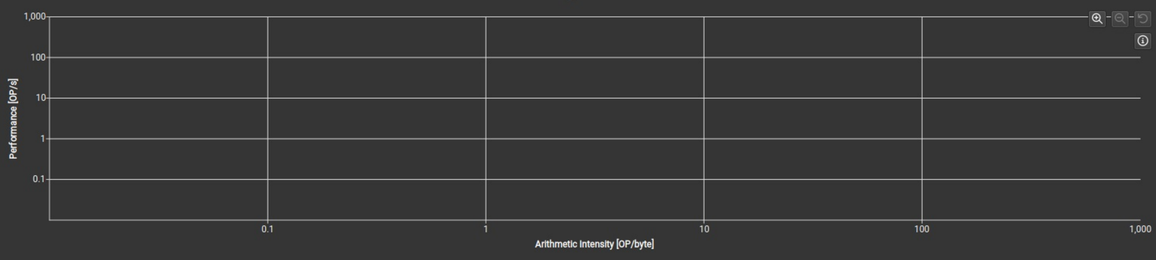
Floating Point Operations Roofline (Half Precision)



Floating Point Operations Roofline (Single Precision)



Tensor Core Operations Roofline



	# Operations	# Operations / Cycle	# Operations / s	Peak %	Peak Operations / Cycle	Peak Operations / s
Src:fp16,bf16,tf32 Dst:fp32	0	0	0	0	40,960	23,963.23
Src:fp16 Dst:fp16	0	0	0	0	40,960	23,963.23
Src:int1	0	0	0	0	81,920	47,926.46
Src:int4	0	0	0	0	81,920	47,926.46
Src:int8	0	0	0	0	81,920	47,926.46

GPU and Memory Workload Distribution

Analysis of workload distribution in active cycles of SM, SMP, SMSP, L1 & L2 caches, and DRAM

Average SM Active Cycles [cycle]	1,204,589.27	Average L1 Active Cycles [cycle]	1,204,589.27
Average L2 Active Cycles [cycle]	214,856.78	Average SMSP Active Cycles [cycle]	1,201,336.01
Average DRAM Active Cycles [cycle]	92,029.50	Total SM Elapsed Cycles [cycle]	49,155,328
Total L1 Elapsed Cycles [cycle]	49,155,328	Total L2 Elapsed Cycles [cycle]	57,469,376
Total SMSP Elapsed Cycles [cycle]	196,621,312	Total DRAM Elapsed Cycles [cycle]	83,977,216

Workload Distribution

	Average	Min	Max	Sum
SM Active Cycles	1,204,589.27	1,176,635	1,223,676	48,183,571
SMSP Active Cycles	1,201,336.01	1,172,382	1,221,057	192,213,761
L1 Active Cycles	1,204,589.27	1,176,635	1,223,676	48,183,571
L2 Active Cycles	214,856.78	194,156	251,520	6,875,417
DRAM Active Cycles	92,029.50	86,736	101,908	736,236