	Result	Size	Time	Cycles	GPU	SM Frequency	Process	Attributes
Current	559 - brute_force	(4, 1, 1)x(1024, 1, 1)	11.94 ms	6,982,928	0 - Tesla T4	585.00 Mhz	[12442] exe	

Summary | Details | Source | Context | Comments | Raw | Session

Compare | Tools | View | Export

GPU Speed Of Light Throughput

All

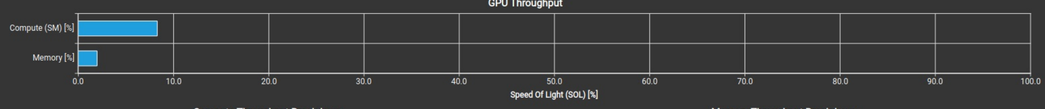
High-level overview of the throughput for compute and memory resources of the GPU. For each unit, the throughput reports the achieved percentage of utilization with respect to the theoretical maximum. Breakdowns show the throughput for each individual sub-metric of Compute and Memory to clearly identify the highest contributor. High-level overview of the utilization for compute and memory resources of the GPU presented as a roofline chart.

Compute (SM) Throughput [%]	8.29	Duration [ms]	11.94
Memory Throughput [%]	1.97	Elapsed Cycles [cycle]	6,982,928
L1/TEX Cache Throughput [%]	20.41	SM Active Cycles [cycle]	674,538.57
L2 Cache Throughput [%]	0.00	SM Frequency [Mhz]	585.00
DRAM Throughput [%]	0.00	DRAM Frequency [Ghz]	5.00

Small Grid This kernel grid is too small to fill the available resources on this device, resulting in only 0.1 full waves across all SMs. Look at Launch Statistics for more details.

Roofline Analysis The ratio of peak float (fp32) to double (fp64) performance on this device is 32:1. The kernel achieved close to 0% of this device's fp32 peak performance and close to 0% of its fp64 peak performance. See the Kernel Profiling Guide for more details on roofline analysis.

GPU Throughput



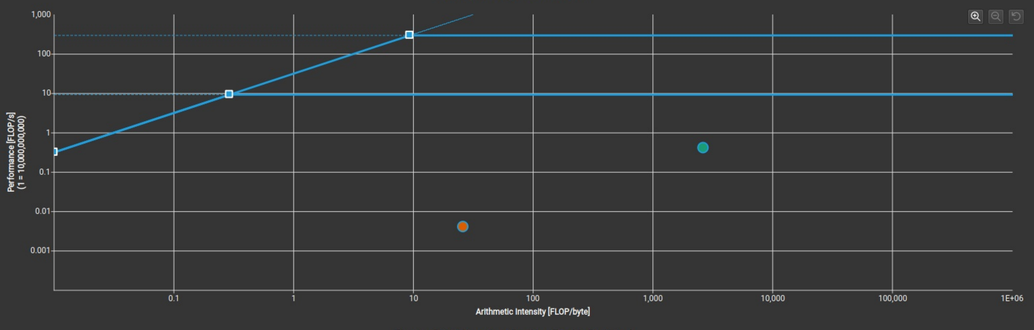
Compute Throughput Breakdown

SM: Pipe Alu Cycles Active [%]	8.29
SM: Issue Active [%]	7.18
SM: Inst Executed [%]	7.18
SM: Inst Executed Pipe Adu [%]	3.93
IDC: Request Cycles Active [%]	2.93
SM: Pipe Fma Cycles Active [%]	2.47
SM: Inst Executed Pipe Lsu [%]	1.97
SM: Mio Inst Issued [%]	1.97
SM: Mio Pq Write Cycles Active [%]	1.96
SM: Mio Pq Read Cycles Active [%]	1.95
SM: Inst Executed Pipe Cbu Pred On Any [%]	1.54
SM: Mio2rf Writeback Active [%]	0.97
SM: Pipe Fp64 Cycles Active [%]	0.06
SM: Inst Executed Pipe Uniform [%]	0.01
SM: Inst Executed Pipe Xu [%]	0.00
SM: Memory Throughput Internal Activity [%]	0
SM: Pipe Tensor Cycles Active [%]	0
SM: Pipe Shared Cycles Active [%]	0
SM: Instruction Throughput Internal Activity [%]	0
SM: Inst Executed Pipe Tex [%]	0
SM: Inst Executed Pipe Ipa [%]	0
SM: Inst Executed Pipe Fp16 [%]	0

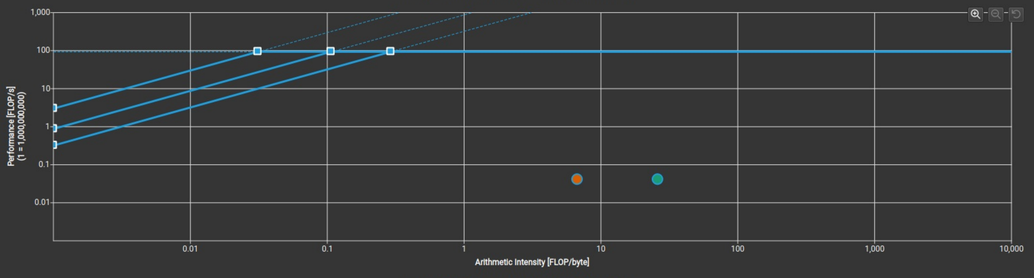
Memory Throughput Breakdown

L1: Lsuin Requests [%]	1.97
L1: Data Pipe Lsu Wavefronts [%]	1.06
L1: Lsu Writeback Active [%]	0.48
L1: Data Bank Reads [%]	0.11
L1: Data Bank Writes [%]	0.06
L2: T Sectors [%]	0.00
L2: Ltc2xbar Cycles Active [%]	0.00
L2: Xbar2ltc Cycles Active [%]	0.00
L1: M L1tex2xbar Req Cycles Active [%]	0.00
GPU: Compute Memory Access Throughput Internal Activity [%]	0.00
DRAM: Cycles Active [%]	0.00
L2: D Sectors [%]	0.00
L2: D Sectors Fill Device [%]	0.00
DRAM: Dram Sectors [%]	0.00
L2: T Tag Requests [%]	0.00
L1: F Wavefronts [%]	0.00
L1: Texin Sm2tex Req Cycles Active [%]	0.00
L1: Data Pipe Tex Wavefronts [%]	0
L1: M Xbar2l1tex Read Sectors [%]	0
L1: Tex Writeback Active [%]	0
L2: D Atomic Input Cycles Active [%]	0
L2: D Sectors Fill Sysmem [%]	0
GPU: Compute Memory Request Throughput Internal Activity [%]	0

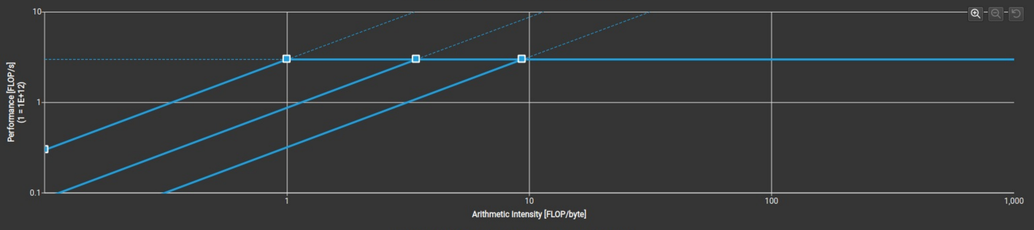
Floating Point Operations Roofline



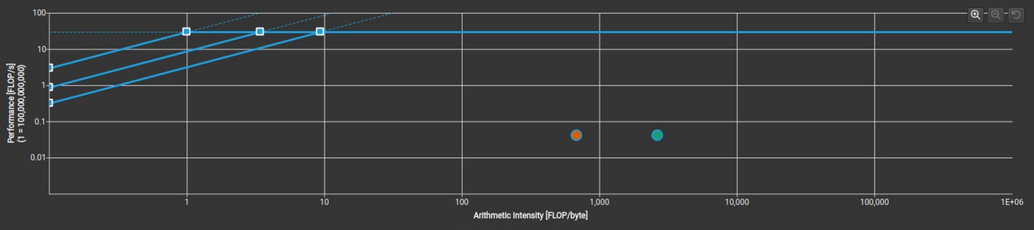
Floating Point Operations Roofline (Double Precision)



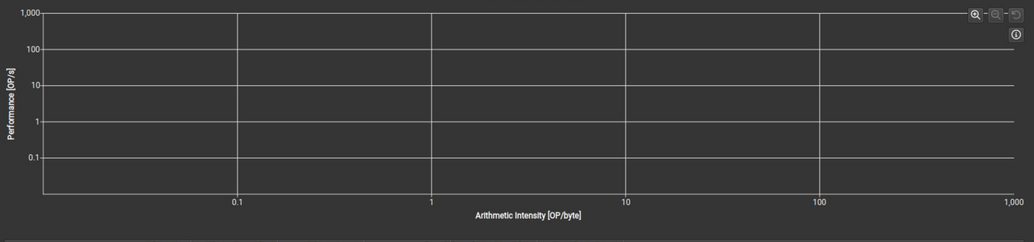
Floating Point Operations Roofline (Half Precision)



Floating Point Operations Roofline (Single Precision)



Tensor Core Operations Roofline



	# Operations	# Operations / Cycle	# Operations / s	Peak % Peak Operations / Cycle	Peak Operations / s
Src:fp16,bf16,tf32 Dst:fp32	0	0	0	0	40,960	23,957.58
Src:fp16 Dst:fp16	0	0	0	0	40,960	23,957.58
Src:int1	0	0	0	0	81,920	47,915.15
Src:int4	0	0	0	0	81,920	47,915.15
Src:int8	0	0	0	0	81,920	47,915.15

GPU and Memory Workload Distribution

Analysis of workload distribution in active cycles of SM, SMP, SMSP, L1 & L2 caches, and DRAM

Average SM Active Cycles [cycle]	674,538.57	Average L1 Active Cycles [cycle]	674,538.57
Average L2 Active Cycles [cycle]	962.56	Average SMSP Active Cycles [cycle]	649,137.07
Average DRAM Active Cycles [cycle]	286	Total SM Elapsed Cycles [cycle]	279,271,208
Total L1 Elapsed Cycles [cycle]	279,271,208	Total L2 Elapsed Cycles [cycle]	326,586,144
Total SMSP Elapsed Cycles [cycle]	1,117,084,832	Total DRAM Elapsed Cycles [cycle]	477,679,616

SMs Workload Imbalance
Est. Speedup: 8.73%
One or more SMs have a much lower number of active cycles than the average number of active cycles. Maximum instance value is 90.34% above the average, while the minimum instance value is 100.00% below the average.

SMSPs Workload Imbalance
Est. Speedup: 8.43%
One or more SMSPs have a much lower number of active cycles than the average number of active cycles. Maximum instance value is 90.70% above the average, while the minimum instance value is 100.00% below the average.

L1 Slices Workload Imbalance
Est. Speedup: 8.73%
One or more L1 Slices have a much lower number of active cycles than the average number of active cycles. Maximum instance value is 90.34% above the average, while the minimum instance value is 100.00% below the average.

Workload Distribution

	Average	Min	Max	Sum
SM Active Cycles	674,538.57	0	6,980,954	26,981,543
SMSP Active Cycles	649,137.07	0	6,980,930	103,861,932
L1 Active Cycles	674,538.57	0	6,980,954	26,981,543
L2 Active Cycles	962.56	427	1,638	30,802
DRAM Active Cycles	286	168	400	2,288