	Result	Size	Time	Cycles	GPU	SM Frequency	Process	Attributes
Current	728 - brute_force_AL_coarsening	(32768, 1, 1)x(32, 1, 1)	2.16 ms	1,263,896	0 - Tesla T4	584.98 Mhz	[9877] exe	

Summary | Details | Source | Context | Comments | Raw | Session

Compare | Tools | View | Export

GPU Speed Of Light Throughput

All

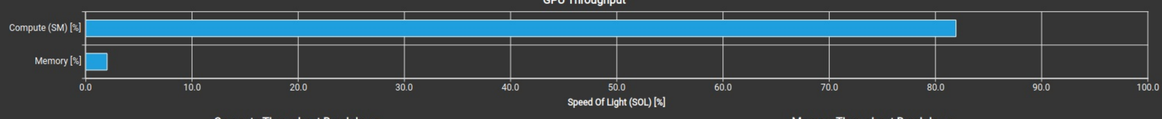
High-level overview of the throughput for compute and memory resources of the GPU. For each unit, the throughput reports the achieved percentage of utilization with respect to the theoretical maximum. Breakdowns show the throughput for each individual sub-metric of Compute and Memory to clearly identify the highest contributor. High-level overview of the utilization for compute and memory resources of the GPU presented as a roofline chart.

Compute (SM) Throughput [%]	81.94	Duration [ms]	2.16
Memory Throughput [%]	2.01	Elapsed Cycles [cycle]	1,263,896
L1/TEX Cache Throughput [%]	1.56	SM Active Cycles [cycle]	1,257,112.10
L2 Cache Throughput [%]	0.67	SM Frequency [Mhz]	584.98
DRAM Throughput [%]	2.01	DRAM Frequency [Ghz]	4.98

High Throughput The kernel is utilizing greater than 80.0% of the available compute or memory performance of the device. To further improve performance, work will likely need to be shifted from the most utilized to another unit. Start by analyzing workloads in the Compute Workload Analysis section.

FP64/32 Utilization
Est. Local Speedup: 65.14% The ratio of peak float (fp32) to double (fp64) performance on this device is 32:1. The kernel achieved close to 1% of this device's fp32 peak performance and 61% of its fp64 peak performance. If Compute Workload Analysis determines that this kernel is fp64 bound, consider using 32-bit precision floating point operations to improve its performance. See the Kernel Profiling Guide for more details on roofline analysis.

GPU Throughput



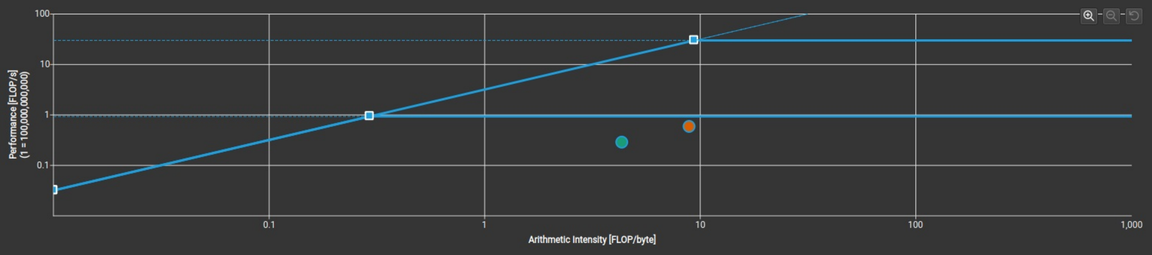
Compute Throughput Breakdown

SM: Pipe Fp64 Cycles Active [%]	81.94
SM: Pipe Alu Cycles Active [%]	43.51
SM: Issue Active [%]	34.17
SM: Inst Executed [%]	34.17
SM: Mio Pq Write Cycles Active [%]	26.92
SM: Inst Executed Pipe Adu [%]	19.71
IDC: Request Cycles Active [%]	11.32
SM: Pipe Fma Cycles Active [%]	10.23
SM: Mio Inst Issued [%]	10.11
SM: Mio Pq Read Cycles Active [%]	5.92
SM: Inst Executed Pipe Cbu Pred On Any [%]	4.60
SM: Mio2rf Writeback Active [%]	2.89
SM: Inst Executed Pipe Lsu [%]	0.39
SM: Inst Executed Pipe Xu [%]	0.13
SM: Pipe Tensor Cycles Active [%]	0
SM: Inst Executed Pipe Fp16 [%]	0
SM: Pipe Shared Cycles Active [%]	0
SM: Memory Throughput Internal Activity [%]	0
SM: Instruction Throughput Internal Activity [%]	0
SM: Inst Executed Pipe Uniform [%]	0
SM: Inst Executed Pipe Tex [%]	0
SM: Inst Executed Pipe Ipa [%]	0

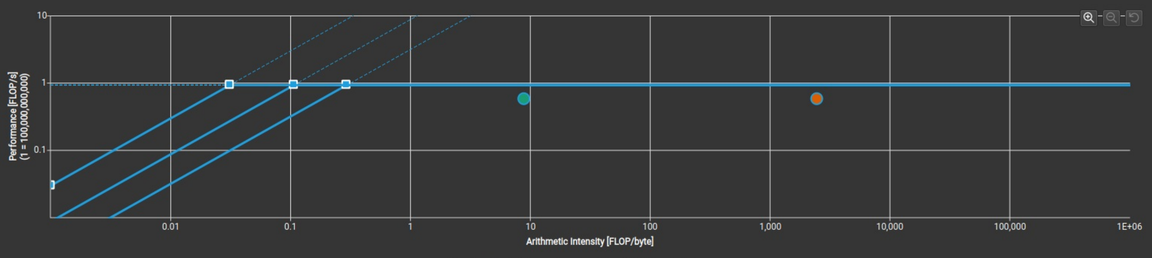
Memory Throughput Breakdown

DRAM: Cycles Active [%]	2.01
DRAM: Dram Sectors [%]	1.46
L1: M L1tex2xbar Req Cycles Active [%]	0.78
L2: T Sectors [%]	0.67
L2: Xbar2lts Cycles Active [%]	0.67
L1: Lsuin Requests [%]	0.39
L2: D Sectors [%]	0.32
L1: Data Pipe Lsu Wavefronts [%]	0.28
GPU: Compute Memory Access Throughput Internal Activity [%]	0.17
L2: T Tag Requests [%]	0.17
L1: Data Bank Reads [%]	0.10
L1: Data Bank Writes [%]	0.10
L1: Lsu Writeback Active [%]	0.06
L2: Lts2xbar Cycles Active [%]	0.00
L1: Texin Sm2tex Req Cycles Active [%]	0.00
L1: F Wavefronts [%]	0.00
L2: D Sectors Fill Device [%]	0.00
L1: M Xbar2l1tex Read Sectors [%]	0
L1: Tex Writeback Active [%]	0
L2: D Atomic Input Cycles Active [%]	0
L2: D Sectors Fill Sysmem [%]	0
L1: Data Pipe Tex Wavefronts [%]	0
GPU: Compute Memory Request Throughput Internal Activity [%]	0

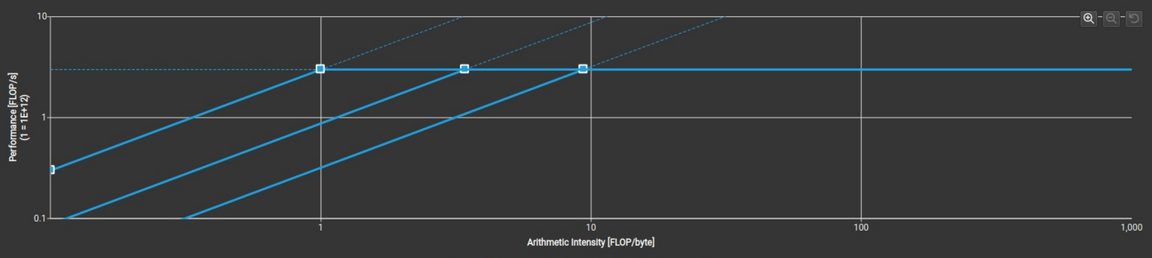
Floating Point Operations Roofline



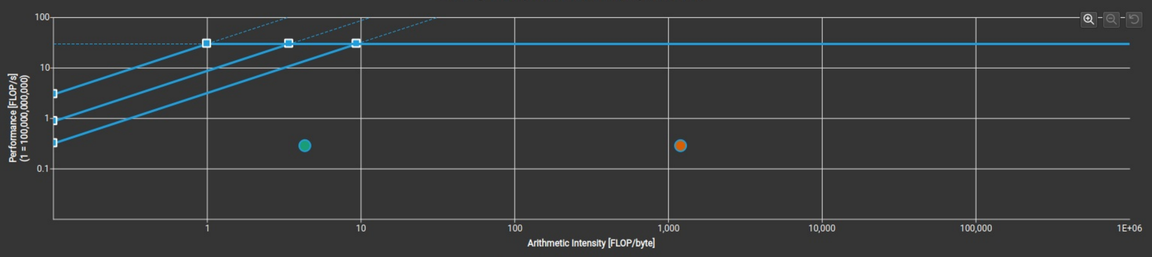
Floating Point Operations Roofline (Double Precision)



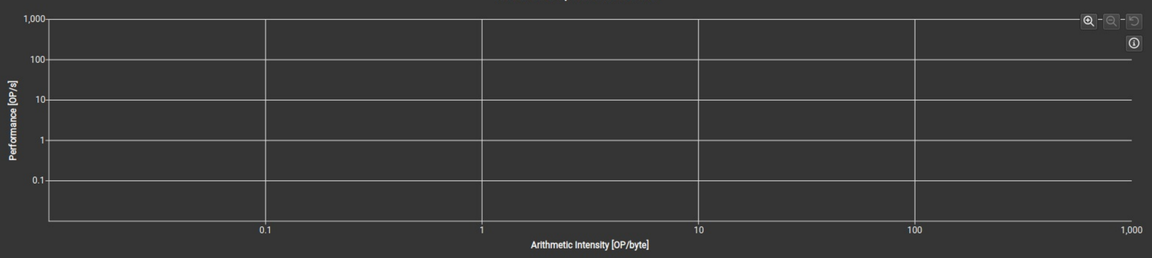
Floating Point Operations Roofline (Half Precision)



Floating Point Operations Roofline (Single Precision)



Tensor Core Operations Roofline



	# Operations	# Operations / Cycle	# Operations / s	Peak % ?eak Operations / Cycle	Peak Operations / Cycle	Peak Operations / s
Src:fp16,bf16,tf32 Dst:fp32	0	0	0	0	40,960	23,957.43
Src:fp16 Dst:fp16	0	0	0	0	40,960	23,957.43
Src:int1	0	0	0	0	81,920	47,914.87
Src:int4	0	0	0	0	81,920	47,914.87
Src:int8	0	0	0	0	81,920	47,914.87

GPU and Memory Workload Distribution

Analysis of workload distribution in active cycles of SM, SMP, SMSP, L1 & L2 caches, and DRAM

Average SM Active Cycles [cycle]	1,257,112.10	Average L1 Active Cycles [cycle]	1,257,112.10
Average L2 Active Cycles [cycle]	109,956.31	Average SMSP Active Cycles [cycle]	1,255,327.39
Average DRAM Active Cycles [cycle]	216,128	Total SM Elapsed Cycles [cycle]	50,548,688
Total L1 Elapsed Cycles [cycle]	50,548,688	Total L2 Elapsed Cycles [cycle]	59,111,168
Total SMSP Elapsed Cycles [cycle]	202,194,752	Total DRAM Elapsed Cycles [cycle]	86,095,872

Workload Distribution

	Average	Min	Max	Sum
SM Active Cycles	1,257,112.10	1,253,817	1,261,117	50,284,484
SMSP Active Cycles	1,255,327.39	1,249,525	1,261,019	200,852,382
L1 Active Cycles	1,257,112.10	1,253,817	1,261,117	50,284,484
L2 Active Cycles	109,956.31	109,287	110,793	3,518,602
DRAM Active Cycles	216,128	215,560	216,704	1,729,024