FAIRCHILD SEMICONDUCTOR™

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CD4094BC
8-Bit Shift Register/Latch with 3-STATE Outputs

General Description

The CD4094BC consists of an 8-bit shift register and a 3-STATE 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage (Q_S) can be used to cascade several devices. Data on the Q_S output is transferred to a second output, Q'_S, on the following negative clock edge.

The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is HIGH, data propagates through the latch to 3-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken HIGH.

Features

- Wide supply voltage range: 3.0V to 18V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility:
  Fan out of 2 driving 74L or 1 driving 74LS
- 3-STATE outputs

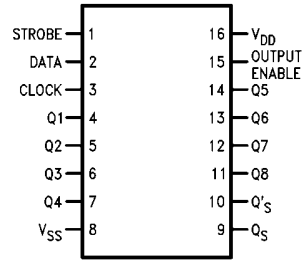
Ordering Code:

Order Number	Package Number	Package Description
CD4094BCWM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
CD4094BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOIC



Top View

Truth Table

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S (Note 1)	Q'_Σ
⌐‾	0	X	X	Hi-Z	Hi-Z	Q7	No Change
‾⌐	0	X	X	Hi-Z	Hi-Z	No Change	Q7
⌐‾	1	0	X	No Change	No Change	Q7	No Change
⌐‾	1	1	0	0	Q_N–1	Q7	No Change
⌐‾	1	1	1	1	Q_N–1	Q7	No Change
‾⌐	1	1	1	No Change	No Change	No Change	Q7

X = Don't Care
‾⌐ = HIGH-to-LOW
⌐‾ = LOW-to-HIGH

Note 1: At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

Block Diagram