CPU Architecture

LAB2 preparation report

VHDL part2

Sequential code and Behavioral modeling

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1. Aim of the Laboratory

- Obtaining skills in VHDL part2 code, which contains Sequential code and Behavioral modeling.
- Obtaining basic skills in ModelSim (multi-language HDL simulation environment).
- knowledge in digital systems design.
- Proper analysis and understanding of architecture design.

2. System Design definition

In this laboratory you will design a synchronous digital system which implements a dynamic growing N-modulo counter where N is growing dynamically each counting round till it reaches the ***UpperBound*** value and starts from the beginning. The system block diagram is depicted in figure 1, you are required to design the whole system and make a test bench for testing.

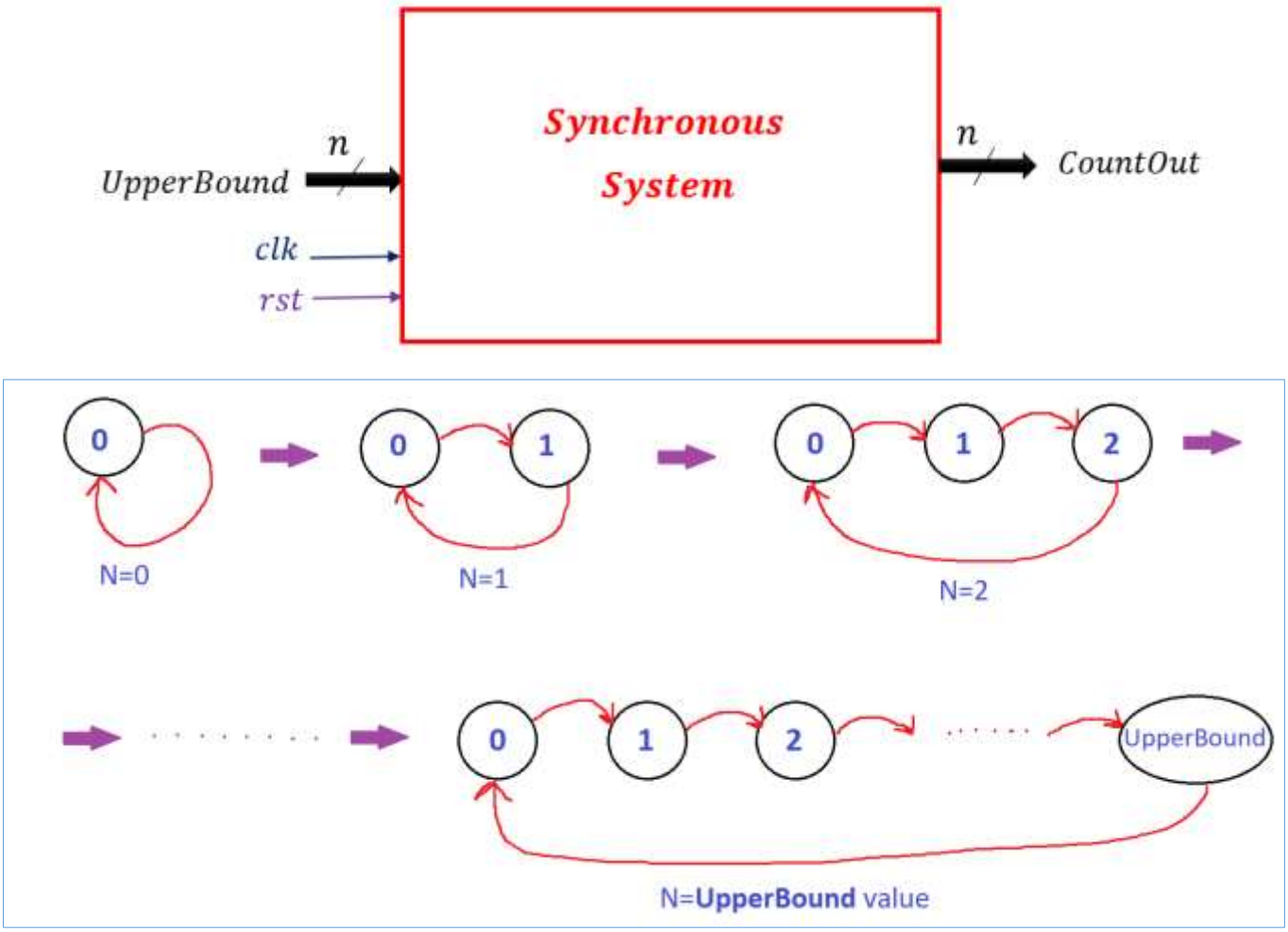
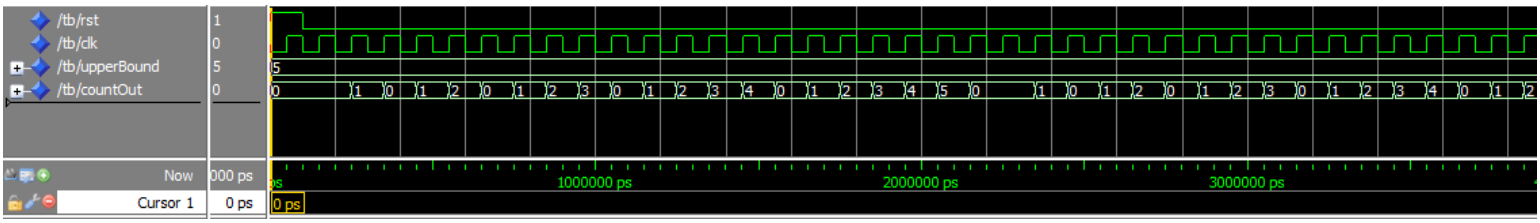


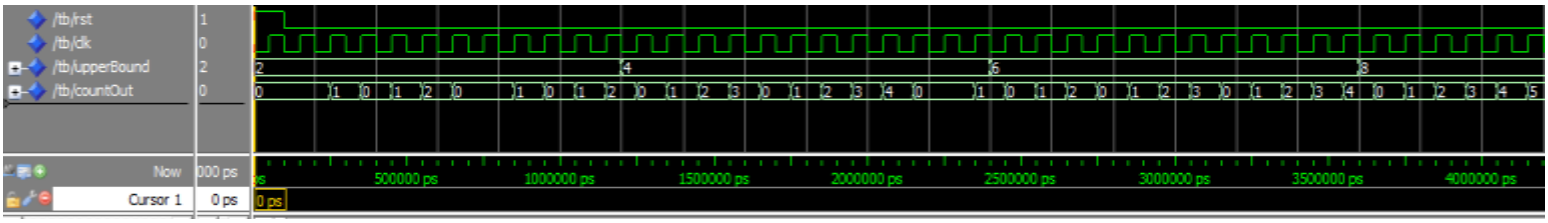
Figure 1 : System structure

- The Top Level design modeling should be Behavioral.
- You are given the above two files that you must use ***only*** in your project: **top.vhd**, **aux_package.vhd (**you must use the given Entity definitions and can only add your code to these files, ***you are not allowed to erase anything*****).** The given **top.vhd** contains two PROCESS' template that you can use ***only*** *(i.e. you cannot add more PROCESS).*
- The submitted project must be compiled using the given **tb.vhd** file (otherwise the submitted project will be considered as a failure).
- The submitted assignments get through copy checking machine, in this case, both sides' assignments will be disqualified.
- **Examples:**

  Example where ***UpperBound*** value remains unchanged.



  Example where ***UpperBound*** value is changed throughout time.



3. Test and Timing:

- Design a test bench which tests all the system.
- Analyze the results by zooming on the important transactions in the waveforms. explain these (input/output/internal signals of the system).
- You are welcome to use the Internet also as reference.
- The timing of the system will be ideal (means a functional simulation).

4. Requirements

a. The lab assignment is in pairs (as shown in the inlay file).

b. The design must be well commented.

c. **Important:** For each of two submodules:

- Graphical description (a square with ports going in and out) and short descriptions.

d. Elaborated analysis and wave forms:

- Remove irrelevant signals.
- Zoom on regions of interest.
- Draw clouds on the waveform with explanations of what is happening (Figure 4).
- Change the waveform colors in ModelSim for clear documentation **(Tools->Edit Preferences->Wave Windows).**

e. A ZIP file in the form of **id1_id2.zip** (where id1 and id2 are the identification number of the submitters, and id1 < id2) *must be upload to Moodle only by student with id1* (any of these rules violation disqualifies the task submission).

f. The **ZIP** file will contain (***only the exact next sub folders***):

Directory	Contains	Comments
DUT	Project VHDL files	**Only VHDL files of DUT**, excluding test bench **Note: your project files must be well compiled without errors as a basic condition before submission**
TB	VHDL files that are used for test bench	At least two test bench file you used to simulate the DUT
SIM	ModelSim DO files (wave, list)	To pairs of DO file (one for wave and one for list)
DOC	Project documentation	• ***readme.txt*** (list of the DUT **.vhd* files with their brief functional description) • ***pre1.pdf*** (report file that includes brief explanation of the top module with its wave diagrams as shown in figure 3)

Table 2: Directory Structure

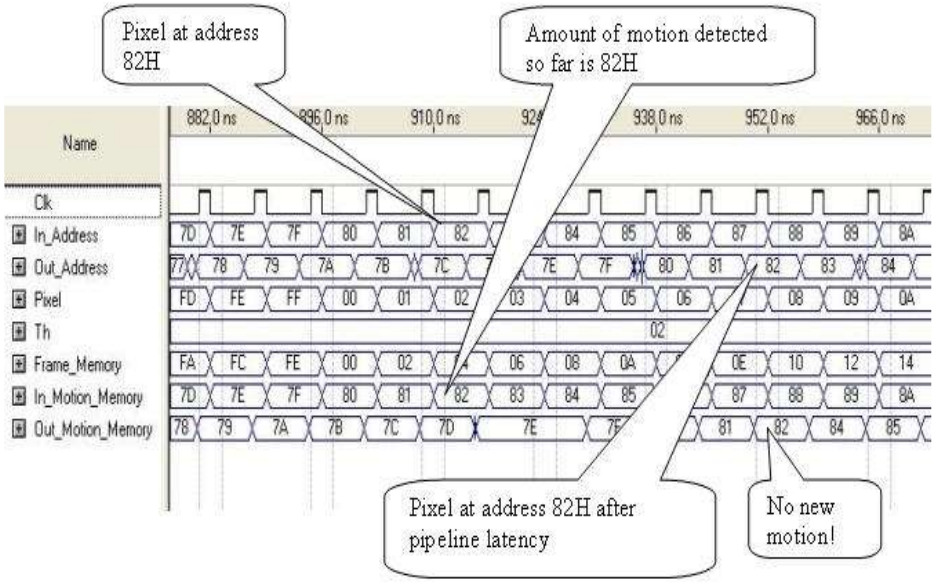


Figure 3: Clouds over the waveform example

5. Grading Policy

Weight	Task	Description
10%	Documentation	The "clear" way in which you presented the requirements and the analysis and conclusions on the work you've done
90%	Analysis and Test	The correct analysis of the system (under the requirements)

Table 1 : Grading

Under the above policies you'll be also evaluated using common sense:

- Your files will be compiled and checked, the system must work.
- Your design and architecture must be intelligent, minimal, effective and well organized.

For a late submission the penalty is 2^{days}