CPU Architecture

LAB1 preparation report

VHDL part1 – Concurrent code

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Table of contents

1. Aim of the Laboratory

- Obtaining skills in VHDL part1 code, which contains Code Structure, Data Types, Operators and Attributes, Concurrent Code, Design Hierarchy, Packages and Components.
- Obtaining basic skills in ModelSim (multi-language HDL simulation environment).
- General knowledge rehearsal in digital systems.
- Proper analysis and understanding of architecture design.

2. System Design definition

In this laboratory you will design a module which contains the next three sub-modules:

- Generic Adder/Subtractor module between two vectors Y, X of size n-bit (the default is n=8).
- Generic Shifter module based on Barrel-Shifter n-bit size (the default is n=8).
- Boolean Logic operates bitwise.
- The generic n value can be 4,8,16,32 (set from ***tb.vhd*** file).
- You are required to design the whole system and make a test bench for testing.

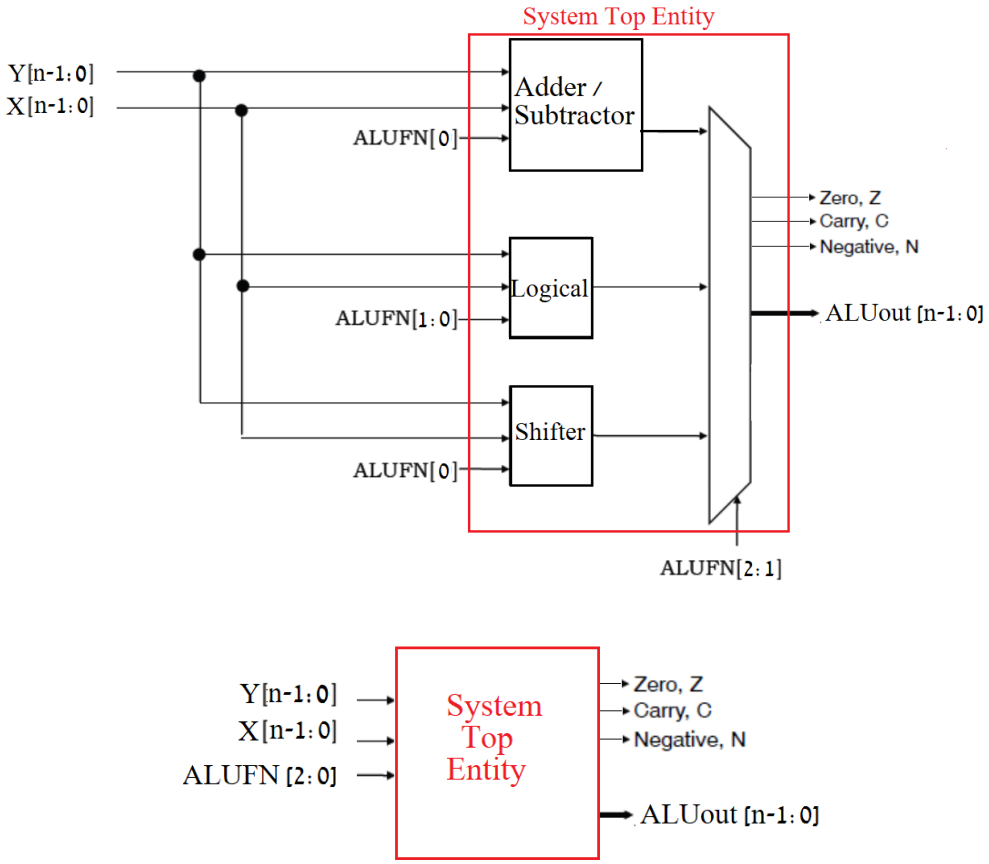
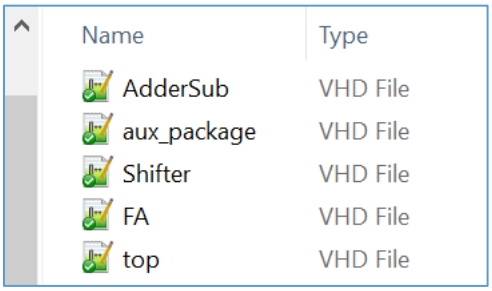


Figure 1 : System structure

Decimal value	ALUFN	Operation	Note
0	000	Res=Y+X	
1	001	Res=Y-X	
2	010	Res=SHL Y,X(k-1 to 0)	Shift Left Y of X(k-1 ..0) times When $k = \log_2 n$
3	011	Res=SHR Y,X(k-1 to 0)	Shift Right Y of X(k-1 ..0) times When $k = \log_2 n$
4	100	Res=Y or X	
5	101	Res=Y and X	
6	110	Res=Y xor X	
7	111	Res=Y nor X	

Table 1: Selected operations

- The Top Level design must be Structural (***your DUT must contain <u>at least</u> the next five *.vhd files***).



- You are given the above two files <u>that you must use in your project</u>: **top.vhd**, **aux_package.vhd (**you must use the given Entity definitions and can only add code to these files, ***you are not allowed to erase anything*****), you can only add *.vhd files.**
- The submitted project must be compiled using the given **tb.vhd** file (otherwise the submitted project will be considered as a failure).
- The submitted assignments get through copy checking machine, in this case, both sides' assignments will be disqualified.

3. Generic Adder/Subtractor module:

- You are required to design a Generic Adder/Subtractor between two vectors Y, X of size n-bit (the default is n=8), using the next diagram. The design must be Structural of a least two levels.
- In order to do so, you are asked to use the Generic Adder code that was given in Moodle.

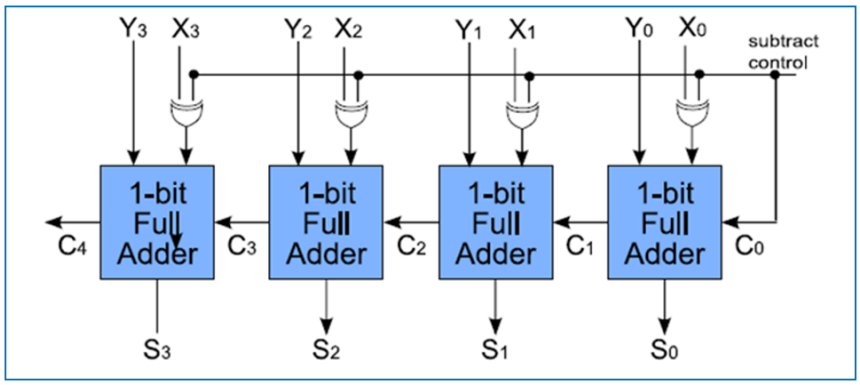


Figure 2: Generic Adder/Subtractor

4. Shifter Module based on Barrel-Shifter n-bit:

Note: using **sll, srl** operators are forbidden and will cause to disqualification of the assignment.

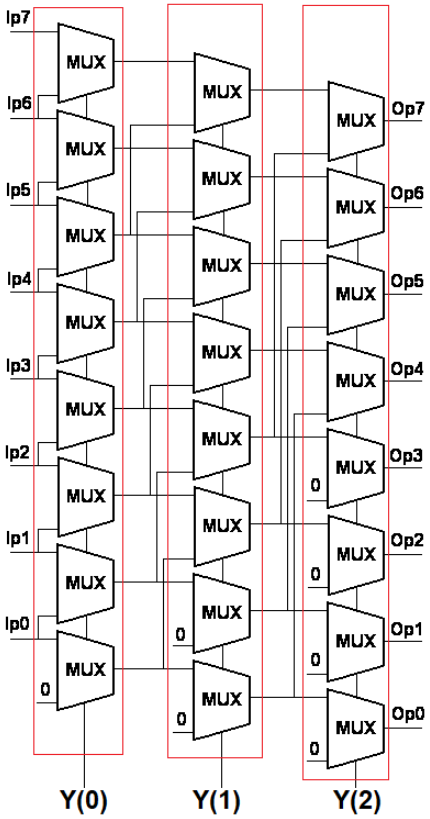


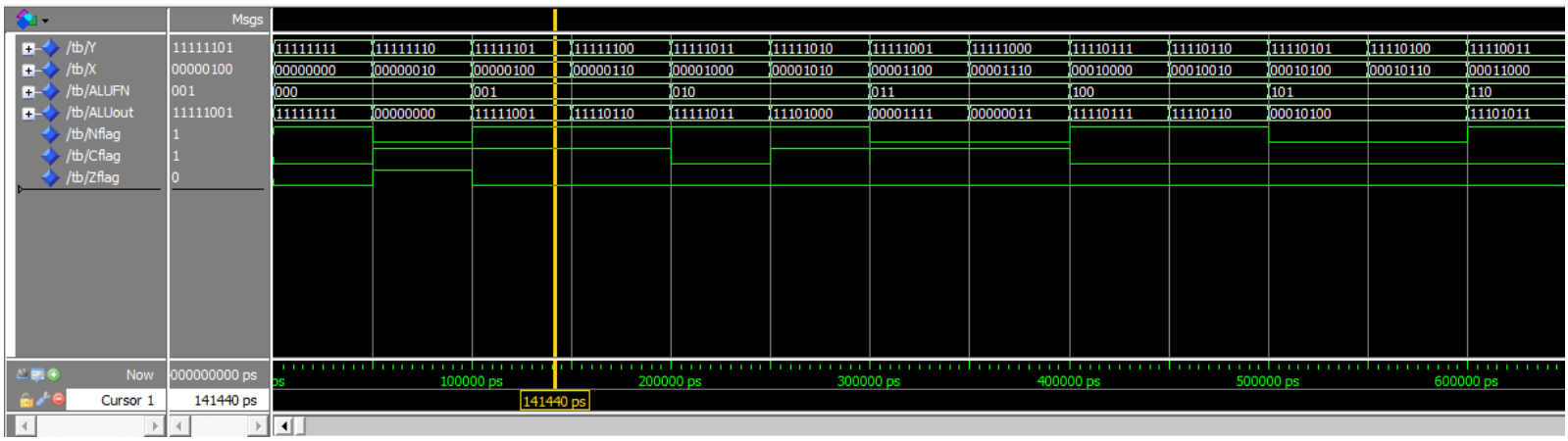
Figure 3: Example of 8-bit Barrel Shifter

5. Test and Timing:

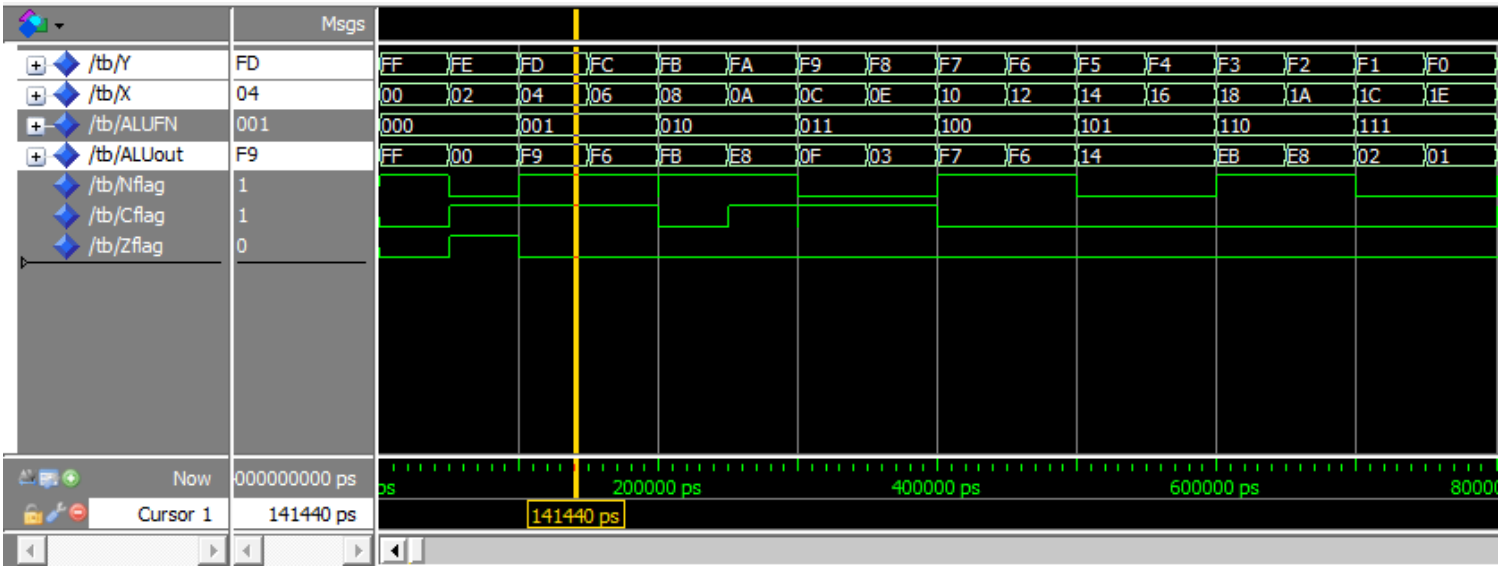
- Design a test bench which tests all the system.
- Analyze the results by zooming on the important transactions in the waveforms. explain these (input/output/internal signals of the system).
- You are welcome to use the Internet also as reference.
- **Good tip for beginners**: Build a test bench for each module you are designing for easy debugging, otherwise you will waste a lot of time for whole system debug.
- The timing of the system will be ideal (means a functional simulation).

6. System Output Example (for n=8)

Signals are shown in binary format



Signals ***Y, X, ALUout*** are shown in HEX format (same exact example as above).



7. Requirements

1. The lab assignment is in pairs (as shown in the inlay file).
2. The design must be well commented.
3. **Important:** For each of two submodules:
   - Graphical description (a square with ports going in and out) and short descriptions.
4. Elaborated analysis and wave forms:
   - Remove irrelevant signals.
   - Zoom on regions of interest.
   - Draw clouds on the waveform with explanations of what is happening (Figure 4).
   - Change the waveform colors in ModelSim for clear documentation **(Tools->Edit Preferences->Wave Windows).**
5. A ZIP file in the form of **id1_id2.zip** (where id1 and id2 are the identification number of the submitters, and id1 < id2) *must be upload to Moodle only by student with id1* (any of these rules violation disqualify the task submission).
6. The **ZIP** file will contain (***only the exact next sub folders***):

Directory	Contains	Comments
DUT	Project VHDL files	**Only VHDL files of DUT**, excluding test bench **Note: your project files must be well compiled without errors as a basic condition before submission**
TB	***Four*** VHDL files that are used for test bench	Adder/Subtractor, Logical, shifter, System (top)
SIM	***Four*** ModelSim DO files (wave, list)	Adder/Subtractor, Logical, shifter, System (top)
DOC	Project documentation	• ***readme.txt*** (list of the DUT **.vhd* files with their brief functional description) • ***pre1.pdf*** (report file that includes brief explanation of the four modules with their wave diagrams as shown in figure 4)

Table 2: Directory Structure

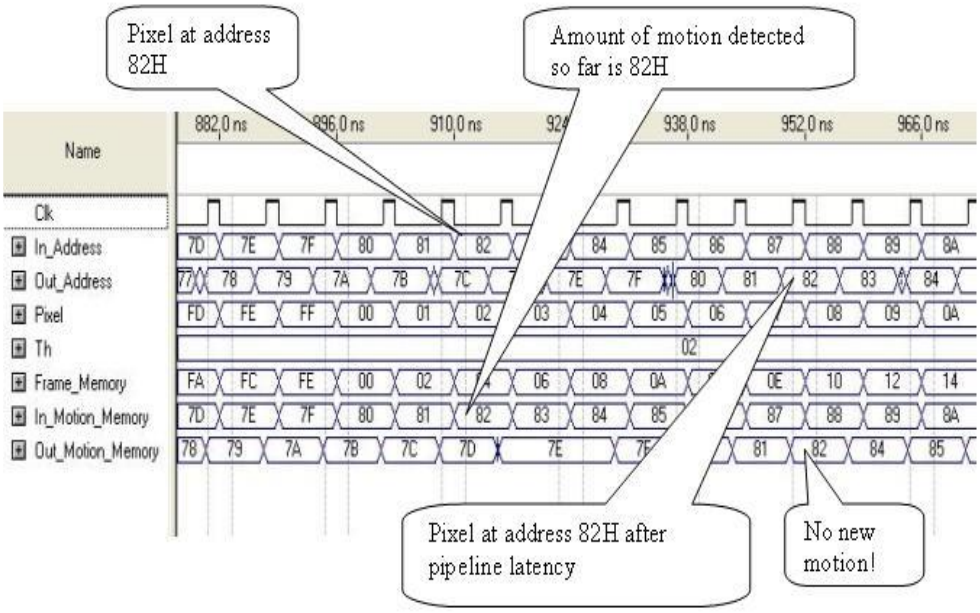


Figure 4: Clouds over the waveform

8. Grading Policy

Weight	Task	Description
10%	Documentation	The "clear" way in which you presented the requirements and the analysis and conclusions on the work you've done
90%	Analysis and Test	The correct analysis of the system (under the requirements)

Table 1 : Grading

Under the above policies you'll be also evaluated using common sense:

- Your files will be compiled and checked, the system must work.
- Your design and architecture must be intelligent, minimal, effective and well organized.

For a late submission the penalty is 2^{days}