Hi3518E V200 Economical HD IP Camera SoC

Brief Data Sheet

Issue 02

Date 2015-12-28

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Key Specifications

Processor Core

- ARM926@540 MHz, 32 KB I-cache, 32 KB D-cache

Video Encoding

- H.264 main/high profile L4.0
- H.264 baseline encoding
- MJPEG/JPEG baseline encoding

Video Encoding Performance

- A maximum of 2-megapixel resolution for H.264 encoding
- Real-time H.264 & JPEG encoding of multiple streams: 720p@30 fps+VGA@30 fps+QVGA@30 fps+720p@1 fps JPEG snapshot
- 2 megapixels@5 fps JPEG snapshot
- CBR or VBR with the output bit rate ranging from 2 kbit/s to 100 Mbit/s
- Encoding frame rate ranging from 1/16 fps to 30 fps
- Encoding of eight ROIs
- OSD overlaying of eight regions before encoding

Intelligent Video Analysis

- Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis

Video and Graphics Processing

- Video pre-processing, including 3D denoising, image enhancement, and edge enhancement
- Anti-flicker for output videos and graphics
- 1/15x to 16x video scaling
- 1/2x to 2x graphics scaling
- OSD overlaying of eight regions before encoding
- Hardware graphics overlaying for videos at the video layer and graphics layer 1 during post-processing

ISP

- 2x2 Pattern RGB-IR sensor
- Adjustable 3A (AE, AF, and AWB) functions
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoising, and digital image stabilization
- Anti-fog
- Lens distortion correction
- Picture rotation by 90° or 270°
- Mirroring and flipping
- Build-in WDR and tone mapping
- ISP tuning tools for the PC

Audio Encoding/Decoding

- Voice encoding/decoding complying with multiple protocols by using software
- G.711, ADPCM, and G.726 protocols supported
- Echo cancellation, noise suppression, and automatic gain

Security Engine

- AES, DES, 3DES, and RSA encryption/decryption algorithms implemented by hardware
- Hash digest tamper proofing implemented by hardware
- Integrated 512-bit OTP storage space and hardware random number generator

Video Interfaces

- VI interfaces
  - 8-, 10-, 12-, or 14-bit RGB Bayer/RGB-IR inputs, maximum clock frequency of 100 MHz
  - BT.601, BT.656, and BT.1120 VI interfaces
  - 4-Lane MIPI/HiSPI/LVDS VI interfaces
  - Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, OmniVision, and Panasonic
  - Various sensor levels supported
  - Programmable sensor clock output
  - Maximum input resolution of 2 (1920*1080) megapixels
- VO interfaces
  - One BT.656 VO interface supporting 8-bit serial LCD outputs

Audio Interfaces

- Integrated audio CODEC that supports 16-bit audio inputs and outputs
- Mono-channel differential microphone inputs for reducing the background noises
- I^2S input

Peripheral Interfaces

- POR
- One integrated high-precision RTC
- One 4-channel SAR ADC
- Three UART interfaces
- IR interfaces, I^2C interfaces, SPI master interfaces, and GPIO interfaces
- Four PWM interfaces
- Two SDIO interfaces, one of which supports SD 3.0
- One USB 2.0 interface that supports the host/device mode
- RMII in 10/100 Mbit/s full-duplex or half-duplex mode, TSO network acceleration, and PHY clock output

External Memory Interfaces

- DDR2 SDRAM interface
  - Embedded 512 Mbits, 16-bit DDR2 SDRAM
  - Maximum frequency of 360 MHz
- SPI NOR flash interface
  - 1-, 2-, or 4-bit SPI NOR flash interface
- SPI NAND flash interface
  - Maximum capacity of 4 Gbits
- eMMC 5.0 interface
  - Maximum capacity of 64 GB
- Booting from the SPI NOR flash, SPI NAND flash, or eMMC

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SDK

- Linux 3.4-based SDK
- High-performance H.264 PC decoding library

Physical Specifications

- Power consumption
  - Typical power consumption of 700 mW (including DDR2 SDRAM)
  - Multi-level power saving mode
- Operating voltages
  - 1.1 V core voltage
  - 3.3 V I/O voltage and 3.8 V margin voltage
- Package
  - Body size of 10 mm x 10 mm (0.39 in. x 0.39 in.), 0.65 mm (0.03 in.) ball pitch, TFBGA RoHS package with 192 pins

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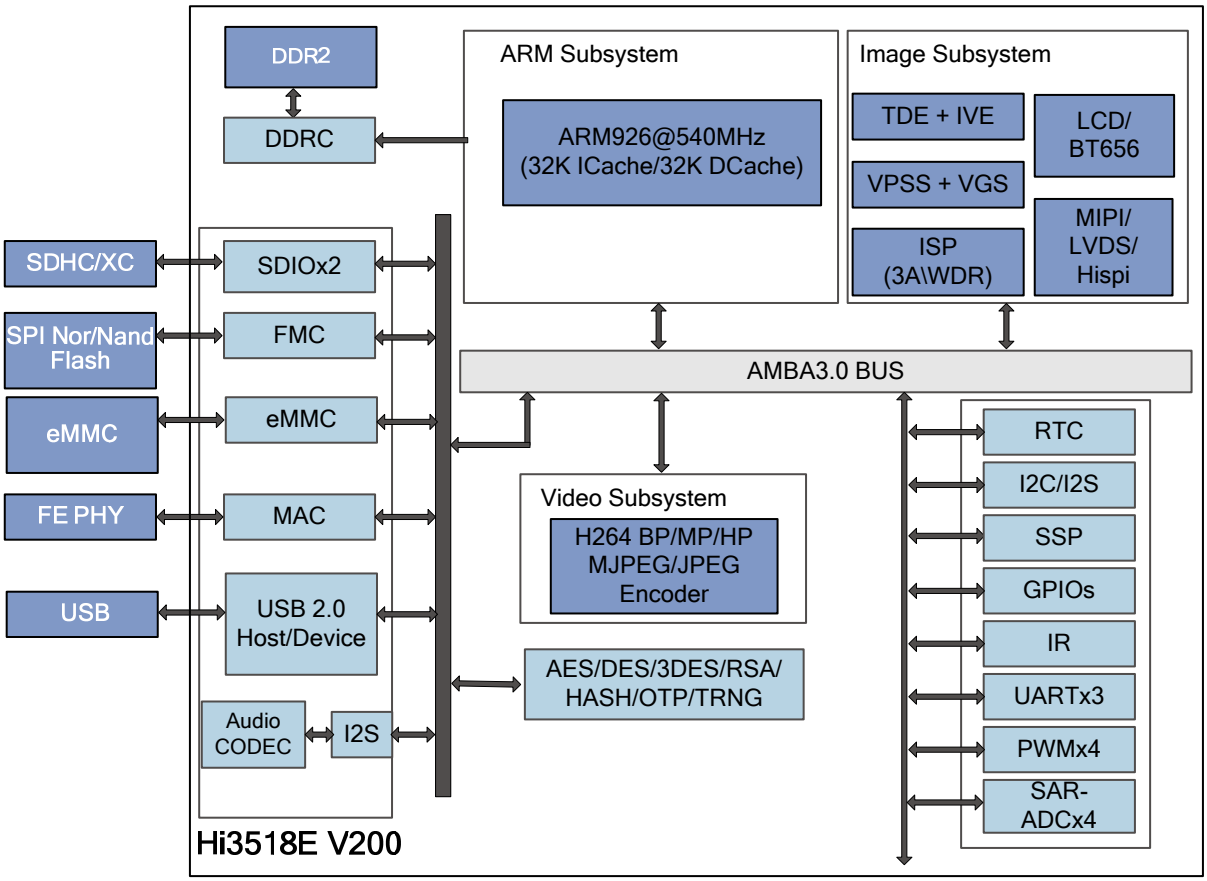
Functional Block Diagram



Hi3518E V200 is a new-generation SoC designed for the HD IP camera. It has an integrated new-generation ISP and H.264 encoder. It uses the optimized picture processing algorithm before encoding, advanced low-power technology, and low-power architecture design. These designs and functions enable Hi3518E V200 to feature industry-leading low bit rate, high picture quality, and low power consumption. It supports 90° or 270° rotation and lens distortion correction by using hardware, which meets requirements in various surveillance application scenarios. It also supports 3A algorithms, which allow customers to design various types of IP cameras including the movement of the integrated camera. Hi3518E V200 integrates the POR, RTC as well as audio CODEC and supports various sensor levels and clock outputs, which significantly reduces the EBOM costs for the Hi3518E V200 HD IP camera. Similar to other HiSilicon DVR and NVR SDKs, the Hi3518E V200 SDK supports rapid mass production and the system layout of IP cameras, DVRs, and NVRs.

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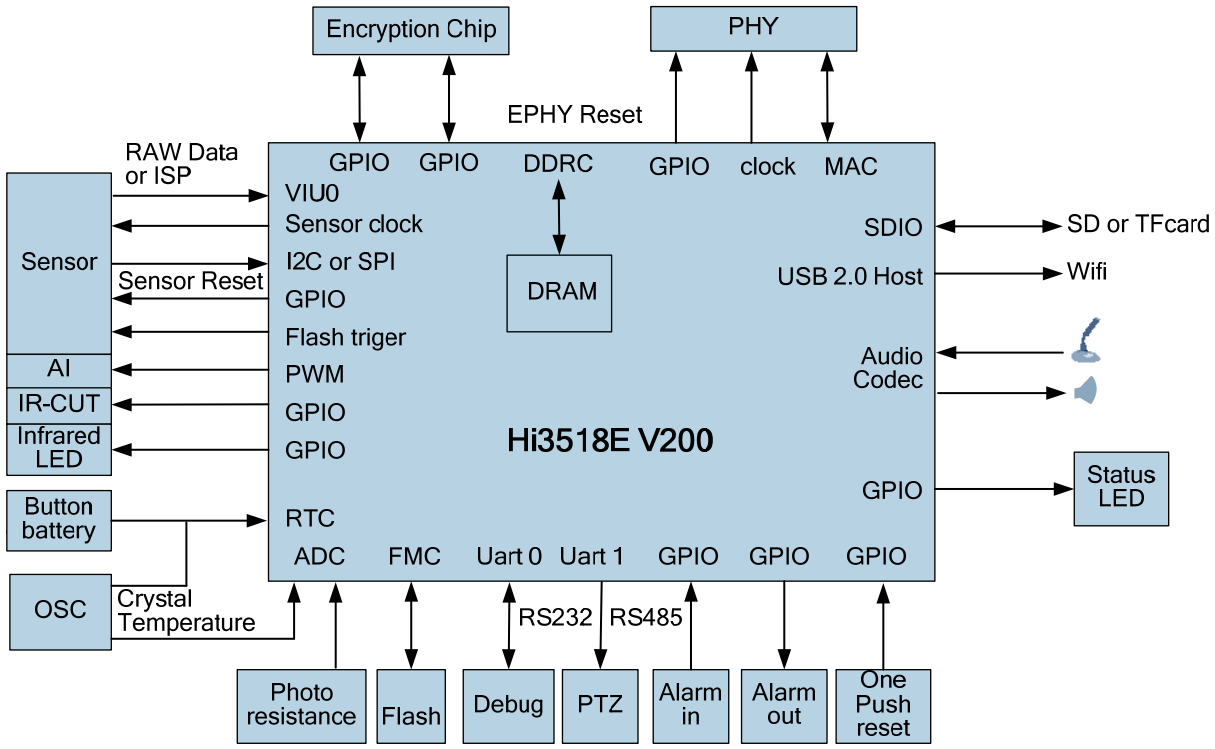
Hi3518E V200 Economical HD IP Camera Solution



Acronyms and Abbreviations

3DES	triple data encryption standard
ADPCM	adaptive differential pulse code modulation
AE	automatic exposure
AES	advanced encryption standard
AF	automatic focus
AWB	automatic white balance
CBR	constant bit rate
CODEC	coder/decoder
DDR	double data rate
DES	data encryption standard
DVR	digital video recorder
EBOM	engineering bill of materials
eMMC	embedded multimedia card
GPIO	general-purpose input/output
HD	high definition
HiSPI	high-speed serial pixel interface
I^2C	inter-integrated circuit
I^2S	inter-IC sound
IR	infrared
ISP	image signal processor
IVE	intelligent video engine
LCD	liquid crystal display
LVDS	low-voltage differential signaling
MIPI	mobile industry processor interface
NVR	network video recorder
OSD	on-screen display
OTP	one-time programming
POR	power-on reset
PWM	pulse-width modulation

RGB	red-green-blue
RMII	reduced media independent interface
RoHS	Restriction of Hazardous Substances
ROI	region of interest
RSA	Rivest-Shamir-Adleman
RTC	real-time clock
SAR ADC	successive approximation register analog-to-digital converter
SDIO	secure digital input/output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SoC	system-on-chip
SPI	serial peripheral interface
TFBGA	thin & fine-pitch ball grid array
TSO	TCP segmentation offload
UART	universal asynchronous receiver transmitter
VBR	variable bit rate
VGA	video graphics array
VI	video input
VO	video output
WDR	wide dynamic range