



NTNU
Norwegian University of
Science and Technology

Lecture 6: Energy efficiency and RAM HDL example

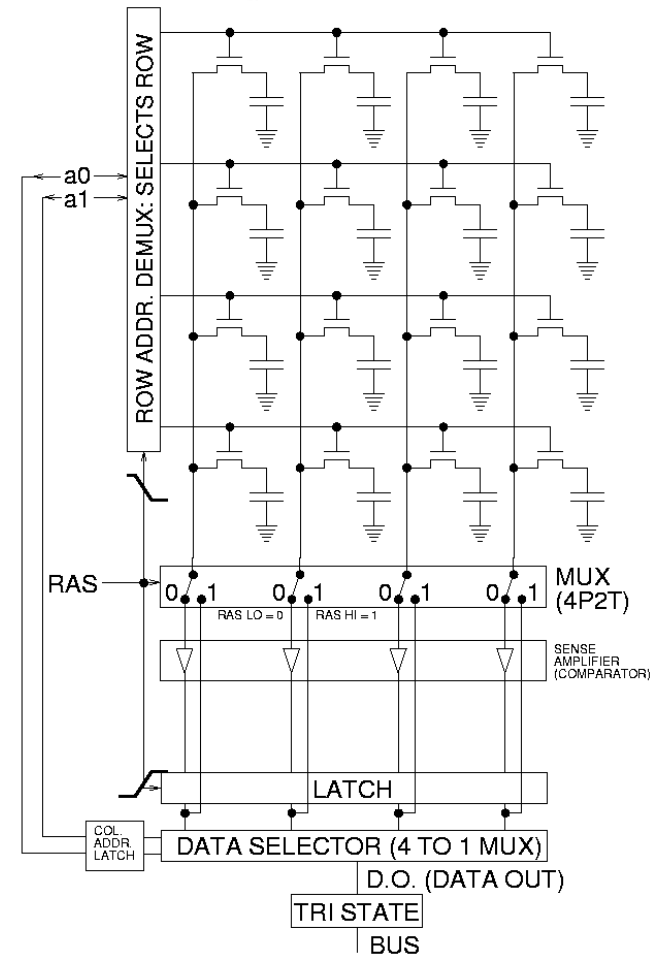
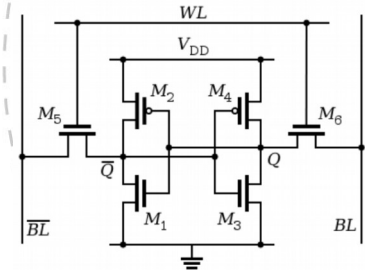
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Question

- What is most energy efficient, SRAM or DRAM?

DRAM vs SRAM

- DRAM cells:
 - Capacitor
 - Access transistor
- SRAM cells
 - 4 transistors (two inverters)
 - 2 access transistors
- Both arranged in arrays, with bitlines and sense amplifiers
- DRAM read is destructive, sense amplifiers must refresh row capacitors for every read
- All DRAM cells must be refreshed periodically



CACTI

- CACTI: Cache and memory model from HP labs
 - power model, leakage, access time, area, ...
- Used for researching memory system tradeoffs
- Available as C++ code, or through a web interface
 - <http://www.hpl.hp.com/research/cacti/>

CACTI results

- Two similar 64kB RAM arrays, DRAM and SRAM
- 32nm:
 - Dynamic energy per read: SRAM uses 50.8% of DRAM
 - 4.39pJ vs 8.64pJ
 - Power at max frequency: 12mW vs 13mW
 - Total standby leakage power: SRAM uses 7.88 times DRAM
 - 5.75mW vs 0.73mW
- 90nm:
 - Dynamic energy per read: SRAM uses 43% of DRAM
 - Total standby leakage power: SRAM uses 4.5 times DRAM

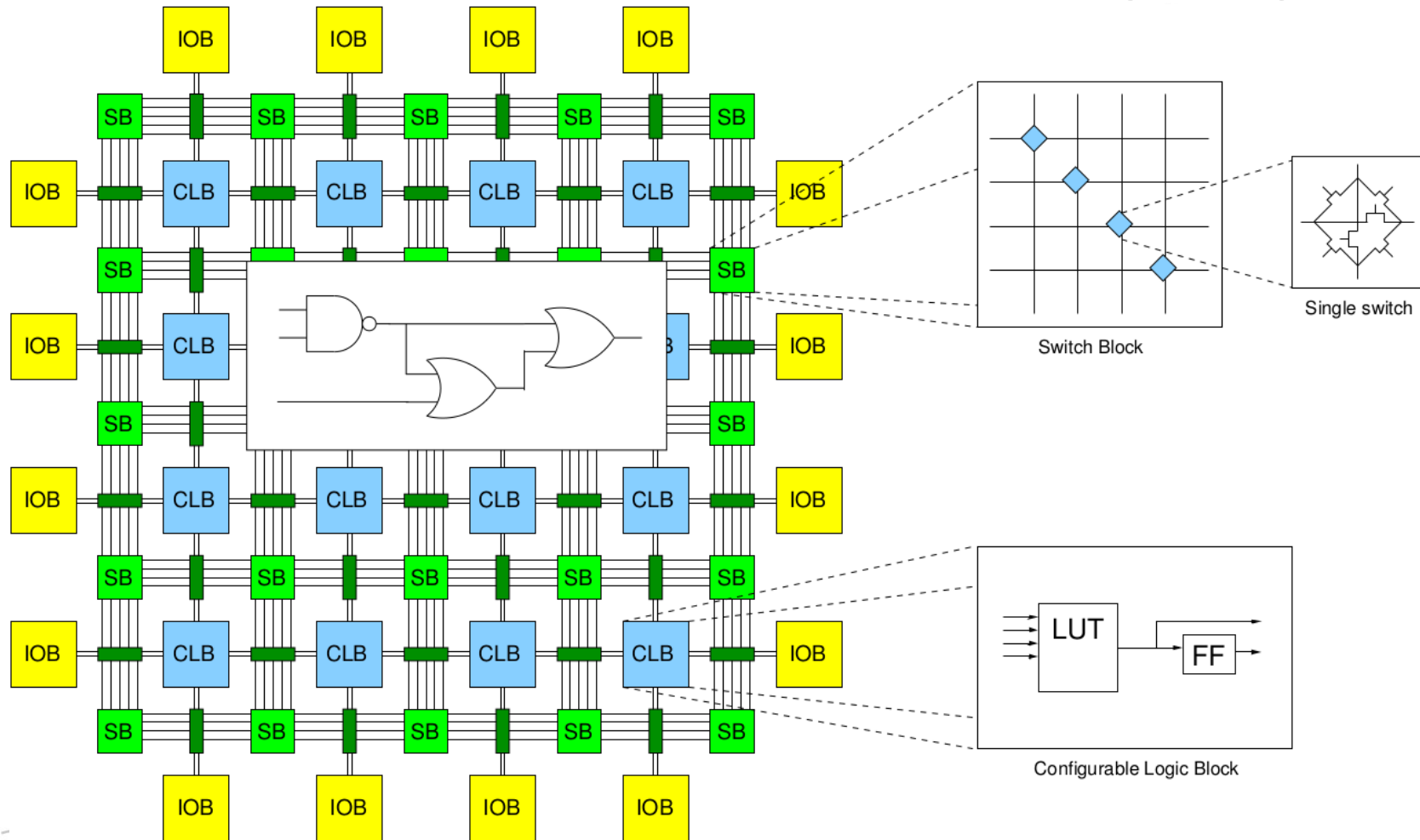
Conclusion

- Answer to question:
 - SRAM idle power much worse than DRAM
 - SRAM read power slightly better than DRAM
- More important: Can you stay on-chip or do you have to go off-chip?
 - CACTI numbers are for on-chip memory
 - Usually cant mix general digital logic with DRAM, SRAM is OK
 - Off chip busses are expensive
 - Conclusion: On-chip SRAM cache just big enough to hold your working set, off-chip DRAM

Question

- What do Hardware Description Languages look like?

Hardware Description Languages



Hardware description language example

- Two main languages:
 - Verilog
 - VHDL
- Both express roughly the same, but with different syntax.