Ultra low voltage CMOS reducing power consumption up to several orders of magnitude, or energy per switching up to 1-2 orders of magnitude
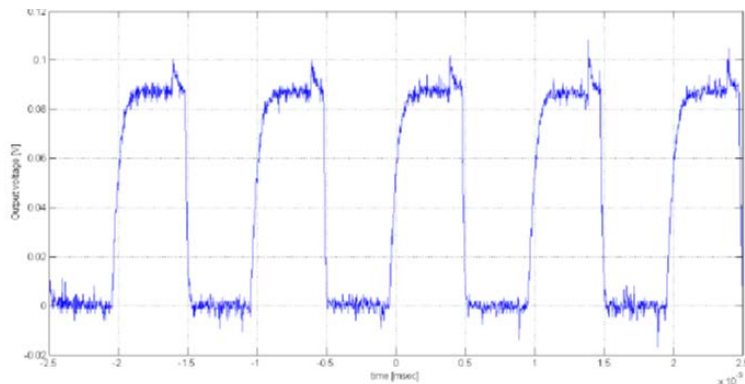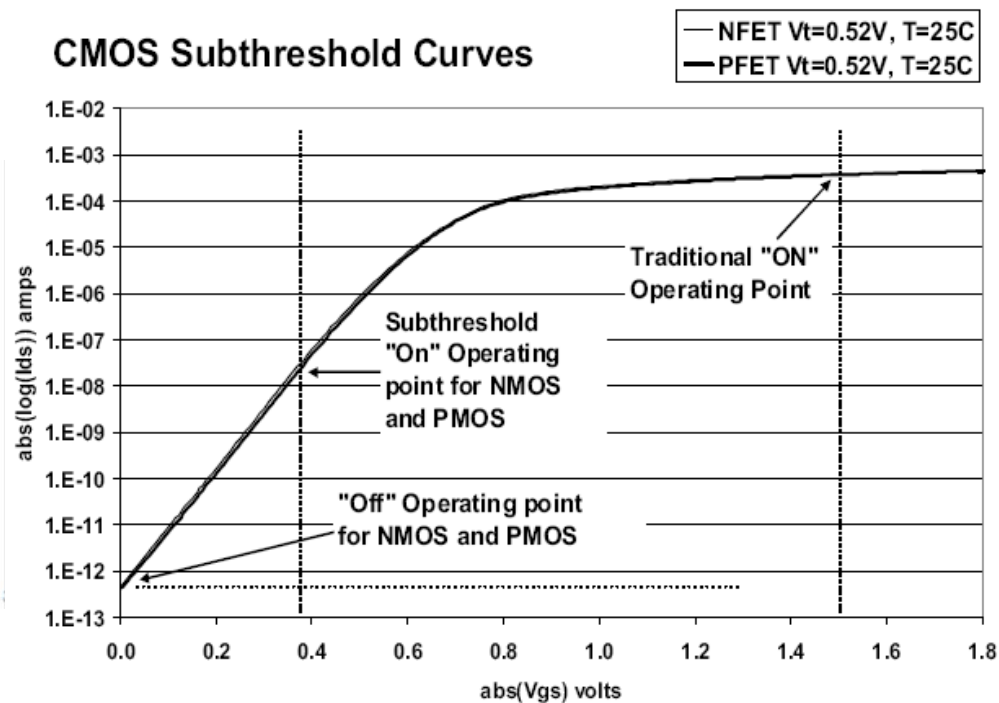
Figure 55: The Serial Adder output at the lowest possible Supply Voltage, 106mV input

CMOS Subthreshold Curves

- NFET Vt=0.52V, T=25C
- PFET Vt=0.52V, T=25C

Traditional "ON" Operating Point

Subthreshold "On" Operating point for NMOS and PMOS

"Off" Operating point for NMOS and PMOS

abs(Vgs) volts

abs(log(Ids)) amps

Department of Information and Computer Science, NTNU, 2013.02.28

Snorre Aunet, Department of Electronics and Telecommunications, NTNU /

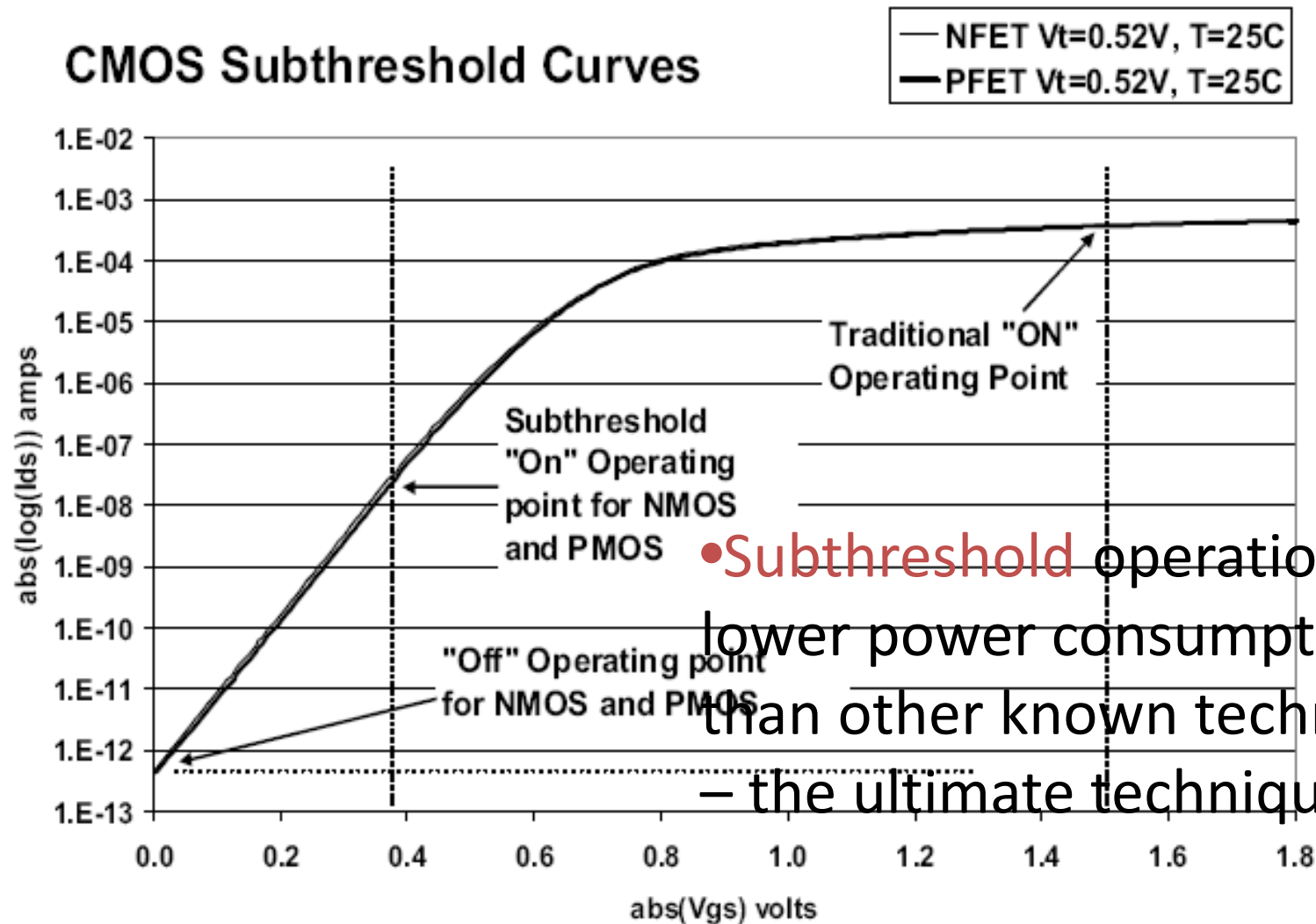Department of informatics, University of Oslo (part time).

aunet@ieee.org / (+47) 90013264

Subthreshold is attained by using a supply voltage below the absolute value of the inherent threshold voltages of the PMOS and NMOS transistors

Vdd

IN

OUT

Gnd
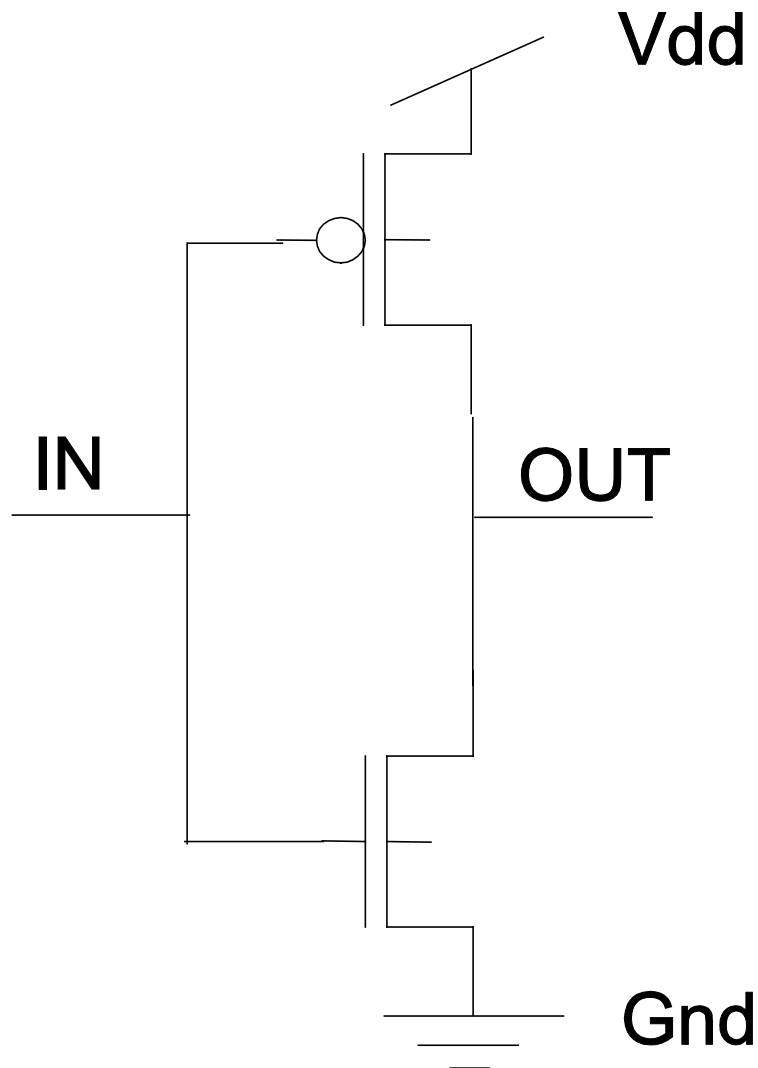
- Normal operation, example: Vtp = -0.3 V, Vtn = 0.3 V. Supply voltage, Vdd = 1.2 V.
- Subthreshold operation, example: |Vtp| = |Vtn| = 0.3 V, Vdd = 0.180 V

- Subthreshold currents may be used for computations in ultra low power / low energy circuits and systems.
- Inverter shown left. OUT = IN'
- ; IN = Vdd → OUT = Gnd.
  IN = Gnd → OUT = Vdd.
  Vdd = «1», Gnd = «0»

CMOS Subthreshold Curves

Legend: NFET Vt=0.52V, T=25C — PFET Vt=0.52V, T=25C

Traditional "ON" Operating Point

Subthreshold "On" Operating point for NMOS and PMOS

"Off" Operating point for NMOS and PMOS

Y-axis: abs(log(Ids)) amps

X-axis: abs(Vgs) volts

- Subthreshold operation: lower power consumption than other known techniques – the ultimate technique

Why low-voltage ("subthreshold" / near threshold) to reduce power- and energy consumption? A few reasons:

- International Technology Roadmap for Semiconductors, Five Crosscutting Challenges for Design technology: 1) design productivity, 2) power management, 3) design for manufacturability, 4) interference and 5) reliability.

- Increasing battery lifetime

- Enabling systems based on very limited energy budget, sometimes based on energy scavenging / energy harvesting (ex. Mobile, battery-powered devices, wireless sensor networks, biomedical applications ..)

- Applications in crypto systems where subthreshold operation may provide improved resistance towards DPA (Differential Power Analysis) Attacks

- Subthreshold operation might work well with certain asynchronous solutions, absorbing worst-case delays accounted for in synchronous counterparts

- Space applications – local low power processing of raw data before transmission

- Innovation - new products

New information acquisition and processing devices enabled by ultra-low power technologies – the sensory swarm

- Sensory swarm «… *will have a tremendous impact in domains such as advanced healthcare, improved energy efficiency, environmentally-friendly living, mobility management, enhanced security, and many others.*»

THE IT PLATFORM OF THE NEXT DECADE(S)

Infrastructural core

Sensory swarm

Mobile access

TRILLIONS OF CONNECTED DEVICES

[J. Rabaey, ASPDAC'08]

The Swarm at the Edge of the Cloud – A New Perspective on Wireless

Jan M. Rabaey

University of California at Berkeley

Intel's top 10 technology predictions for the next decade (''subthreshold'' included in prediction 1 and prediction 6)

Prediction One - new classes of portable devices with ten times more battery life
Sub-threshold integrated circuit technology requires only 300mV to operate.

Intel showed 4-way SIMD (single instruction multiple data) vector processing accelerator in 45nm in CMOS operated below its gate threshold voltage at the ISSCC technology conference.

"This will lead to new classes of portable devices designed to take advantage of greater battery life, which in turn will drive popularity and uptake."

How fast can you design an LED circuit?

National Semiconducto
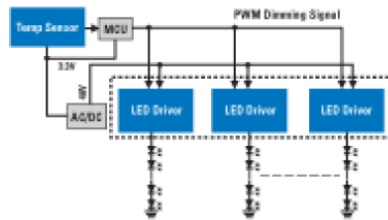
Prediction six - personal internet devices will be truly personal
Mobile internet devices (Mids) are already powerful enough to be useful and the introduction of sub-threshold devices (prediction one) mean these will run all day.

Add this to a continuous Internet connection and users will, for example, be able translate words into other languages and hear then pronounced, or with GPS get a constant geographically-based pollen prediction for that day.

Ten years from now Mids will be ubiquitous and application developers will flood the market with all sorts of ingenious ideas.

- *''Ten years from now Mids will be ubiquitous and application developers will flood the market with all sorts of ingenious ideas''*

- New classes of portable devices with ten times more battery life (prediction 1)
- Personal mobile internet devices (''Mids'') being able to run all day (pred. 6)

Subthreshold CMOS extending the functionality of microwatt (ex: energy scavenging) systems?

A 180-mV Subthreshold FFT Processor Using a Minimum Energy Design Methodology

Alice Wang, *Member, IEEE,* and Anantha Chandrakasan, *Fellow, IEEE*

"Wang" subthreshold FFT (90 nW by 16-b 1024 pt operation @180 mV):

Abstract—In emerging embedded applications such as wireless sensor networks, the key metric is minimizing energy dissipation rather than processor speed. Minimum energy analysis of CMOS circuits estimates the optimal operating point of clock frequencies, supply voltage, and threshold voltage [1]. The minimum energy analysis shows that the optimal power supply typically occurs in subthreshold (e.g., supply voltages are below device thresholds). New subthreshold logic and memory design methodologies are developed and demonstrated on a fast Fourier transform (FFT) processor. The FFT processor uses an energy-aware architecture that allows for variable FFT length (128–1024 point), variable bit-precision (8 b and 16 b) and is designed to investigate the estimated minimum energy point. The FFT processor is fabricated using a standard 0.18-μm CMOS logic process and operates down to 180 mV. The minimum energy point for the 16-b 1024-point FFT processor occurs at 350-mV supply voltage where it dissipates 155 nJ/FFT at a clock frequency of 10 kHz.
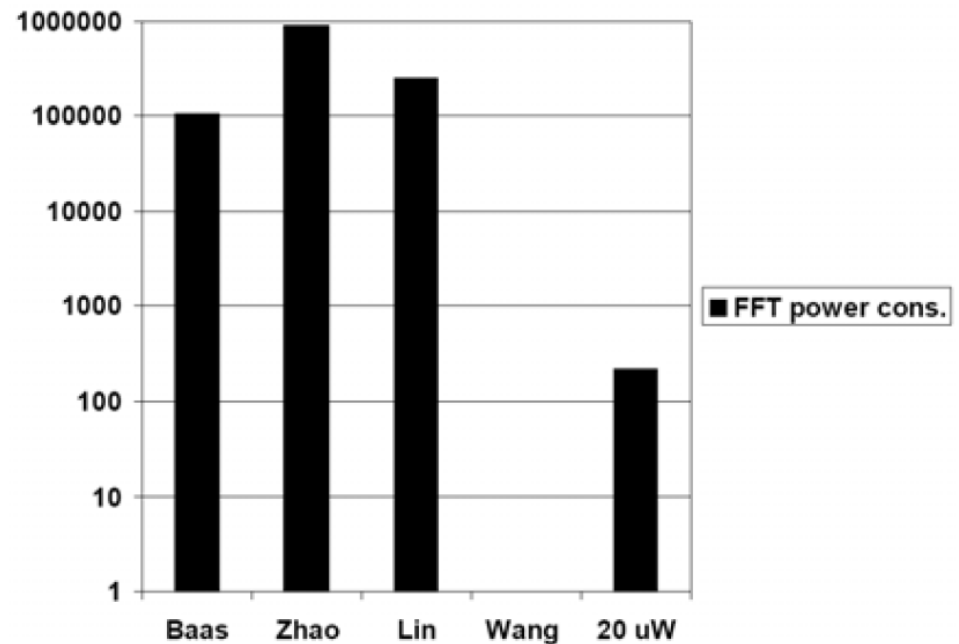

Fig. 1.3 The FFTs in figures 1.1, 1.2 have their relative power consumptions depicted on a logarithmic scale. "Wang" is the only subthreshold FFT. 20 uW, which might be the allowable power consumption for an energy-scavenging system, is shown for comparison.

Ultra Low Voltage processor from IMEC

- **ISSCC: IMEC reports threshold-voltage processor**
- **Peter Clarke**
- **2/21/2013 6:06 AM EST**
-
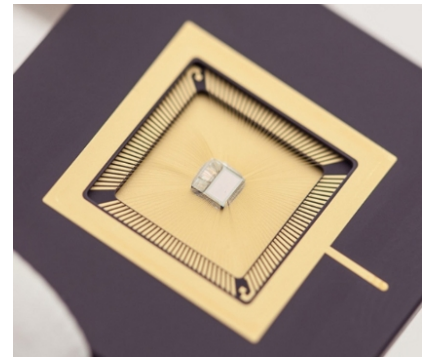
LONDON – Engineers from research institutes IMEC (Leuven, Belgium) and the Holst Center (Eindhoven, The Netherlands) have produced a processor circuit that operates at 0.4 volts.

The processor, designed for use in monitoring of electroencephalograph (EEG) and electrocardiograph (ECG) information operates at close the threshold voltage of the 40nm CMOS process and at clock frequencies of up to 1MHz.

The processor includes nine 32-bit functional unit, from FU0 to FU8, providing inherent scalabilty through the array of dynamically reconfigurable processing units, In tests based on computing Fast Fourier Transforms, IMEC said it consumed 79-microwatts, a fraction of the power consumption at standard voltages.

The architecture of the IC includes a general-purpose processor core to enable ultra-low voltage operation and a system of in-situ monitoring for computational need and automatic scaling of performance.

The ability to maintain reliable operation over a wide range of operating voltages and temperatures was achieved by forward biasing the transistors within the processor, allowing it to operate at voltages just above the threshold for the CMOS process used. The operating voltage can be adjusted between the processor's nominal voltage of 1.1V and a minimum voltage of 0.4V depending on the performance requirements.

The natural variability of manufacturing processes can lead to voltage fluctuations causing such a processor to stop working. To prevent this IMEC/Holst included "canary" flip-flops to the most time-critical parts of the circuit. These are not part of the circuit functionality but are designed to fail before the processor circuit does. By monitoring these "canaries" the operating voltage can be scaled up before noise affects the processor. In addition unused functional units are switched off to reduce power consumption.

Harmke de Groot, ultra-low power program director at Holst, said that much of the industry research is still aimed at improving performance rather increasing energy efficiency. "At Holst Centre, we focus on low power and low voltage to enable battery-powered and energy scavenging smart devices," de Groot said in a statement issued by IMEC.

Reducing the supply voltage into the subthreshold regime may reduce power consumption by several orders of magnitude, or energy per operation by typically 10 to 30 x

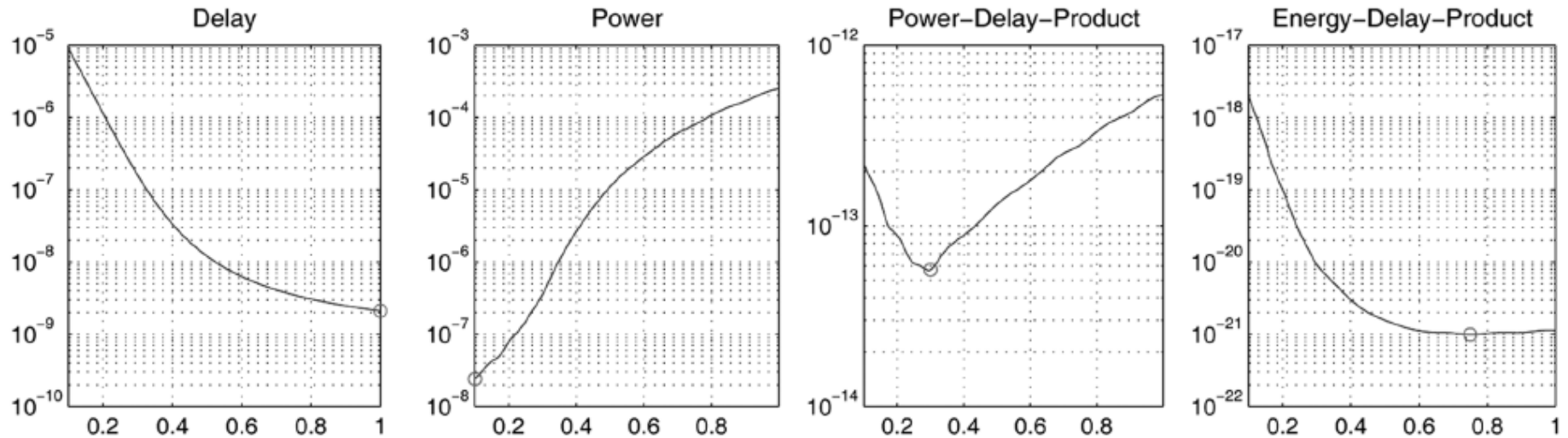Delay | Power | Power-Delay-Product | Energy-Delay-Product

Fig. 10. Effect of varying V_{DD} (32-bit RC) on power, PDP, and EDP

Optimum operating point is marked with a circle.

Serial Addition: Locally Connected Architectures

Valeriu Beiu, *Senior Member, IEEE*, Snorre Aunet, *Senior Member, IEEE*, Jabulani Nyathi, *Member, IEEE*, Robert R. Rydberg III, *Student Member, IEEE*, and Walid Ibrahim, *Member, IEEE*

- $P = P_{static} + P_{dyn} + P_{sc} =$
  $V_{DD}I_{leak} +$
  $\alpha V_{swing}V_{DD}C_L f_{CLK}$
  $+ I_{sc}V_{DD}$

Power = Voltage x Current
Energy = Power x Delay
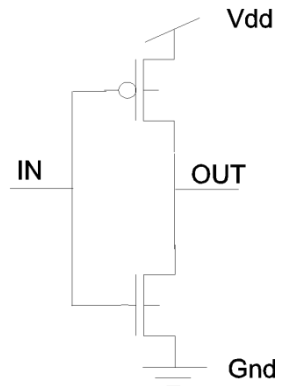
General signal processing system exploiting low-voltage signal processing for some parts
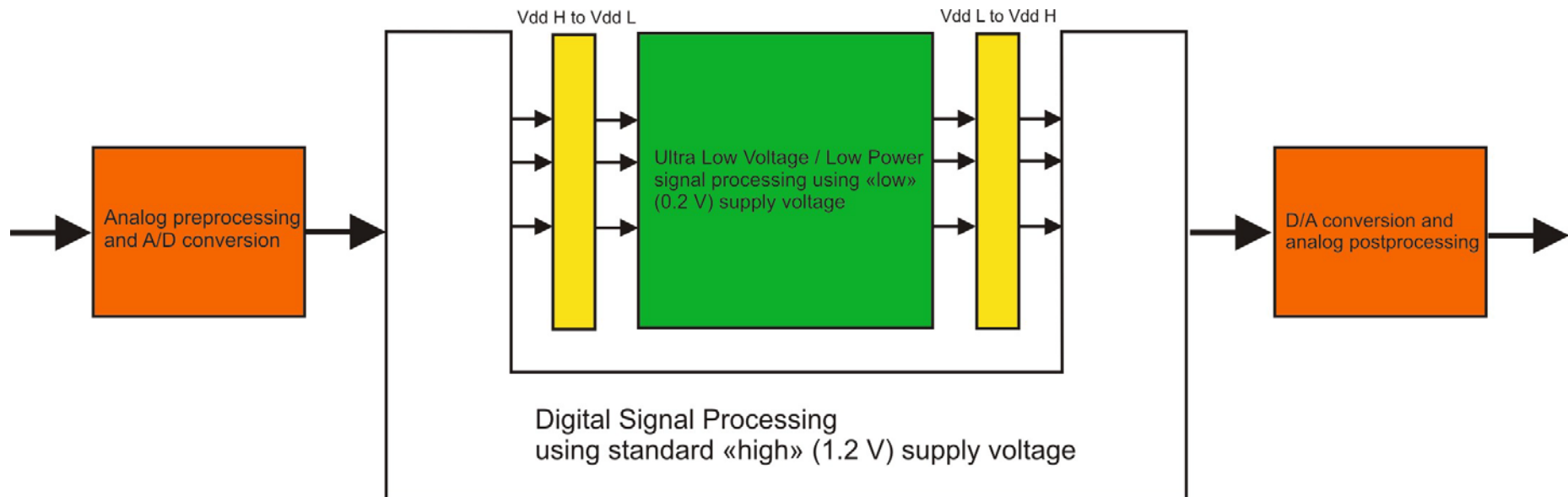
For a general digital system, or "Finite State Machine": combinatorial circuits + memory including for example nand, nor, inv, buf, exor, exnor, and, or and D flip-flop's and SRAM

Chip measurements, 32-bit addition, Vdd = 106-600 mV (90 nm CMOS)
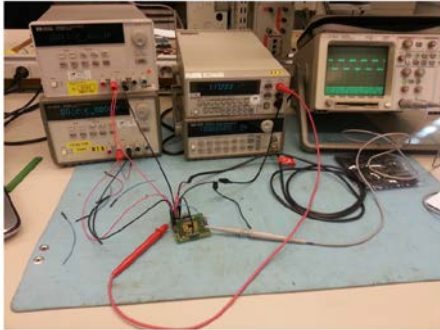

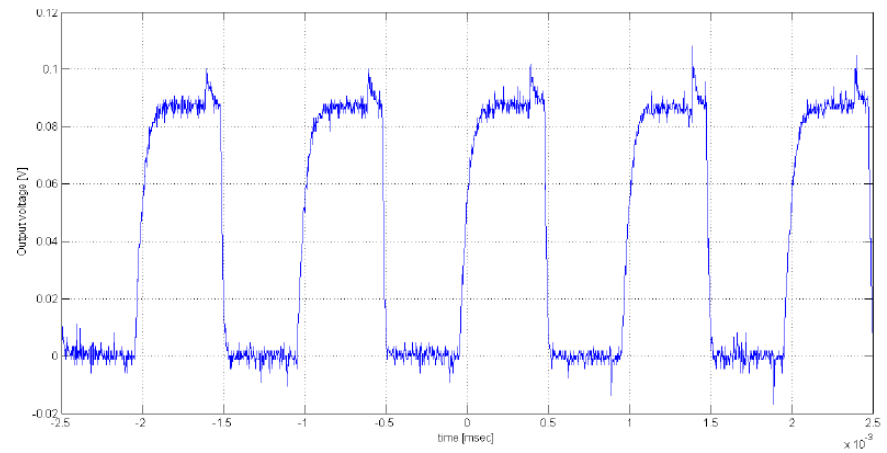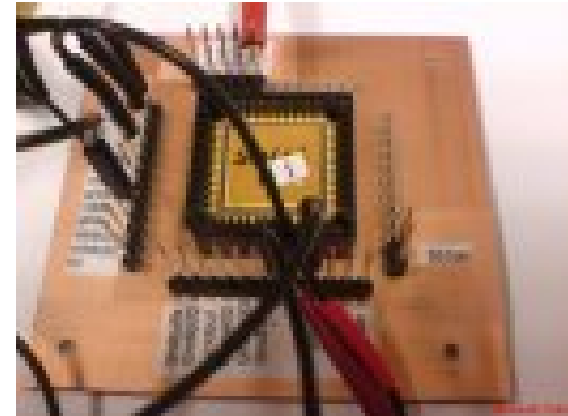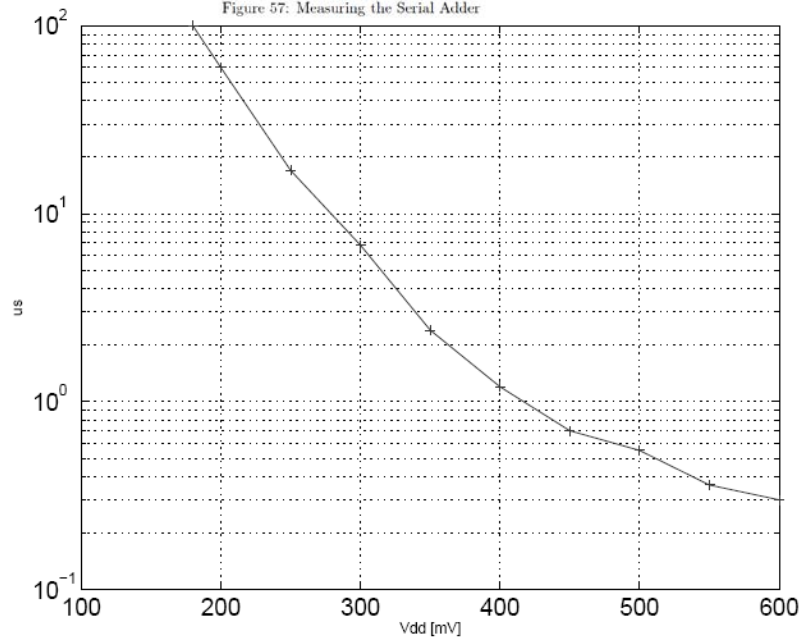Figure 57: Measuring the Serial Adder

Figure 55: The Serial Adder output at the lowest possible Supply Voltage, 106mV input

14. Delay, capacitively loaded 32-bit serial adder as a function of V_{dd}.

Measurements for 32-bit serial adder, above (S. A., Norchip 2009)

Upper , right: 32-bit addition CARRY, Vdd = 106 mV (unpublished measurements, Nov. 2012). Thanks to siv. Ing. Student Magne Værnes!

A 65 nm 32 b Subthreshold Processor With 9T Multi-Vt SRAM and Adaptive Supply Voltage Control

Sven Lütkemeier, *Student Member, IEEE*, Thorsten Jungeblut, *Member, IEEE*,
Hans Kristian Otnes Berge, *Student Member, IEEE*, Snorre Aunet, *Senior Member, IEEE*,
Mario Porrmann, *Member, IEEE*, and Ulrich Rückert, *Member, IEEE*

Abstract—An energy-efficient SoC with 32 b subthreshold RISC processor cores, 32 kB conventional cache memory, and 9T ultra-low voltage (ULV) SRAM based on a flexible and extensible architecture was fabricated on a 2.7 mm² test chip in 65 nm low power CMOS. The processor cores are based on a custom standard cell library that was designed using a multiobjective approach to optimize noise margins, switching energy, and propagation delay simultaneously. The cores operate over a supply voltage range from 200 mV (best samples) to 1.2 V with clock frequencies from 10 kHz to 94 MHz at room temperature. The lowest energy consumption per cycle of 9.94 pJ is observed at 325 mV and 133 kHz. A 2 kb ULV SRAM macro achieves minimum energy per operation at averages of 321 mV (0.030 σ/μ), 567 fJ (0.037 σ/μ), and 730 kHz (0.184 σ/μ), for equal number of 32 b read/write operations. The off-chip performance and power management subsystem provides dynamic voltage and frequency scaling (DVFS) combined with an adaptive supply voltage generation for dynamic PVT compensation.
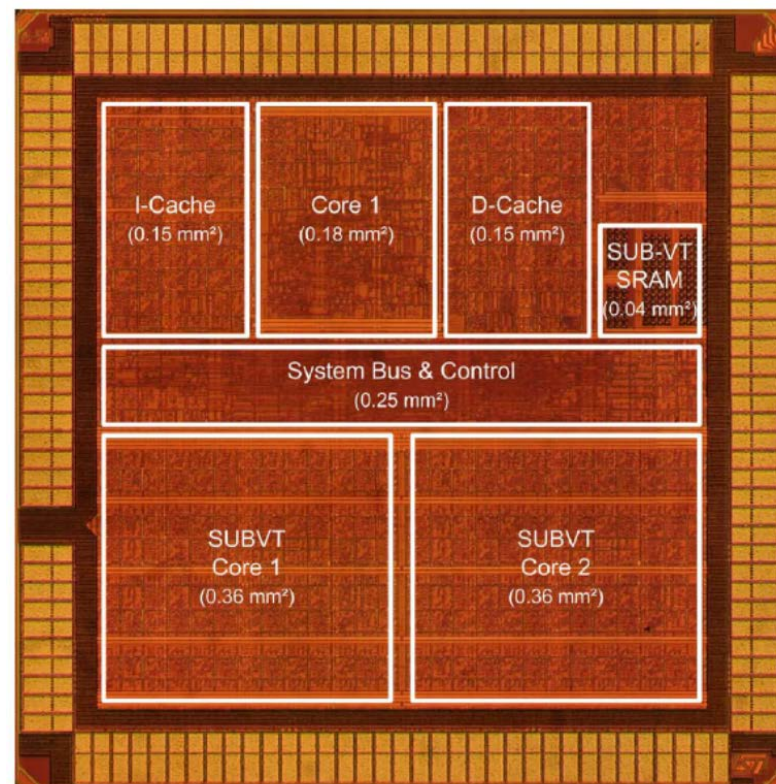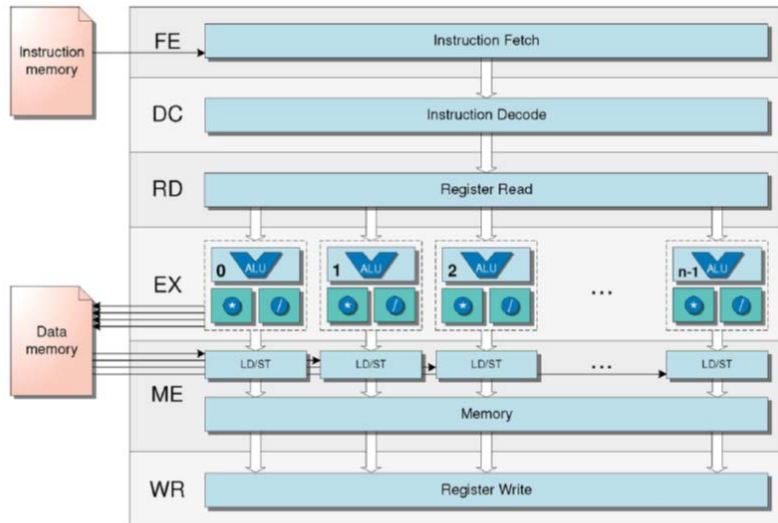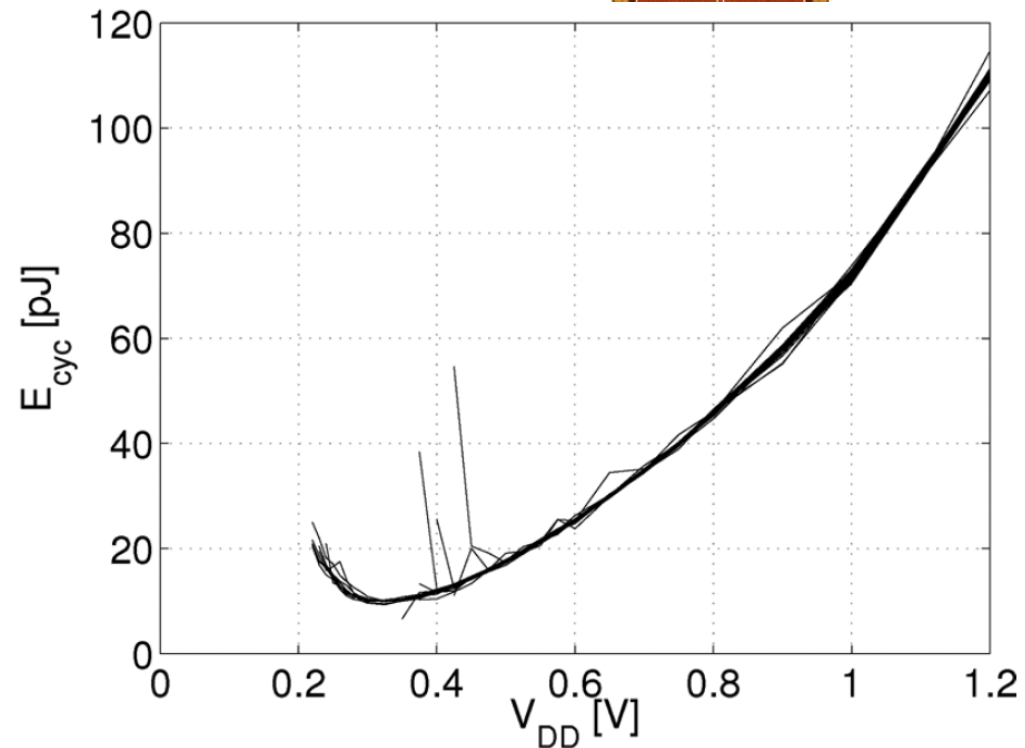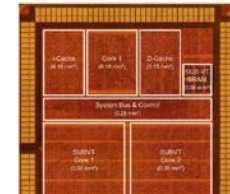
Energy per operation reduced to 1/11 when reducing supply voltage from 1.2 to about 0.3 V, demonstrated by chip measurements (or 90.1 % reduction). Power consumption: 1.32 μW
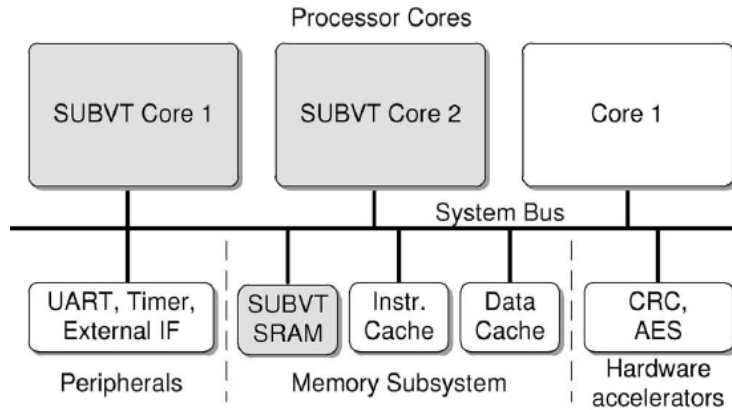
Generic pipeline structure of the CoreVA processor.

Energy per cycle reduced by a factor 8 when reducing Vdd from 1.2 to 0.4 V (Sub-Vt library), and 4.6 times when compared to the standard cell impl. [German fishing trip friends]

Sub-threshold RISC Core
First Results

CoreVA processor
- 32bit VLIW architecture
- highly generic, configurable as a conventional (single slot) 32bit RISC core
- multiobjective-optimized sub-threshold standard cell library in 65nm CMOS (57 cells)
- minimum energy point design approach

Preliminary results

	Sub-Vt CoreVA		„normal" CoreVA
supply voltage	0.4 V	1.2 V	1.2 V
area	0.402 mm²	0.402 mm²	0.203 mm²
clock frequency	1 MHz	97 MHz	250 MHz
total power	36.54 µW	28.29 mW	42.35 mW
leakage power	0.45 µW	0.003 mW	0.27 mW
dynamic power	36.09 µW	28.29 mW	42.08 mW
energy per cycle	36.54 pJ	291.4 pJ	169.4 pJ
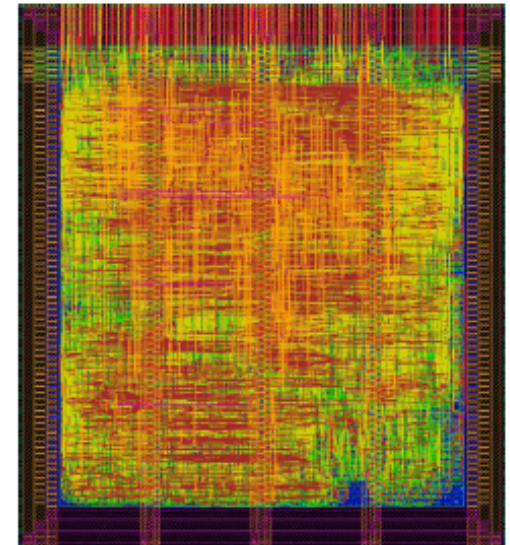
Serial addition for lower Power-Delay-Product, reduced area and increased defect tolerance, especially when combined with redundancy (V. Beiu, A. Djupdal, S. Aunet, «IWANN», 2005)

32-bit parallell and serial adders:
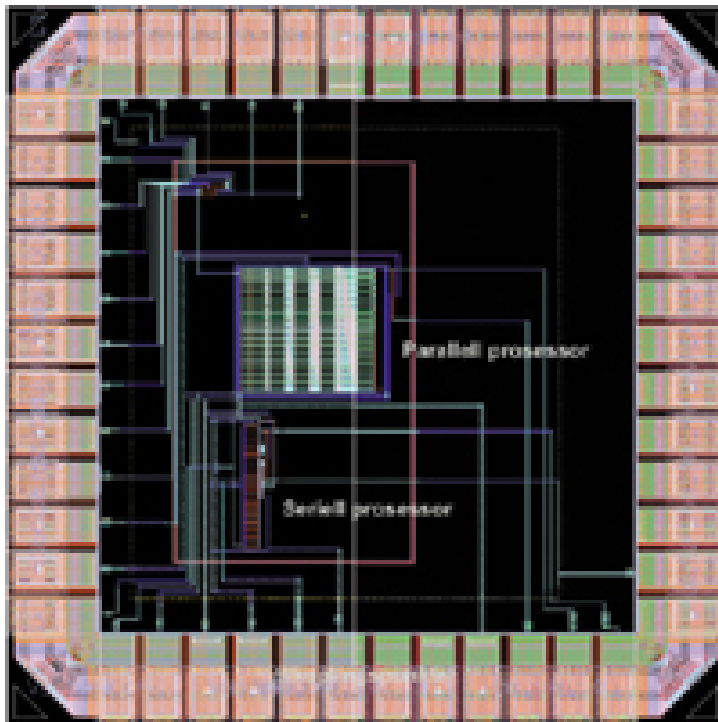
The serial adder uses less energy when maintaining same speed as parallell adder:
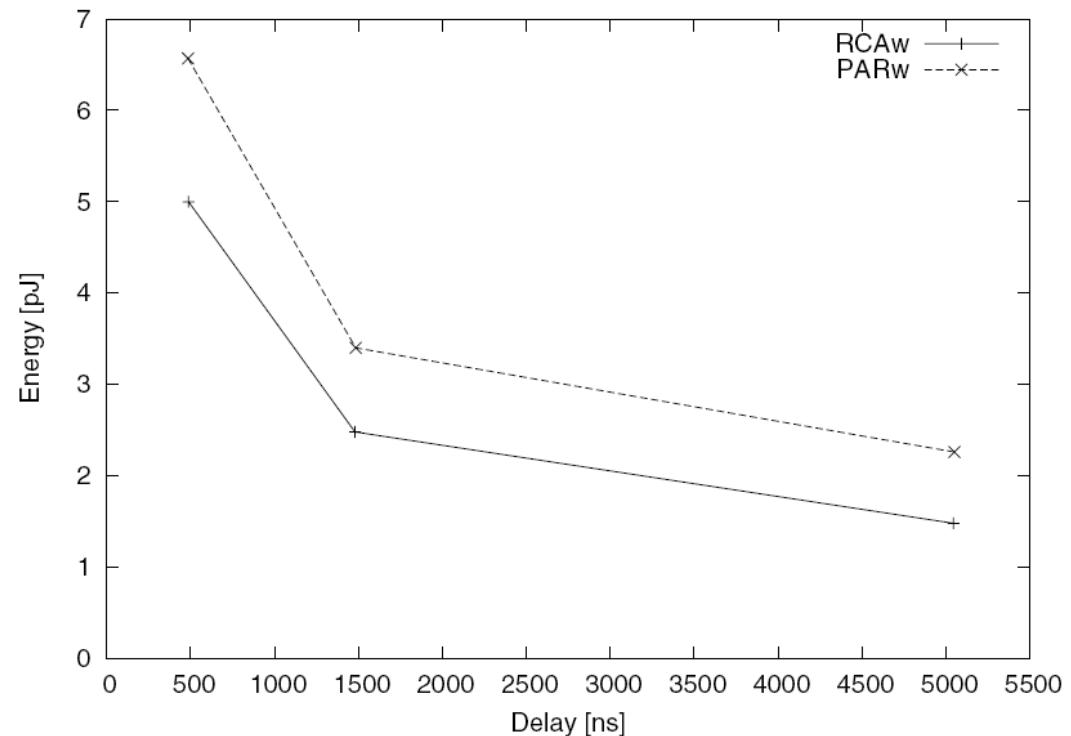
$$I_{ds,n} = I_0 exp\{\frac{\kappa V_{gs}}{V_t}\} exp\{(1-\kappa)\frac{V_{bs}}{V_t}\}(1-exp\{\frac{-V_{ds}}{V_t}\} + \frac{V_{ds}}{V_0})$$

Some considerations to improve yield for subthreshold voltages and process variations

- Choose robust circuit topologies (static CMOS, fan-in limited, flip-flop's that is less prone to produce setup time violations) The basic inverter is a much more robust gate than for example static CMOS NAND..

- Make your own full custom cell library (Standard libraries aimed at strong inversion will be suboptimal) and use Synthesis tools (place and route and timing constraints)

- Increase L, and also W, for symmetry in switching, noise margins etc (RDFs)

- Adjust Vdd to maintain proper operational speed and/or functionality (spec. Latches)

- Substrate biasing

- Serial addition (RCA) will be more energy economic than parallel (ex "Kogge-Stone") in many cases

$$I_{ds,n} = I_0 exp\{\frac{\kappa V_{gs}}{V_t}\} exp\{(1-\kappa)\frac{V_{bs}}{V_t}\}(1 - exp\{\frac{-V_{ds}}{V_t}\} + \frac{V_{ds}}{V_0})$$

Delay variations at three temperatures
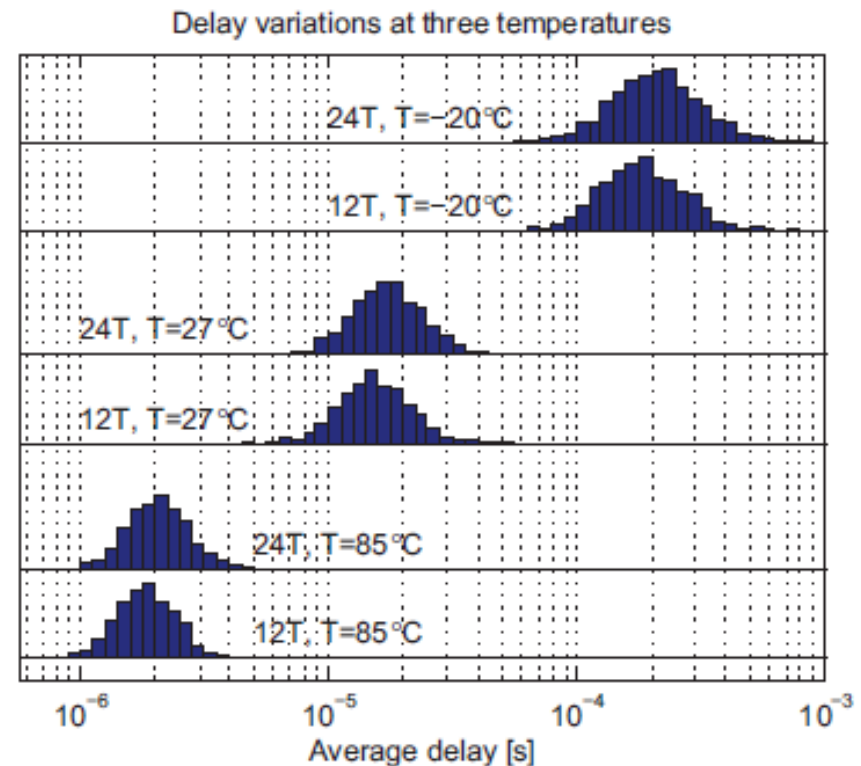

Fig. 6. Delay variations at three temperatures for both the 12T and 24T C-element at $V_{DD} = 150\,mV$

Conclusions

- Subthreshold operation may be combined with other low power techniques and provide the lowest power- and energy consumption attainable

- Main challenges:

- Robustness and good yield accross process and environmental conditions is hard to obtain (, and most often make it impossible to avoid increased transistor dimensions).

- Full custom cell libraries should be developed for good design productivity, and included in standard SW tools for synthesis, layout and verification

Some research, teaching and companies within ultra low power / low energy integrated circuits

- MIT (Massachusetts Institute of Technology) Sub-threshold Circuits Group:
  http://www-mtl.mit.edu/researchgroups/icsystems/stcg/
- University of Michigan, Integrated Circuits and VLSI Design: http://blaauw.eecs.umich.edu/
- University of Oslo, Department of informatics, Nanoelectronics group: http://www.mn.uio.no/ifi/forskning/grupper/nano/index.html
- NTNU, Department of Electronics and Telecommunications, Circuits and Systems group: http://www.iet.ntnu.no/en/groups/cas
- Iridium Technologies, LLC: http://iridiumtec.com/
- Ambiq Micro: http://www.ambiqmicro.com/

Thank you for your attention!

Questions?

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- http://www.iet.ntnu.no/nb/ansatte/krets_og_system
- http://www.mn.uio.no/ifi/personer/vit/sa/index.html

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- +47 90013264 (mob.)

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- [Steve Bush:](#) **Intel makes its top ten technology predictions for next decade** http://www.electronicsweekly.com/Articles/2009/05/13/45950/intel-makes-its-top-ten-technology-predictions-for-next-decade.htm
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- Jan Rabaey: **Exploring the boundaries of ultra low power design – microscopic wireless**, talk at Lund Circuit Design Workshop, Lund, Sweden, Sept. 9-10, 2009.
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- S. Luetkemeier, T. Jungeblut, M. Porrmann, U. Rueckert: **A 200mV 32b Subthreshold Processor with Adaptive Supply Voltage Control,** IEEE International Solid State Circuits Conference («ISSCC») , San Francisco, CA, February 20-23, 2012.
- S. Luetkemeier, H. K. O. Berge, S. Aunet, M. Porrmann U. Rueckert: **A 65 nm 32 b Subthreshold Processor With 9T Multi-Vt SRAM and Adaptive Supply Voltage Control**, IEEE Journal of Solid-State Circuits, Jan. 2013.
- H. K. O. Berge, A. Hasanbegovic, S. Aunet : **Muller C-elements based on Minority-3 Functions for Ultra Low Voltage Supplies**, IEEE DDECS, Cottbus, Germany, 2011.
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