Gaohan (Elijah) Ye

Latest Update: 09/29/2025

CONTACT

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TECHNICAL SKILLS

Programming: SystemVerilog (Advanced), C/C++ (Advanced), UVM/OVM, Python, CUDA, Assembly (x86, RISC-V)
Hardware Design: RTL Design, CPU Architecture, RISC-V, x86, CXL/PCIe, Cache Design, Pipeline Optimization
Hardware Verification: Design Verification, UVM/OVM, Functional Coverage, System-Level Testing, FuSa Testing
Technologies/Tools: Verdi, VCS, Git, Linux, Intel Extension for PyTorch, Performance Analysis, Intel MLC

WORK EXPERIENCE

Rivian Automotive May 2025 – Aug 2025
Design Verification Intern, Special Project Champaign, IL

- Increased design verification coverage to over 90% via a new, more efficient coverage generation flow
- Enhanced an existing integration test suite, reducing the failure rate from over 40% to less than 5%
- Developed a new system-level test to validate memory access, creating a baseline for future verification tests
- Authored new FuSa tests to validate error injection and interrupt mechanisms for critical components

University of Illinois at Urbana-Champaign Jan 2025 – Current
Teaching Assistant for Digital Systems Laboratory, ECE 385 Champaign, IL

- Evaluated SystemVerilog/FPGA projects and microprocessor system implementations
- Conducted technical demonstrations and assessments of digital circuits, state machines, and SoC designs
- Graded lab reports covering combinational/sequential logic, timing analysis, and hardware-software co-design

Rivian Automotive Apr 2024 – Aug 2024
Design Verification Intern, Special Project Champaign, IL

- Created a performance monitor to track AXI transaction signals to test read and write operation performance
- Increased toggle coverage of chip blocks by creating and implementing new targeted tests
- Conducted system-level verification for the DUT using a custom UVM testbench
- Developed and executed detailed test plans, identifying bugs and successfully debugging and resolving issues

University of Illinois at Urbana-Champaign Jan 2023 – Dec 2024
Teaching Assistant for Computer System Engineering, ECE 391 Champaign, IL

- Led weekly lab and discussion sessions, teaching students about operating system concepts, including process scheduling, virtual memory, file systems, and system call implementation
- Offered comprehensive support to students, addressing inquiries regarding x86, virtual memory, scheduling, file systems, and course materials

- Graded over 300 student assignments and conducted demos of their custom operating systems
- Collaborated with professors in the grading process for midterms and final exams

Headline (a Venture Capital Company based in San Francisco) May 2022 – Aug 2022
Frontend Developer Intern Remote

- Added display features and security auditing in a custom integration with Gmail that exposes several million highly sensitive emails across the organization by relying on Rails backend and React front end
- Implemented internal management tool with React.js; restructured API calls to improve page latency by 30%
- Improved performance of Streak CRM and Gmail integrations by fixing timeout bugs

Publications & Research

"CXL Memory Device Characterization" **2025 (In Progress)**

- Evaluated Samsung CMM-H CXL memory prototype using Intel MLC benchmarking tools
- Compared performance characteristics against internal lab CXL SSD implementations

"Exploiting Intel Advanced Matrix Extensions (AMX) for LLM Inference" **2024**
IEEE Computer Architecture Letters (CAL), 2024, IEEE Best Paper Award
Advisor: *Nam Sung Kim* Dec 2023 – Present

- Contributed to research on Intel Extension for PyTorch utilizing Intel Sapphire Rapids CPU with AMX
- Developed CPU-GPU heterogeneous computing techniques to accelerate Large Language Model inference
- Collaborated with Prof. Nam Sung Kim's research group to advance computational efficiency and speed

Relevant Projects

Multi-stage RISC-V Processor | *SystemVerilog, RISC-V* Sept 2023 – Dec 2023
Course Participant Champaign, IL

- Designed and implemented RV32I processor in SystemVerilog with data & branch hazard detection as team
- Achieved 28.6% frequency increase and 47% cache stall reduction, securing 3rd place among 30 groups
- Applied timing analysis and logic optimization principles for hardware-software co-design

Linux Kernel | *C, x86* Oct 2022 – Dec 2022
Course Participant Champaign, IL

- Created a Linux Kernel featuring 3 terminals and 6 processes
- Implemented read-only File System, Round-Robin Scheduling, 4kB and 4mB Paging
- Successfully handled interrupts, exceptions, and system calls from user programs

FPGA Flappy Bird Game | *SystemVerilog, Python, C* Jan 2022 – May 2022
Course Participant Champaign, IL

- Programmed an FPGA to output a VGA signal to draw game visuals to a monitor
- Enabled keyboard-FPGA communication via SPI to run C-based keyboard drivers on SoC
- Wrote Python scripts to compress PNG format into MIF format to instantiate onto the FPGA on-chip memory

- Implemented state machine in SystemVerilog to animate a walking character depending on keyboard inputs
- Detected collisions between the map and the player with state machine-controlled memory address into ROMs

Education

University of Illinois Urbana-Champaign — Aug 2024 – May 2026
Master of Science, Electrical and Computer Engineering — GPA: 3.83/4.00

University of Illinois Urbana-Champaign — Aug 2020 – Dec 2023
Bachelor of Science, Computer Engineering — GPA: 3.96/4.00

Relevant Coursework
Computer Architecture, SoC/Hardware Design, VLSI System Design (Spring 2026), Network Protocol, Operating System, Data Structure, Algorithm

Awards and Distinctions

IEEE Best Paper Award — **2024**

A.R. "Buck" Knight Scholarship, ECE Department — **Aug 2023**

Oakley Award in Electrical and Computer Engineering — **Mar 2023**

Bradley A. Simmons Memorial Scholarship, ECE Department — **Sep 2022**