Computer-Aided VLSI System Design
Final Project Report

Due Tuesday, Jan. 15, 23:59

Student IDs:R08941044 R09943111

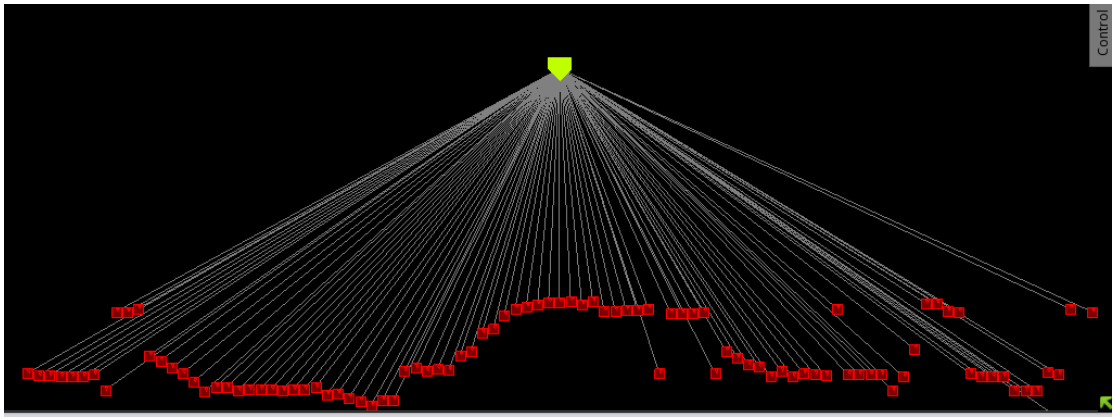
Student Names:卓奕辰 吳宥璁

Questions and Discussion

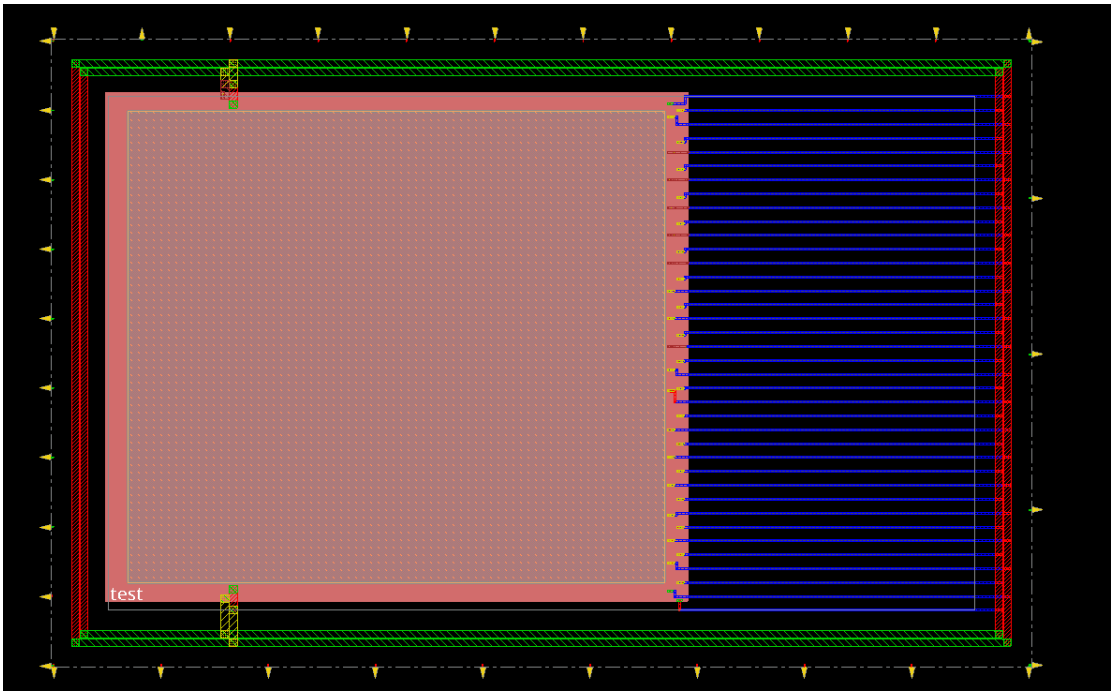
1. Fill in the blanks

Physical category		
Design Stage	Description	Value
Gate-level Simulation	Cycle time for Gate-level Simulation (ex. 10ns)	20ns
P&R	Number of DRC violation (ex: 0) (innovus # > verify_drc)	0
	Number of LVS violation (ex: 0) (Verify -> Verify Connectivity…)	0
	Core area (um^2)	31464.70
	Die area (um^2)	43523.03
Post-layout Simulation	Cycle time for Post-layout Simulation (ex. 10ns)	20ns
	Post-layout Simulation Time for tb0	7863402.485ns
	Post-layout Simulation Time for tb1	10938602.485ns
	Post-layout Simulation Time for tb2	12474602.485ns
	Post-layout Simulation Time for tb3	21050702.485ns
	Post-layout Simulation Time for tb4	25191402.485ns
	Post-layout Simulation Time for tb5	22179302.485ns
	Post-layout Simulation Time for tb6	28689202.485ns

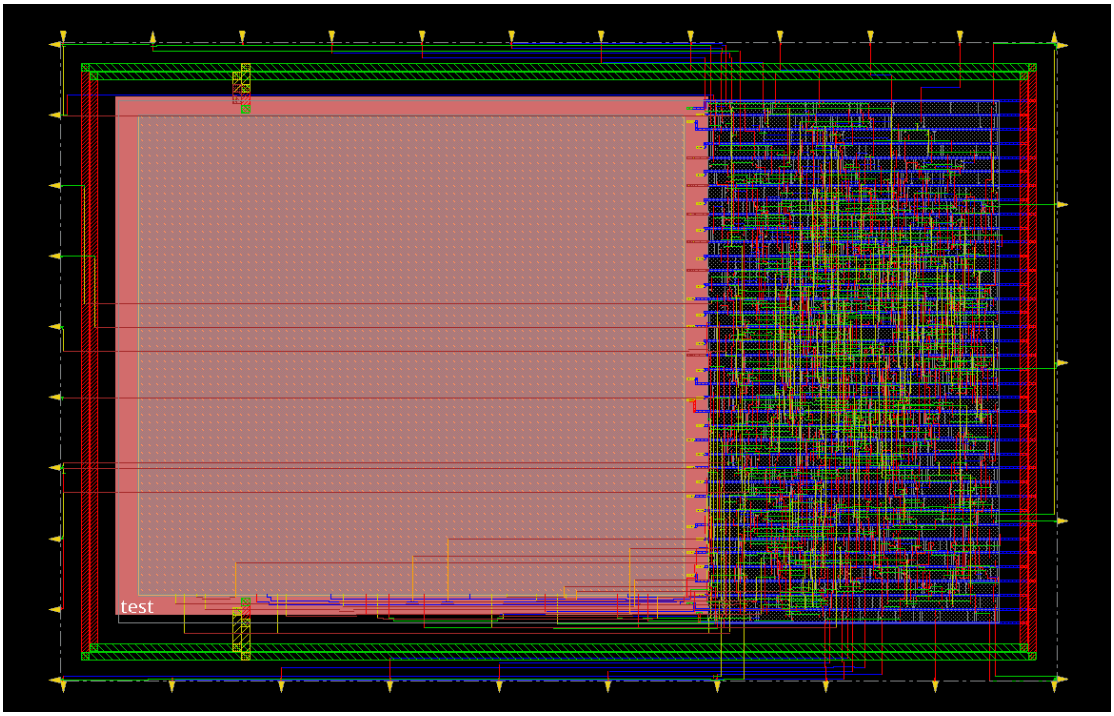
2. Attach the snapshot of CCOpt Clock Tree Debugger result.



3. Attach the snapshot of your final layout in **Floorplan View** after adding core filler.



4. Attach the snapshot of your final layout in **Physical View** after adding core filler.



5. Show one of the critical paths (reg2reg) from setup time analysis after post-route optimization.

```
Clock Rise Edge                     0.000
+ Drive Adjustment                  0.424
+ Source Insertion Delay            0.028
= Beginpoint Arrival Time           0.451
Timing Path:
```

Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk			0.451	13.892
kernel_y_reg_0_/CK	^	clk	DFFRX1	0.029	0.480	13.920
kernel_y_reg_0_/Q	v	kernel_y[0]	DFFRX1	0.608	1.088	14.529
U373/B	v	kernel_y[0]	ADDHXL	0.000	1.088	14.529
U373/CO	v	r489_carry[2]	ADDHXL	0.181	1.269	14.710
U378/B	v	r489_carry[2]	ADDHXL	0.000	1.269	14.710
U378/S	^	N108	ADDHXL	0.227	1.497	14.937
U593/B1	^	N108	OAI22XL	0.000	1.497	14.937
U593/Y	v	n696	OAI22XL	0.255	1.752	15.193
U557/B1	v	n696	OAI22XL	0.000	1.752	15.193
U557/Y	^	n567	OAI22XL	0.566	2.318	15.759
U554/A	^	n567	NAND2X1	0.000	2.318	15.759
U554/Y	v	n703	NAND2X1	0.315	2.633	16.074
U603/A	v	n703	INVXL	0.000	2.633	16.074
U603/Y	^	n576	INVXL	0.310	2.943	16.383
U607/A0	^	n576	AO22X1	0.000	2.943	16.384
U607/Y	^	n577	AO22X1	0.216	3.159	16.599
U608/C0	^	n577	AOI211XL	0.000	3.159	16.599
U608/Y	v	n581	AOI211XL	0.077	3.236	16.677
U610/B0	v	n581	AO22X1	0.000	3.236	16.677
U610/Y	v	n586	AO22X1	0.379	3.615	17.055
U611/A	v	n586	INVXL	0.000	3.615	17.055
U611/Y	^	n588	INVXL	0.184	3.799	17.239
U624/A	^	n588	NAND2XL	0.000	3.799	17.239
U624/Y	v	n591	NAND2XL	0.140	3.938	17.379
U524/B	v	n591	AND2X1	0.000	3.938	17.379
U524/Y	v	n668	AND2X1	0.247	4.185	17.626
U625/B	v	n668	NOR2XL	0.000	4.185	17.626
U625/Y	^	n612	NOR2XL	0.216	4.401	17.842
U665/A	^	n612	NAND2XL	0.000	4.401	17.842
U665/Y	v	n699	NAND2XL	0.158	4.560	18.000
U666/C	v	n699	NAND3XL	0.000	4.560	18.000
U666/Y	^	n620	NAND3XL	0.220	4.779	18.220
U674/C	^	n620	NOR3X1	0.000	4.779	18.220
U674/Y	v	n710	NOR3X1	0.198	4.978	18.418
U675/A	v	n710	INVXL	0.000	4.978	18.418
U675/Y	^	n632	INVXL	0.204	5.182	18.622
U677/B	^	n632	NOR2X1	0.000	5.182	18.622
U677/Y	v	n709	NOR2X1	0.148	5.330	18.771
U687/B1	v	n709	AO22X1	0.000	5.331	18.771
U687/Y	v	n555	AO22X1	0.410	5.740	19.181
U689/A0	v	n555	AOI222XL	0.000	5.740	19.181
U689/Y	^	n634	AOI222XL	0.322	6.062	19.503
U690/A0N	^	n634	AOI2BB2X1	0.000	6.062	19.503
U690/Y	^	n636	AOI2BB2X1	0.181	6.243	19.684
U692/B0	^	n636	OAI211XL	0.000	6.243	19.684
U692/Y	v	rom_a_w[0]	OAI211XL	0.164	6.407	19.848
U738/B1	v	rom_a_w[0]	OA22X1	0.000	6.407	19.848
U738/Y	v	ex_sram_a_w[0]	OA22X1	0.403	6.810	20.250
ex_sram_a_reg_0_/D	v	ex_sram_a_w[0]	DFFRX1	0.000	6.810	20.250

6. Attach the snapshot of timing report for setup time with no timing violation (post-route).

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):| 13.440  | 13.440  | 17.670  | 13.448  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   235   |   104   |   104   |   27    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000     |      1 (96)      |
|   max_fanout   |      0 (0)       |     0       |      1 (1)       |
|   max_length   |      0 (0)       |     0       |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 52.947%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

7. Attach the snapshot of timing report for hold time with no timing violation (post-route).

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.378  |  0.378  |  0.894  |  1.932  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   235   |   104   |   104   |   27    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 52.947%
       (100.000% with Fillers)
```

8. Attach the snapshot of DRC checking after routing (from verify_drc).

```
innovus 31> verify_drc
 *** Starting Verify DRC (MEM: 1856.8) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 130.560 166.870} 1 of 2
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {130.560 0.000 260.820 166.870} 2 of 2
  VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.2  ELAPSED TIME: 0.00  MEM: 13.1M) ***
```

9. Attach the snapshot of LVS checking after routing.

```
innovus 32> VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Fri Jan 15 20:12:36 2021

Design Name: CLE
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (260.8200, 166.8700)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Jan 15 20:12:36 2021
Time Elapsed: 0:00:00.0
```

10. Attach the snapshot of final area result.

```
Finished collecting the design information.
************************** Analyze Floorplan ***************************
    Die Area(um^2)             : 43523.03
    Core Area(um^2)            : 31464.70
    Chip Density (Counting Std Cells and MACROs and IOs): 65.109%
    Core Density (Counting Std Cells and MACROs): 90.061%
    Average utilization        : 147.565%
    Number of instance(s)      : 1017
    Number of Macro(s)         : 1
    Number of IO Pin(s)        : 37
    Number of Power Domain(s) : 0
************************** Estimation Results **************************
************************************************************************
```

11. If there is any feature in your design, please specify it. (5pts)

    Use one sram to store the search stamp on each pixel, and only store current label. Until all pixels with current label are marked, move on next label.

    Use time-consuming method to get smaller area.