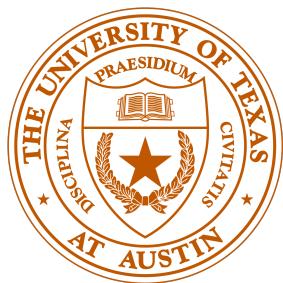


UNIVERSITY OF TEXAS AT AUSTIN, ECE 394J

Control of Power Electronics

Instructor: Dr. BRIAN JOHNSON



Cuauhtemoc Macias, Elijah Macias

Spring 2024

Contents

1 First Milestone	3
1.1 DC-DC Stage Design	3
1.1.1 Current Ripple	3
1.1.2 Switches and Switching Frequency Selection	3
1.1.3 Inductor Design	7
1.1.4 Capacitance Calculations	8
1.1.5 Parameter Table	9
1.2 Board Layout Procedure	9
1.2.1 Switching Loop	10
1.2.2 Gating Loop	11
1.2.3 Capacitive Coupling	13
1.2.4 Thermal Considerations	14
1.2.5 Board Overview	14

1 First Milestone

1.1 DC-DC Stage Design

The first milestone of this project is designing the hardware that will deliver power from our battery to the rear hub motor. This includes fully designing and laying out the DC-DC boost converter stage for our PCB, laying out the digital and analog traces that our digital controller will interface with, and the auxiliary/peripheral components of the integrated power module that will invert the DC power for the motor. After this milestone, we will have fully designed the hardware portion of this project.

In this section we will determine the most critical parameters of our DC-DC converter, including switching frequency, intended current and voltage ripple, and our custom magnetic component. This section will also cover the reasoning behind our design decisions and the constraints that informed these decisions. All derived and chosen parameters of our converter are summarized at the end of this section.

1.1.1 Current Ripple

Our first step in designing this converter is to select our intended current ripple. We are most comfortable designing for a saturation limited converter as this ensures we won't ever reach inductor saturation at full load, and thus picked a smaller ripple to achieve this. To this end, we settled on a 30% inductor current ripple.

1.1.2 Switches and Switching Frequency Selection

Next, we had to determine our switching frequency which was informed by the loss budget that we had chosen for our converter. Considering that our converter's full rated load is intended to be 250 Watts, we chose a loss budget of no more than 1% since this already represents a few watts, which is heuristically known to be the most amount of heat a single switch can bear with a proper thermal management solution. It is worth noting that this budget of power loss is exclusively for the switches of our converter, specifically in the form of switching and conduction losses, according to the formula:

$$P_{loss} = I_{RMS}^2 R_{on} + 2\tau_{FOM} V_o^2 f_s \frac{1}{R_{on}} \quad (1.1)$$

Where P_{loss} is our intended power budget of 1% (2.5 Watts), I_{RMS} is the full load RMS current, R_{on} is the switch's drain to source resistance, τ_{FOM} is the switch device families' figure of merit, f_s is switching frequency, and V_o^2 is the output voltage of our converter. Switching frequency and τ are both within our control, but the following were our constraints for this project:

Converter Requirements	
Property	Ideal Value
Output Voltage (V_o)	48V
Full RMS Current I_{RMS}	9.57A
Power Loss Budget P_{loss}	2.5W

From equation 1.1 we derived an expression for f_{max} using the values listed in table 1.1.2 and the largest figure of merit τ of the device families that we are most interested in (BSC devices). The derived equation is:

$$f_{max} = \frac{\left(\frac{P_{budget}}{P_o}\right)^2 \left(\frac{V_g}{V_o}\right)^2}{4\tau\left(1 + \left(\frac{R^2}{3}\right)\right)} \quad (1.2)$$

From this equation, and using a FOM of $4.95ps$ we calculated a theoretical maximum switching frequency of about $1.238MHz$. To achieve this switching frequency without exceeding a total power loss of 2.5 Watts, every other component and module of our entire project would need to be 100% efficient. Being that this is unrealistic, we decided to design for a maximum theoretical switching frequency of about $650kHz$. With this in mind, we plotted the power lost in our switches with respect to R_{on} for all of the device families that we were interested in, to determine what the most optimal R_{on} (sweeping from $1\mu\Omega$ to $10m\Omega$) value for each respective device family. This was done for several frequencies within a range of $125kHz$ to $625kHz$. The results of this analysis is shown below.

IQE Family $R_{on,opt}$ and P_{loss}

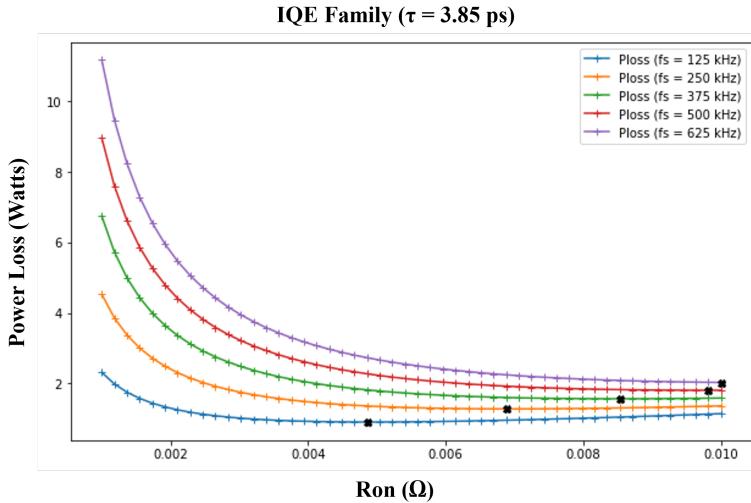
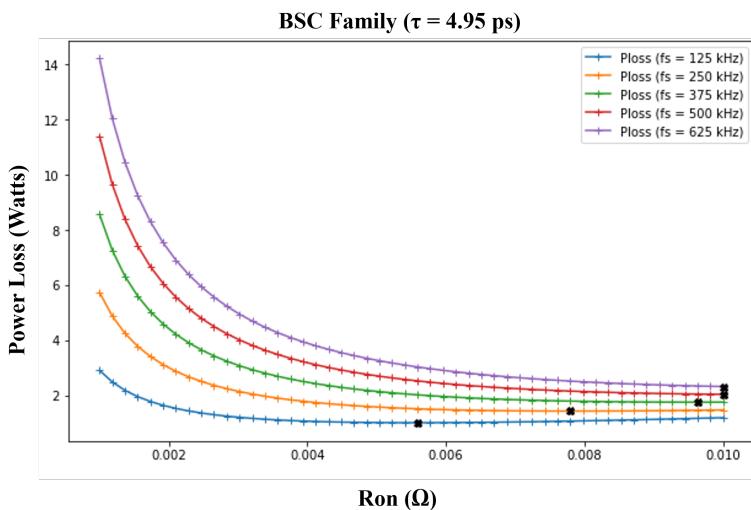
	$f_s = 125kHz$	$f_s = 250kHz$	$f_s = 375kHz$	$f_s = 500kHz$	$f_s = 625kHz$
$R_{on,opt}$	$4.85m\Omega$	$6.87m\Omega$	$8.53m\Omega$	$9.81m\Omega$	$10m\Omega$
P_{loss}	$0.901W$	$1.275W$	$1.562W$	$1.803W$	$2.02W$

Table 1.1: IQE Family Power loss for $R_{on,opt}$ at each switching frequency.

BSC Family $R_{on,opt}$ and P_{loss}

	$f_s = 125kHz$	$f_s = 250kHz$	$f_s = 375kHz$	$f_s = 500kHz$	$f_s = 625kHz$
$R_{on,opt}$	$5.55m\Omega$	$7.79m\Omega$	$9.63m\Omega$	$10m\Omega$	$10m\Omega$
P_{loss}	$1.01W$	$1.43W$	$1.762W$	$2.045W$	$2.328W$

Table 1.2: BSC Family Power loss for $R_{on,opt}$ at each switching frequency.

Figure 1.1: IQE Family R_{opt} sweep for 5 frequencies.Figure 1.2: BSC Family R_{opt} sweep for 5 frequencies.**EPC Family $R_{on,opt}$ and P_{loss}**

	$f_s = 125\text{kHz}$	$f_s = 250\text{kHz}$	$f_s = 375\text{kHz}$	$f_s = 500\text{kHz}$	$f_s = 625\text{kHz}$
$R_{on,opt}$	$5.4m\Omega$	$7.06m\Omega$	$8.71m\Omega$	$10m\Omega$	$10m\Omega$
P_{loss}	$0.924W$	$1.308W$	$1.602W$	$1.85W$	$2.08W$

Table 1.3: EPC Family Power loss for $R_{on,opt}$ at each switching frequency.

From these results we see that switching losses dominate at all frequencies above 125kHz for all

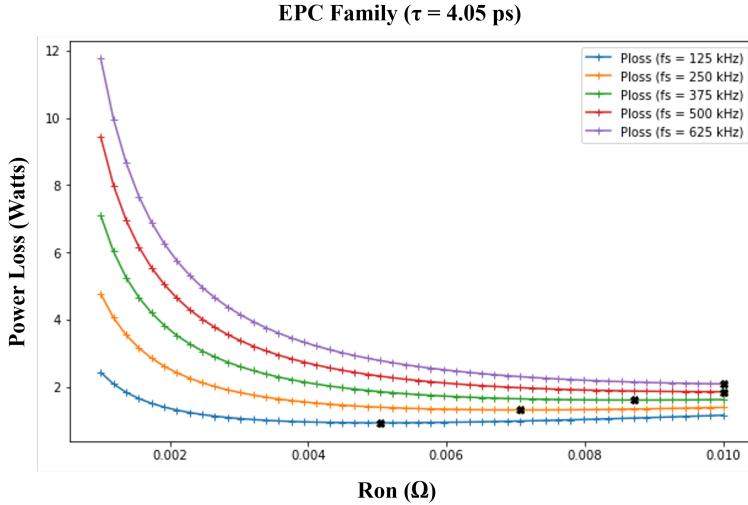


Figure 1.3: EPC Family $R_{on,opt}$ sweep for 5 frequencies.

device families. Upon closer examination we see that all $R_{on,opt}$ values across all device families and frequencies dissipate less power than 2.5W that we are setting as a limit. With this in mind, we decided to pick the highest switching frequency possible. We then looked at the switch device family with the largest figure of merit (BSC), and verified that the R_{on} of the switch we wanted to use would not dissipate more power than we were comfortable managing.

Looking at the BSC028N06NSSC switch we find that a $2.8m\Omega R_{on}$ and a $1750pF C_{oss}$ corresponds to about 3.24W being dissipated for $f_s = 375kHz$. Although this is higher than 1% of the rated power, since this switch has a double sided cooling package, we are confident that an added heat sink will greatly reduce the thermal resistivity of the switch and will allow us to dissipate more power without risking failure.

Having estimated the power loss that the switch will consume and determined this value to be within reason, we were confident that all three devices of interest (EPC 2302, BSC028N06NSSC, and the IQE022N06LM5SC) would be valid options. And since all three switches feature double sided cooling, we know that the switches will be able to dissipate the heat effectively. However, even though the EPC switch has a lower figure of merit than the BSC, it's rated gate voltage of 6V is much lower than the 15V we were planning to use for the IQE switch meaning we would likely need two separate gate drivers. The BSC on the other hand can be driven by the same gate driver as the IQE, and the BSC's package would allow us to greatly reduce the area of the switch node, which tends to be the noisiest node.

Having weighed our options we decided to choose IQE022N06LM5SC as our low side switch, and BSC028N06NSSC as our high side switch and a figure of 375Hz for our switching frequency. With this in mind, we move on to designing the inductor.

1.1.3 Inductor Design

The next step in designing our DC-DC stage is to design an inductor capable of regulating the current that passes through our converter. We first begin by determining the minimum inductance required to achieve volt-second balance which is done by modifying the inductor voltage, which is known to be $V_L = L \frac{di}{dt}$ equation to solve for inductance. By rearranging this equation to find inductance, we find that

$$L_{min} \geq \frac{V_g T_{sw}}{2\Delta i} \quad (1.3)$$

In equation 1.3 we take the voltage across the inductor when the low side (LS) switch is on, that is during the state D, to be V_g . The period of this state is T_{sw} and the total change in current during this state is taken to be $2\Delta i = 2I_{avg}\mathcal{R}$.

Solving 1.3 we find that

$$L_{min} \geq 5.12\mu H \quad (1.4)$$

With the required inductance now determined, the last item that needs to be taken care of before we pick a core and determine the number of turns necessary, is to pick a core material. To do this, we look to the leaders in ferrite core manufacturing, TDK. According to their catalog and application guide, they recommend 5 separate MnZn materials for power applications within 100 – 500kHz (N87, N88, N95, N96, N97). Of these materials, we chose N87 since it was listed as the standard material for this frequency range since this would likely give us the most options for core sizes/shapes of all the materials listed. With this in mind, we can now begin to determine the minimum Kg value of our inductor. The expression for Kg with respect to the electromagnetic parameters characteristic to our core material and the converter is

$$K_g \geq \frac{\rho \cdot L^2 \cdot I_{pk}}{K_u \cdot R_{max} \cdot B_{max}^2} \quad (1.5)$$

In this case, B_{max} is taken to be $B_{sat} \cdot 0.75$ to offer us a buffer to prevent our inductor from saturating. The value for R_{max} is taken to be $1m\Omega$ as this is the most resistance we would like our inductor to exhibit. K_u , the packing factor, is assumed to be 0.3 as this is within reason for manual winding. Using nominal values for the resistivity of copper, inductance, and peak current, we find that

$$K_g \geq 1,002mm^5 \quad (1.6)$$

Having picked our core material and determined the required K_g , the last decision we needed to make was to decide on a core shape. Looking at the options available from TDK for the N87 material, we were most interested in using the RM core for its small footprint and relatively low profile. Once this had been done, we calculated the K_g value of four different sized RM

	RM 12	RM 10	RM 8	RM 6
$K_g (mm^5)$	54,323	15,105	5,138	1,147

Table 1.4: K_g values calculated using core geometries

cores - the RM 12, RM 10, RM 8, and RM 6. This was done by taking the geometric dimensions of these cores using the expression

$$K_g = \frac{W_A \cdot A_c^2}{l_t} \quad (1.7)$$

W_A is the window area, A_c is the area of the central core through which all B field lines are expected to pass through, and l_t is the mean length turn. Using the dimensions available to us from the data sheets for each core size, we calculated the K_g values for these cores. These values are displayed in table 1.4.

As we can see in 1.4 all of the examined cores have a K_g value that exceeds the required value we had previously calculated. Although the RM 6 core would give us the smallest footprint, this was only true when the core is at room temperature ($25^\circ C$). Recalculating 1.5 using the resistivity of copper at ($100^\circ C$) and using the B_{sat} value at ($100^\circ C$) we find that the required K_g increases to $2,575 mm^5$ which exceeds the K_g value of the RM 6 core. With this in mind, we elected to choose the RM 8 core of the N87 MnZn material.

The next item is to calculate how many turns that the inductor must have and this is done using the equation

$$N = \frac{L \cdot I_{pk}}{B_{max} \cdot A_c} \approx 4 \quad (1.8)$$

Once the number of turns has been calculated by using 1.8, our final item with regards to our inductor, is to calculate the shim stock thickness. In order to find this we used the equation

$$l_g = \frac{\mu_0 \cdot N^2 \cdot A_c}{L} = 0.0794 mm \quad (1.9)$$

1.1.4 Capacitance Calculations

The final item we needed to calculate with regards to the DC-DC boost stage was the output and input capacitance. This was done by using the charge balance equation and ensuring that the difference in voltage never exceeds our target of 2%. The equation to calculate output capacitance is as follows:

$$C_o = \frac{P_o}{V_o^2} \frac{V_o - V_g}{V_o} 2fs\mathcal{R}Co \quad (1.10)$$

Parameter	Calculated Value
Switching Frequency (f_s)	375kHz
Inductor Current Ripple	30%
Output Voltage Ripple	2%
Input Voltage Ripple	2%
Inductance (L)	5.12 μ H
Output Capacitance (C_o)	3.616 μ F
Input Capacitance (C_{in})	2.17 μ F

Table 1.5: Calculated and chosen parameters of DC-DC Boost stage.

Similarly, we take the charge balance equations to calculate the necessary output capacitance by the relationship:

$$C_{in} = \frac{\mathcal{R}_{\mathcal{L}}}{8f_s \mathcal{R}_{C_{in}}} \frac{P_o}{V_i^2} \quad (1.11)$$

From here we find that the input capacitance and output capacitance required for a voltage ripple value of no more than 2% for both input and output voltage is 2.17 μ F and 3.61 μ F respectively. When looking for capacitors, we decided to use X7R capacitors since their capacitance is not negatively affected by changes in temperature, and the capacitor deratings given are usually very accurate. With this in mind, we opted for the CNC6P1X7R2A475K250AE and C2012X7R1H475K125AC to use as our input and output capacitors respectively. Looking at the derating curves on each respective datasheet we find that at 50V the input and output capacitors selected are derated to about 1.41 μ F for both capacitors. With this in mind, we decided to have two capacitors at the input and three at the output to have a nominal capacitance of 4.22 μ F on the output and 2.83 μ F on the input.

1.1.5 Parameter Table

All of the calculated parameters of our converter are shown once more in table 1.5.

1.2 Board Layout Procedure

With the design aspect of our converter finished we move on to laying out our board. When laying out a high power, high frequency switched mode power converter, special attention must be paid to critical loops and nodes of the circuit. To assess where these loops and nodes of importance are, one needs only to look back at first principles:

$$v_L = L \frac{di}{dt} \quad (1.12)$$

$$i_C = C \frac{dv}{dt} \quad (1.13)$$

A few conclusions can be drawn from these fundamental equations that will allow us to thoughtfully lay out our board. First, sections of the circuit where a large amount of current and voltage are changing rapidly, we will see large voltage and currents induced in the form of overshoots that could damage our components. Secondly, we notice that these overshoots are proportional to the amount of parasitic inductance due to the loop, and parasitic capacitance due to the node respectively. Due to the nature of high frequency designs, the unwanted effects of high $\frac{di}{dt}$ and $\frac{dv}{dt}$ loops and nodes are inherent to such a design and can only be mitigated but never fully eliminated. Therefore the only effective way to combat this phenomena is to minimize parasitic loop inductance and node capacitance at these critical points.

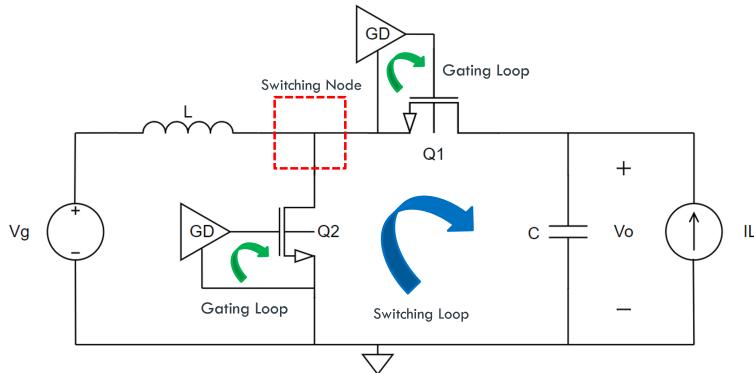


Figure 1.4: Boost converter topology with critical points highlighted

Referring to figure 1.4 we recognize that, for a boost converter, the switching loop has high current that changes at the switching frequency. Additionally we see that the switching node will have a high voltage that also changes at the switching frequency. These two points will be the primary culprits of the parasitics in the boost stage, so they will need to be laid out carefully and critically. Another source of parasitics is the gating loop, which has high frequency switching current in its path. This as well will need to be laid out carefully, so as to not induce high voltage spikes in our gate signals that could trigger a false turn on/off of the switch.

1.2.1 Switching Loop

As was motivated in the previous section, the switching loop must be designed in such a way as to minimize its parasitic inductance. To do this, we leverage the vertical nature of a PCB and route our loop through the board, to greatly reduce the cross sectional area and length of the loop.

As is illustrated in figure 1.5, we placed our switches on one side of the board and our output capacitors directly beneath the switches and routed our loop through the PCB. The configuration we chose achieves three key design goals. Firstly and most importantly, this layout reduces

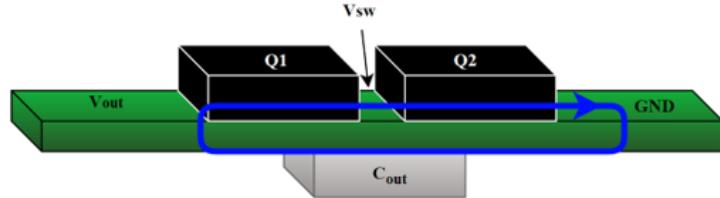


Figure 1.5: Vertical Switching Loop Diagram

our loop inductance by keeping the cross sectional area of the loop, and its length as small as possible (limited only by the package size of the switches). Secondly, in order to achieve this design, the use of vias through the board will be necessary. The use of the vias near our switches will assist in the cooling of the switches as they allow heat to flow through the board and away from our switches. Lastly, by arranging the switches in this configuration, the switching node (V_{SW}) will only need to lie in between the two switches, and not on both sides of the PCB like if we chose to keep a switch on either side of the board. This greatly reduces the size of the switching node, which we noted in the previous section was crucial to reduce capacitive coupling in our converter. A look at our realized switching loop can be seen in figure 1.6 and 1.7.

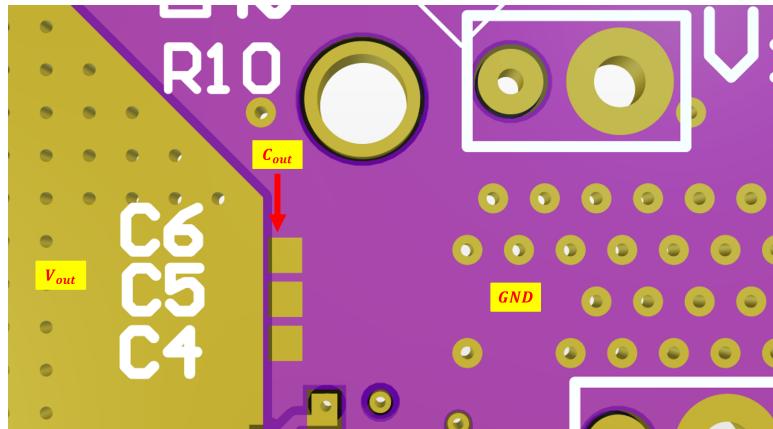


Figure 1.6: Switching loop layout top side

1.2.2 Gating Loop

Though the gating loop is very low power and carries little current, the high frequency nature of the loop means that special attention must be made to minimize the loop inductance, similar to the switching loop. To do this, we employ a similar method of utilizing the vertical nature of the PCB to route the forward and return path of the loop through the board. To make this loop as compact as possible, the gate driver is placed very close to the switches and very small 0402

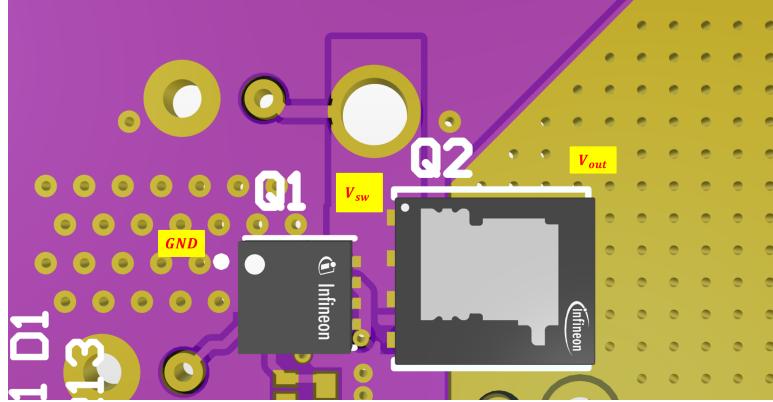


Figure 1.7: Switching loop layout bottom side

components are used for the gate resistors to keep the length very small. Our realized gating loops can be seen in figure 1.8.

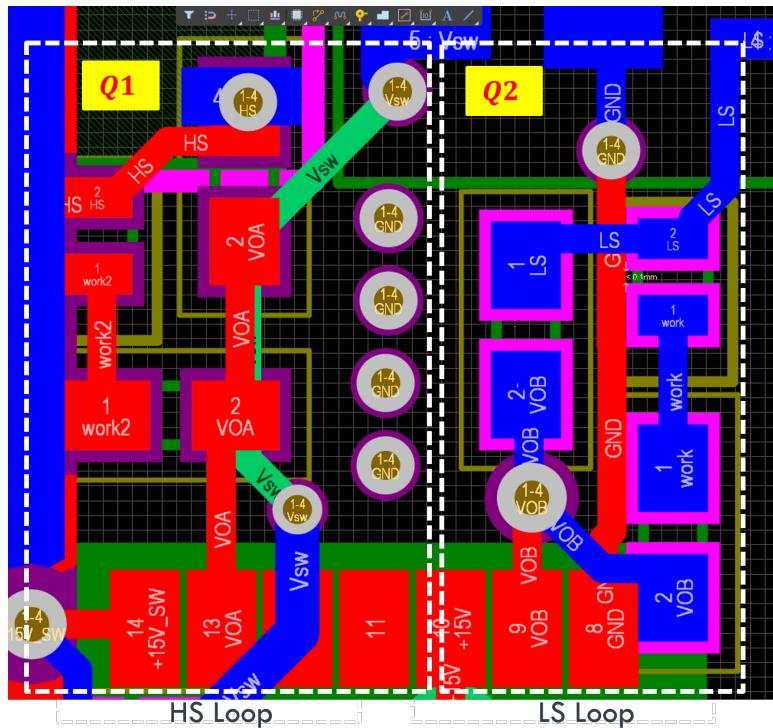


Figure 1.8: PCB snapshot of the gating loops

For the high side (HS) loop, the forward path of the loop from the VOA pad on the gate driver to the gate pin of the high side switch (Q1) is through the 0402 components on the top (red) layer. The return path from (V_{sw}) to the gate driver is routed directly beneath the forward path

on middle layer 3 (green). The low side (LS) loop is routed almost identically, only differing in the layers used.

1.2.3 Capacitive Coupling

For the boost stage, the switching node is the primary culprit of parasitic capacitance in the circuit and, as mentioned in the section on the switching loop, is already reduced to as small as physically possible. In general for our entire board, the switching node, though having the greatest effect due to its high frequency, is not the only source of parasitic capacitance that we encounter. The integrated power module (IPM) will also exhibit some amount of parasitic capacitance due to its high voltage and somewhat high frequency (15kHz). Since we have little control over reducing the parasitic capacitance from the IPM, a technique of shielding sensitive traces near the IPM is used to protect sensitive analog signals needed for our controller. To do this, a pseudo-Faraday cage made of vias and polygon pours is used to cut down on capacitive coupling to the noisy nodes. This method is referred to by some as a PCB coax cable. A few examples of this method can be seen in figure 1.9.

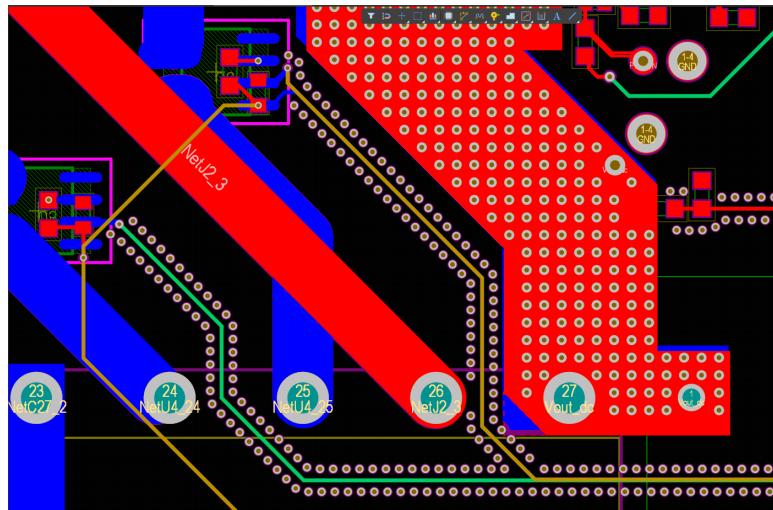


Figure 1.9: Example of shielding use

On our board, we shielded our sensed input dc current, two phases of ac current, and input and output dc voltages. These signals must be preserved in order to have accurate readings for our control loop, so shielding them was crucial. Though this technique is not an exact replica of a Faraday cage or a coax cable, it does help mitigate the capacitance to some extent, which is better than leaving them un-shielded to begin with.

1.2.4 Thermal Considerations

Assessing thermal solutions on a PCB can be mostly qualitative at best without the use of advanced simulations or collected lab data of similar designs. For our case, the boost converter switches are the main source of heat, and will need some sort of provision to keep them from reaching their maximum junction temperature. Since both of our switches are double side cooled, heat sinks will be able to be fitted on the top and will help cool the switches during their operation. To be extra safe, we made other provisions to further cool the switches. The PCB itself can be leveraged as a heat sink. To do this, we made a oversized 1oz copper pour of the drain pad (V_{OUT}) of our high side FET on all layers and via stitched the pour to allow the heat to easily flow through the board. FR4, the material that PCB's are made of, is an extremely bad conductor of heat by design. To help reduce the thermal resistance of FR4, we chose to expose the copper on this pour to further help displace the heat from the switch, a picture of this method can be seen in figure 1.10.

We note that this method is not advisable for the low side FET, as its drain is connected to the switching node, which we made sure to minimize as much as possible to reduce parasitics. The low side FET will mostly rely on its source cooled heat sink for thermals. This design does not take into account the fan that will be used in the enclosure of the electric bike which will further assist our thermal management design.

1.2.5 Board Overview

With the critical parts of our circuit laid out and locked in, less fussy components can be laid out around these parts in a fashion of our choosing. The IPM for instance, its layout only requires its critical components be as close as possible to its pins. The placement of the IPM itself is wholly determined by the placement of the boost stage. With this more eased requirement on layout, we decided to divide our board in two sections, half being where our main power flow lives and the other half being where our launchpad digital signals live. A top down view of our completed board can be seen the figures 1.11 and 1.12.

With all of this analysis and careful thinking, we did our due diligence to route our board to meet all of the previously mentioned specifications. Moving forward we will carry out careful and rigorous testing on our converter before we are confident enough to drive an electric bike's motor.

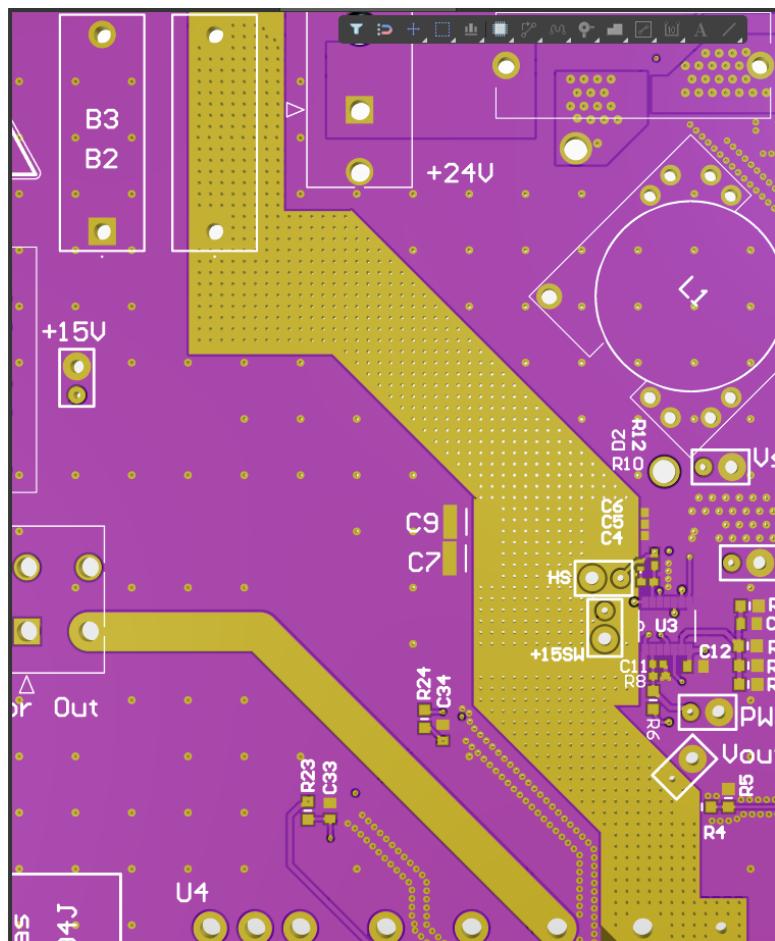


Figure 1.10: V_{OUT} exposed pad for thermals

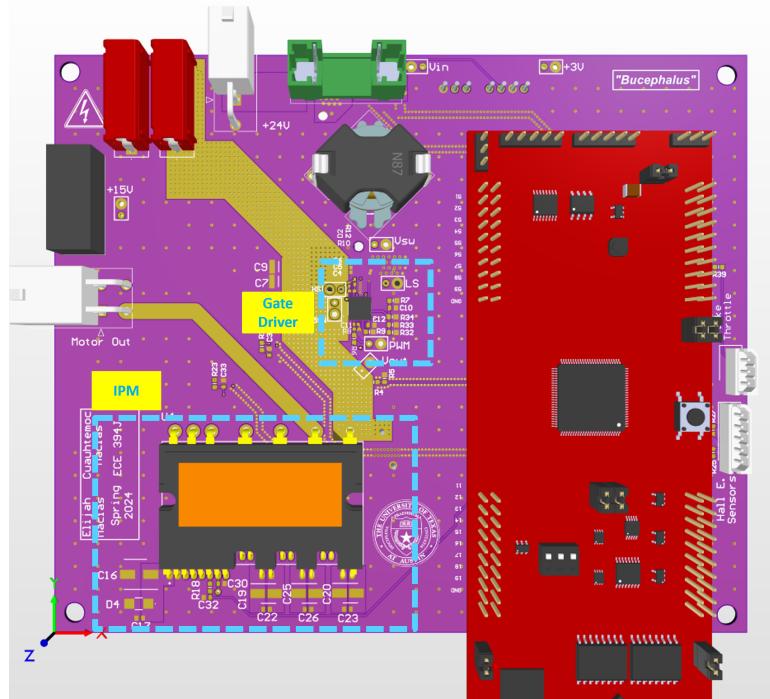


Figure 1.11: Top side of board 3d view

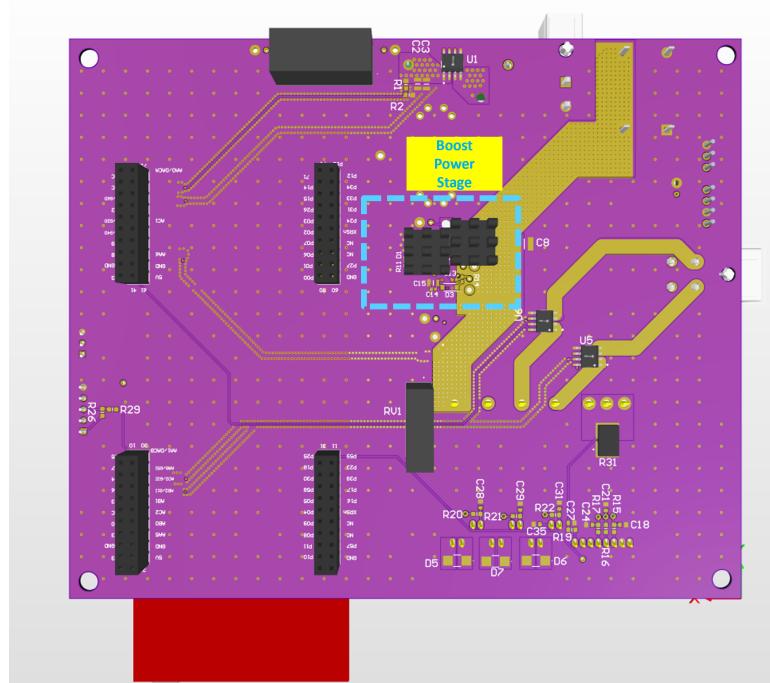


Figure 1.12: Bottom side of board 3d view