[0064] In this case, the encoder **220** may perform BCH encoding and LDPC encoding with respect to the segmented L1 signalings.

[0065] Hereinafter, referring to FIGS. **4**A and **4**B, the encoder **220** will be described in more detail.

[0066] FIGS. **4**A and **4**B are block diagrams illustrating a configuration of an encoder, according to an exemplary embodiment. First, referring to FIG. **4**A, the encoder **220** may include a zero bit inserter **221**, a BCH/LDPC encoder **223**, a parity interleaver **225**, and a zero bit remover/puncturer **227**.

[0067] The zero bit inserter **221** adds zero bits (or zero padding bits) to the segmented L1 signaling.

[0068] Specifically, as shown in FIG. **4**A, the BCH/LDPC encoder **223** includes a BCH encoder **223-1** for performing BCH encoding and an LDPC encoder **223-2** for performing LDPC encoding. That is, the BCH encoder **223-1** may generate a BCH codeword through the BCH encoding to output the BCH codeword to the LDPC encoder **223-2**, and the LDPC encoder **223-2** may perform LDPC encoding using the BCH codeword as an information word. In this case, in the case of the LDPC encoding that is performed by the LDPC encoder **223-2**, an information word having a predetermined length is required according to the code rate, and thus the BCH encoder **223-1** should generate a BCH codeword having the predetermined length.

[0069] In order for the BCH encoder **223-1** to generate a BCH codeword having the predetermined length, it is required to perform the BCH encoding with respect to a predetermined number of bits. Accordingly, the zero bit inserter **221** may pad zero bits to the segmented L1 signaling so that the segmented L1 signaling has the length of the information word that is required in the BCH code, and may output L1 post signaling to which the zero bits are padded to the BCH/LDPC encoder **223**.

[0070] As described above, the length of the segmented L1 signaling may be equal to or smaller than K_{th}. Here, K_{th} may be smaller than the length of the information word that is required during the BCH encoding. Since the length of the information word that is required during the BCH encoding is smaller than the length of the information word that is required during the LDPC encoding, K_{th} may be smaller than the length of the information word that is required during the LDPC encoding.

[0071] Accordingly, the zero bit inserter **221** may add the zero bits to the segmented L1 signaling. For example, in the case where the segmented L1 signaling is formed of K_{sig} bits, the number of bits of the information word that is required during the BCH encoding is K_{bch}, and $K_{bch}>K_{sig}$ is set, the zero padding bit inserter **221** may add $K_{bch}-K_{sig}$ zero bits to the segmented L1 signaling.

[0072] However, according to circumstances, the BCH encoder **223-1** may be omitted from the BCH/LDPC encoder **223**, and the BCH/LDPC encoder **223** may perform only the LDPC encoding without the BCH encoding.

[0073] In this case, the zero bit inserter **221** may pad the zero bits to the segmented L1 signaling so that the segmented L1 signaling has the length of the information word that is required in the LDPC codeword. For example, if the segmented L1 signaling is formed of K_{sig} bits, the number of bits of the information word of the LDPC codeword is K_{ldpc}, and $K_{ldpc}>K_{sig}$ is set, the zero padding bit inserter **221** may add $K_{ldpc}-K_{sig}$ zero bits to the segmented L1 signaling.

[0074] As described above, the zero bit inserter **221** may insert the zero bits into the segmented L1 signaling, and then may output the L1 signaling into which the zero bits are inserted to the BCH/LDPC encoder **223**.

[0075] The BCH/LDPC encoder **223** performs the BCH encoding and the LDPC encoding with respect to the L1 signaling transmitted from the zero bit inserter **221**. For this, as shown in FIG. **4**B, the BCH/LDPC encoder **223** may include a BCH encoder **223-1** for performing the BCH encoding and an LDPC encoder **223-2** for performing the LDPC encoding.

[0076] Specifically, the BCH encoder **223-1** generates BCH parity bits by performing the BCH encoding of the L1 signaling, to which the zero bits are added, as the information word, and generates a plurality of BCH codewords formed of the information word and the BCH parity bits. Here, 168 BCH parity bits may be generated by the BCH encoding.

[0077] Further, the LDPC encoder **223-2** may generate LDPC parity bits by performing the LDPC encoding with respect to the BCH codewords generated by the BCH encoding, and may output a plurality of LDPC codewords formed of the information word and the LDPC parity bits to the parity interleaver **225**. For example, if the length of the information word of the BCH encoder **223-1** is K_{bch}, and the length of the information word of the LDPC encoder **223-2** is K_{ldpc}, the LDPC encoder **223-2** may generate the LDPC codeword having the length of N_{ldpc}, by performing the LDPC encoding at a constant code rate.

[0078] Since the BCH code and the LDPC code are systematic codes, the information word may be included in the codeword. That is, since the BCH encoding is performed using the L1 signaling as the information word, the BCH codeword generated as a result of the BCH encoding may include the L1 signaling that is the information word as it is, and may be in the form in which the BCH parity bits are added to the information word. Further, since the LDPC encoding is performed using the BCH codeword as the information word, the LDPC codeword generated as a result of the LDPC encoding may include the L1 signaling that is the information word and the BCH parity bits as they are, and may be in the form in which the LDPC parity bits are added to the information word.

[0079] In the above-described example, it is described that both the BCH encoding and the LDPC encoding are performed. However, this is merely exemplary, and according to circumstances, the BCH encoding may be omitted. That is, the BCH encoder **223-1** may be omitted. Accordingly, the LDPC encoder **223-2** may generate the LDPC codeword through performing of the LDPC encoding using the L1 signaling transmitted from the zero bit inserter **221** as the information word, and may output the generated LDPC codeword to the parity interleaver **225**.

[0080] Further, in the above-described example, it is described that the zero bits are added to the segmented L1 signaling by the zero bit inserter **221** and the BCH encoding and the LDPC encoding are sequentially performed with respect to the L1 signaling to which the zero bits are added. However, this is merely exemplary, and the zero bit inserter **221** may be arranged between the BCH encoder **223-1** and the LDPC encoder **223-2**. The detailed explanation will be made later with reference to FIG. **10**.