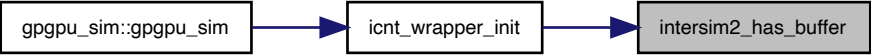


gpgpu\_sim::gpgpu\_sim



```
graph LR; A[gpgpu_sim::gpgpu_sim] --> B[icnt_wrapper_init]; B --> C[intersim2_has_buffer];
```

icnt\_wrapper\_init

intersim2\_has\_buffer