

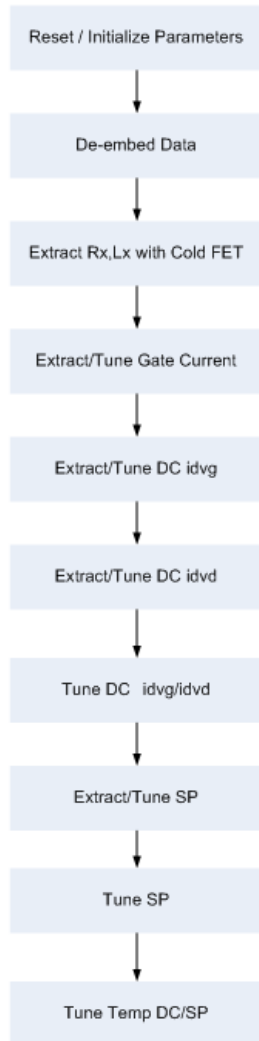
4.2 Hand-Scripts of Angelov Model Parameter Extractions

4.3 Notes on the IC-CAP Help Doc

4.3.1 Parameter Extraction Flow Example

0. Example Parameter Extraction Flow

Based on the parameter extraction flow, following is an example parameter extraction flow to see that DC matches with S-parameter of vgm2.



The following is an orderly description about example extraction flow using the sample data loaded in the Angelov-GaN Toolkit.

1. Initialize

Reset Parameter to Defaults

Reset the values of Model Parameters to the default before you begin the Extraction.

Initialize Parameter and Boundaries for Extraction

Initialize the values of Model Parameters, Opt Min and Opt Max before you begin the Extraction.

Update All Measures Data for Extraction

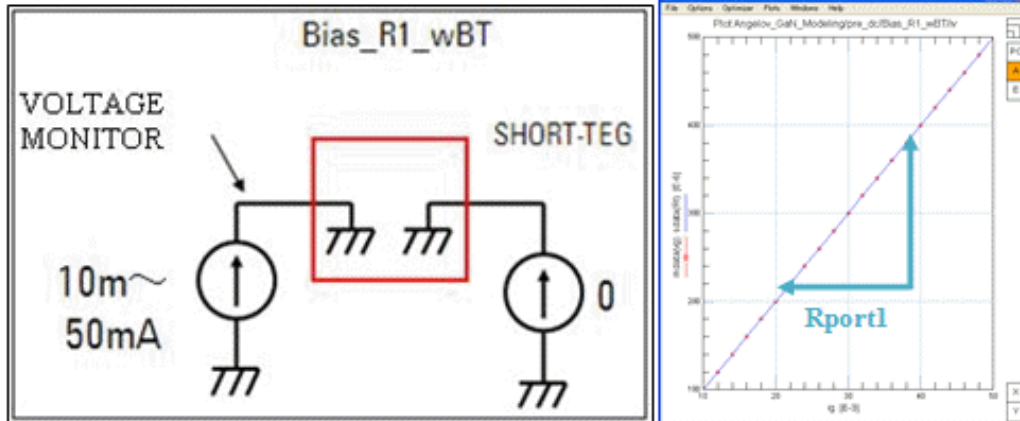
Perform PEL calculation and De-embed with respect to all the data, and update before you begin the extraction.

2. DC Port Resistance

PreDC Port1

Calculate **Rport1**, the DC Path Resistance of Port1 side from the Slope using E:Rport1

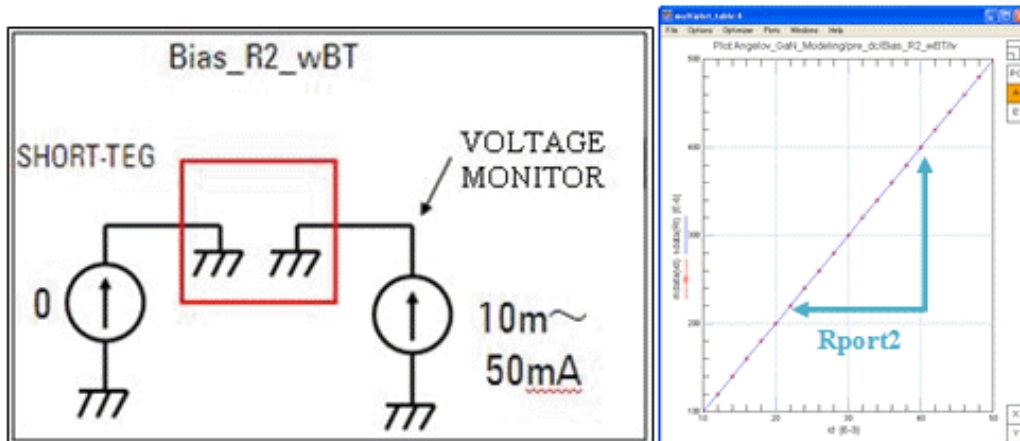
Example of iv plot



PreDC Port2

Calculate **Rport2**, the DC Path Resistance of Port2 side from the Slope using E:Rport2

Example of iv plot



3. SP Cold FET

SP Cold FET

Here you can calculate the resistance and inductance components by ColdFET method.
Since this is the initial value, you need to implement tuning later.

1. Calculate the resistances **RG**, **RD** and **RS** from R11, R22, R30 using E:RG, RD, RS.
In the frequency input prompt that appears, enter the flat range in low frequency part of **R11**, **R22** and **R30** for resistance component and implement the Extraction.
If there is no flat range, you may also use the region used for design.
Extraction results in R11=**RG**, R22=**RD** and R30=**RS**.

Example of prompt (input low frequency)

Enter the lower frequency [Hz] to extract the resistances.

5G

OK Cancel

Example of prompt (input high frequency)

Enter the higher frequency [Hz] to extract the resistances.

10G

OK Cancel

2. Calculate the inductances **LG**, **LD**, **LS** from L11, L22, L30 using E:LG, LD, LS.
In the frequency input prompt that appears, enter the flat range in high frequency part of **L11**, **L22** and **L30** for inductance component and implement the Extraction.
If there is no flat range, you may also use the region used for design.
Extraction results in L11=**LG**, L22=**LD**, L30=**LS**.

Example of prompt (input low frequency)

Enter the lower frequency [Hz] to extract the inductances.

10G

OK Cancel

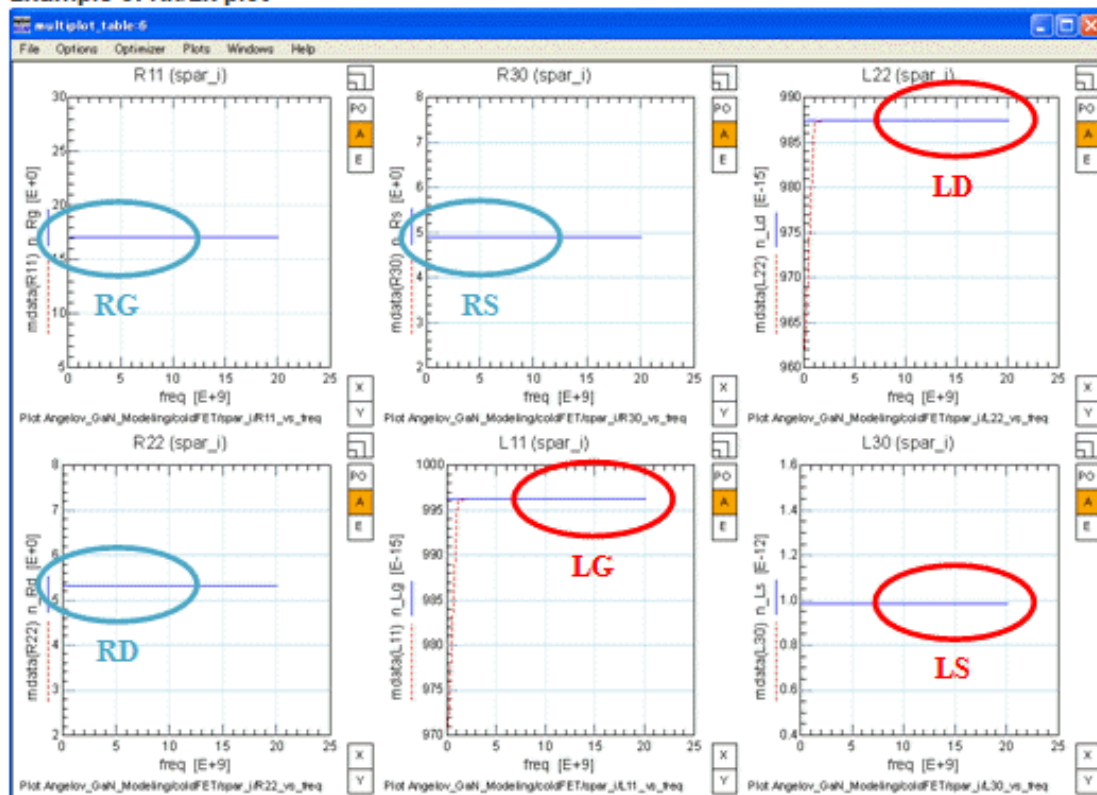
Example of prompt (input high frequency)

Enter the higher frequency [Hz] to extract the inductances.

20G

OK Cancel

Example of Rx/Lx plot



4. Gate Diode

DC gate diode forward

Here you can implement the Extraction and Optimization of forward Gate current.

1. Calculate **IJ**, **PG**, **VJG** from **Ig**, using **E**: **IJ**, **PG**, **VJG**

In the bias input prompt that appears, enter the range in linear part of $\log(Ig)$ and implement the Extraction of **IJ**, **PG** and **VJG**.

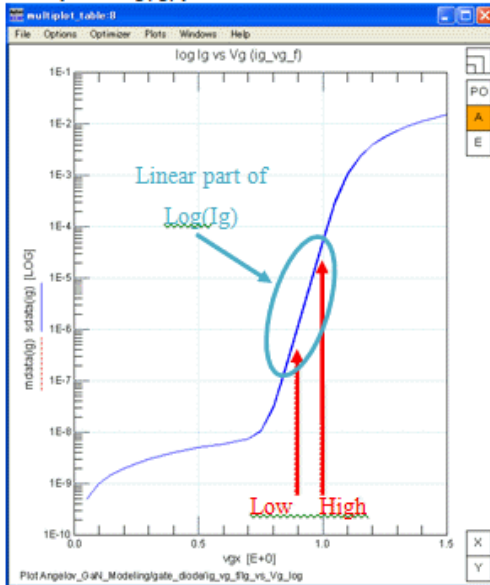
Example of prompt (input low bias)

Enter the lower voltage of v_g to extract f_{diode} .

Example of prompt (input high bias)

Enter the higher voltage of v_g to extract f_{diode} .

Example of $\log(Ig)$ plot



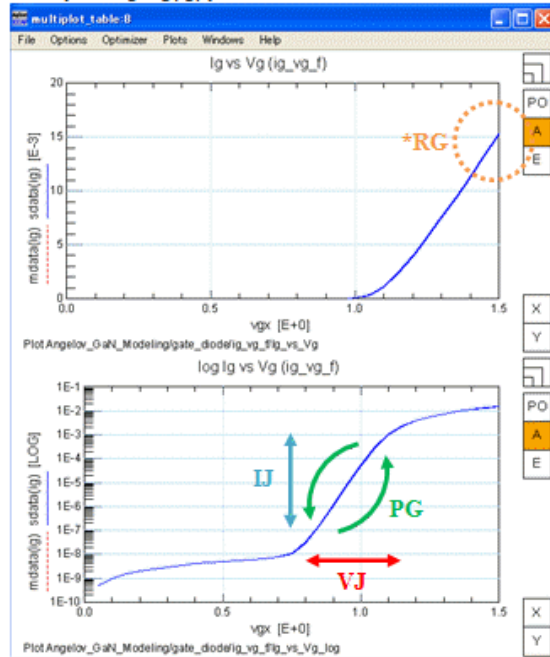
2. Optimization using **O**: **IJ**, **VJG**, **TIJ**, **VJG**

Keeping the Gate current (Ig , $\log-Ig$) in view, carry out an optimization using **IJ** and **VJG** to match the approximate current value.

3. Optimization using O: PG

Keeping the Gate current (I_g , $\log(I_g)$) in view, implement an optimization using **PG** to match the slope of $\log(I_g)$.

Example of $I_g/\log(I_g)$ plot



- RG is usually matched with S-parameter.

DC gate diode reverse

Here you can implement the Extraction and Optimization of reverse Gate current.

1. Calculate **KBGATE**, **VBDGS**, **VBDGD** and **PBGD** from I_g using E: KBGATE, VBDGS, VBDGD, PBGD

In the bias input prompt that appears, enter the range in linear part of $\log(I_g)$ and implement the Extraction of **KBGATE**, **VBDGS**, **VBDGD** and **PBGD**.

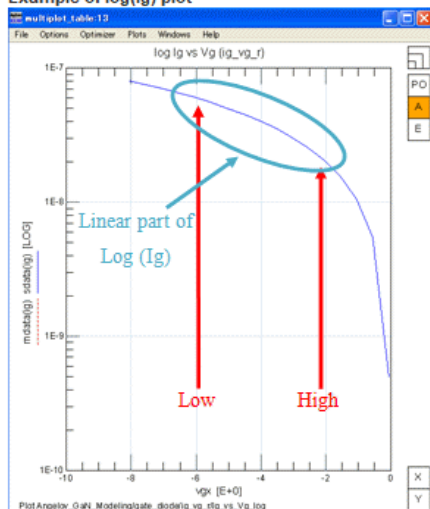
Example of prompt (input low bias)

Enter the lower voltage of V_g to extract r_{diode} .

Example of prompt (input high bias)

Enter the higher voltage of V_g to extract r_{diode} .

Example of $\log(I_g)$ plot

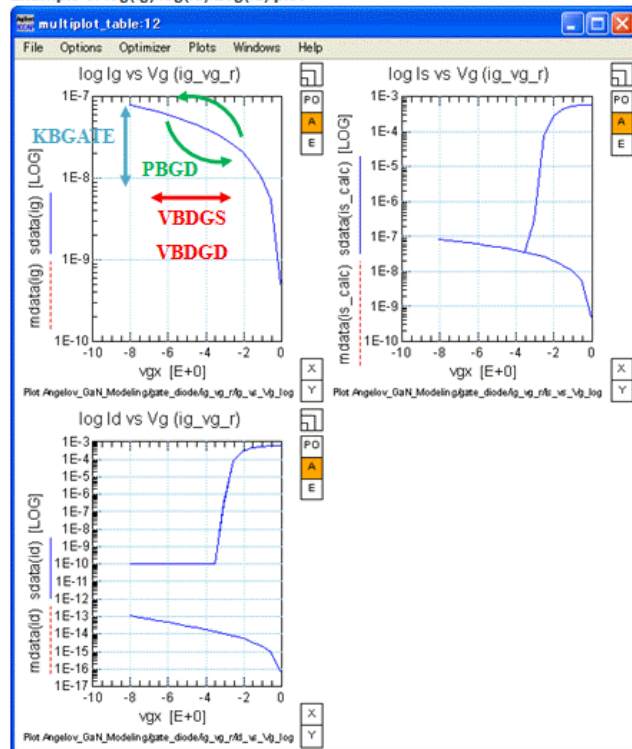


2. Optimize **KBGATE**, **VBDGS**, **VBDGD** and **PBGD** using

T: KBGATE, VBDGS, VBDGD, PBGD.

Keeping the Gate current ($\log(I_g)$) in view, implement an optimization using **KBGATE**, **VBDGS**, **VBDGD** and **PBGD** to match the approximate current value.

Example of $\log(I_g)/\log(I_d)/\log(I_s)$ plot



5. idvg & idvd

DC idvg

Here you can implement the Extraction and Optimization of idvg characteristics.

1. Calculate **IPK0**, **VPKS**, **P1**, **P2** and **P3** from Id using E: IPK0,VPKS,P1,P2,P3{+}{_}.

In the bias input prompt that appears, enter the range as shown below:

Bias before gm is rises up

Bias at which Id starts rising up (Vth vicinity)

Bias which passes over Gm max

And then, implement the Extraction of **IPK0**, **VPKS**, **P1**, **P2** and **P3**.

Example of prompt (input low bias)

Enter the lower voltage of vg to extract peak Gm.

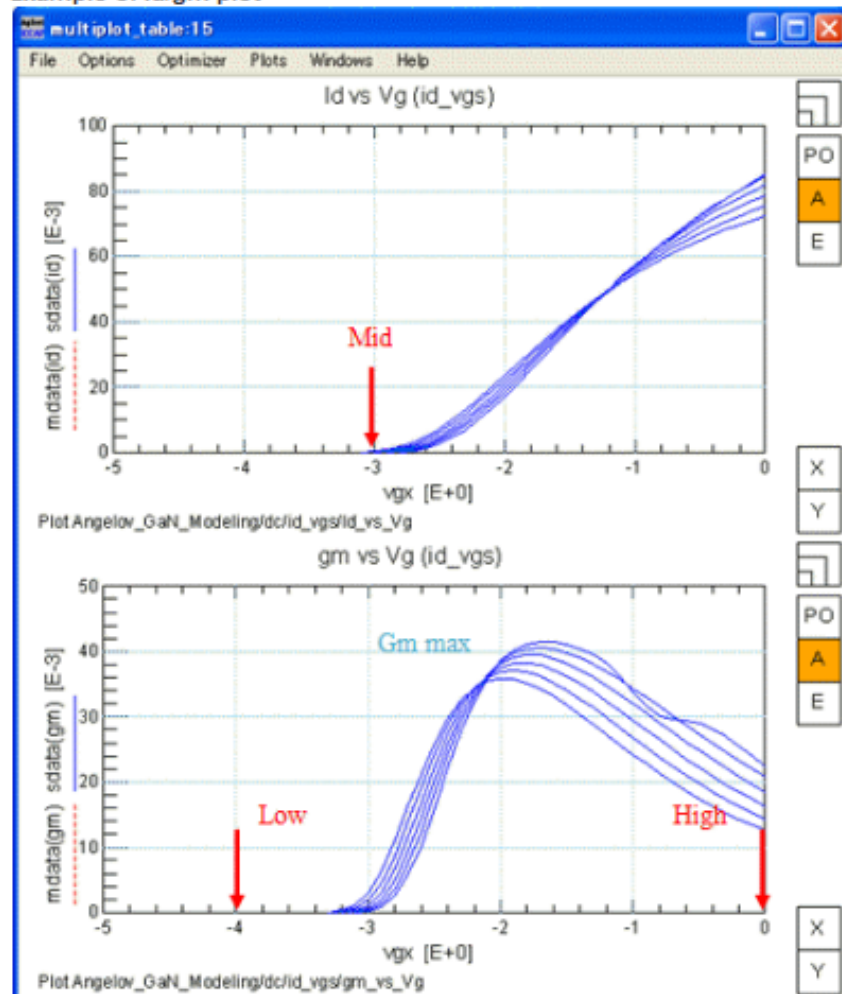
Example of prompt (input mid bias)

Enter the mid voltage of vg.

Example of prompt (input high bias)

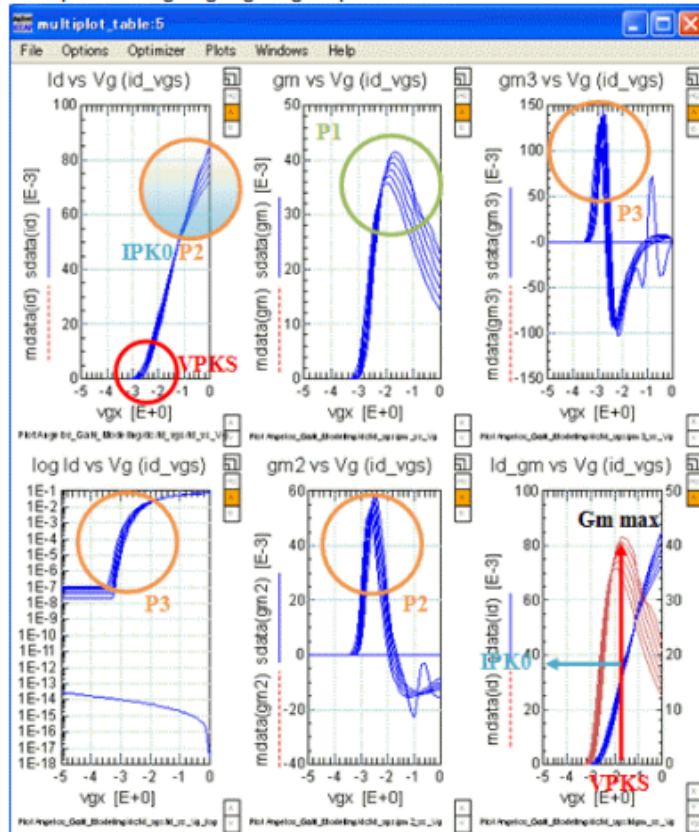
Enter the higher voltage of vg to extract peak Gm.

Example of Id/gm plot



- Optimize **VPKS**, **P2** and **P3** using O: VPKS,P2,P3{+}{_}.
Keeping log-Id, gm, gm2 and gm3 in view, match the approximate shape using **VPKS**, **P2** and **P3**.
- Optimize **IPK0**, **VPKS**, **P1**, **P2** and **P3** using O: IPK0,VPKS,P1,P2,P3{+}{_}.
Keeping Id, log-Id, gm, gm2 and gm3 in view, adjust to make the balance (shape) better on the whole, using **IPK0**, **VPKS**, **P1**, **P2** and **P3**.
- Optimize **VPKS** and **P1** using O: VPKS,P1.
Keeping log-Id and gm in view, match using **VPKS** and **P1**.

Example of Id/log-Id/gm/gm2/gm3 plot



DC idvd

Here you can implement the Extraction and Optimization of idvd characteristics.

1. Calculate **LAMBDA** from Id using E: **LAMBDA**.

In the bias input prompt that appears, enter the range as shown below:

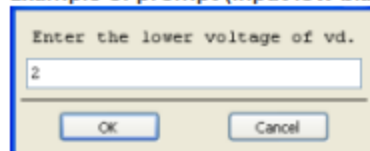
Bias of linear region

Bias at which the self heating is observed

Bias at which Avalanche current is about to appear or Maximum bias

And then, implement the Extraction of **LAMBDA**.

Example of prompt (input low bias)

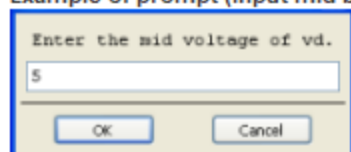


Enter the lower voltage of vd.

2

OK Cancel

Example of prompt (input mid bias)

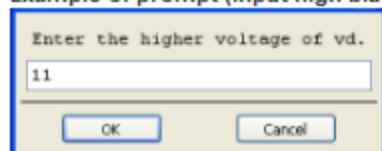


Enter the mid voltage of vd.

5

OK Cancel

Example of prompt (input high bias)

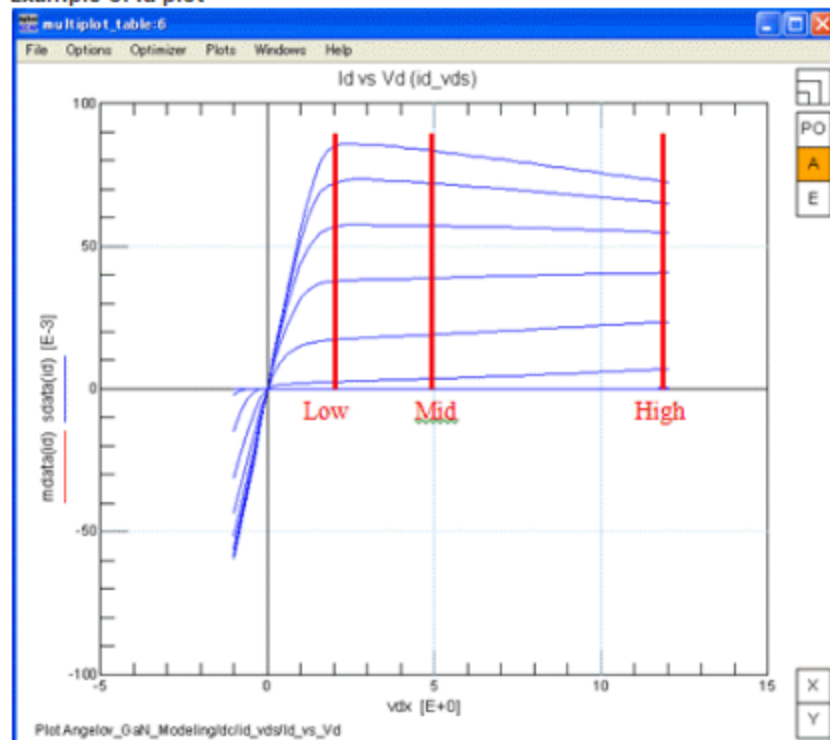


Enter the higher voltage of vd.

11

OK Cancel

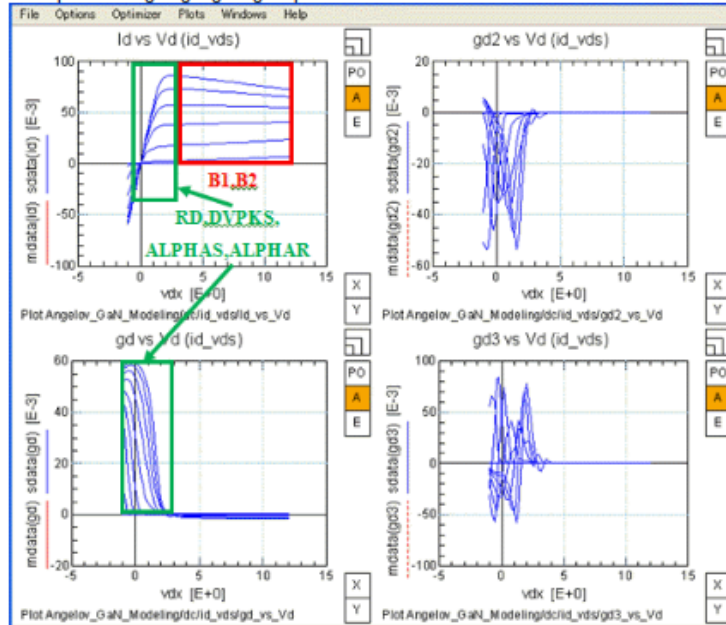
Example of Id plot



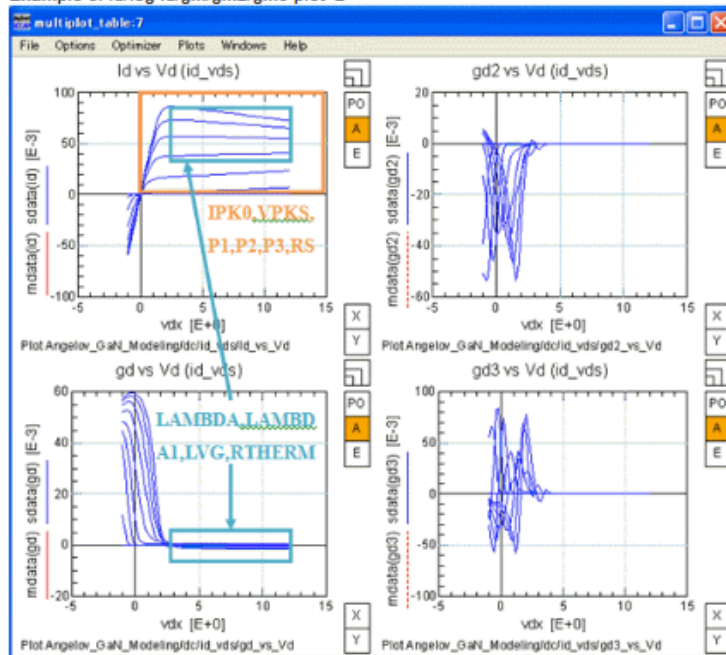
2. Optimize **LAMBDA**, **B1** and **B2** using O: **LAMBDA,B1,B2{+}{_}**.
Keeping Id and gds in view, adjust for a better balance of the bias interval on the whole, using **LAMBDA**, **B1** and **B2**.
3. Optimize **ALPHAR**, **ALPHAS** and **RD** using O: **ALPHAR,ALPHAS,RD{+}{_}**.
Keeping Id and gds in view, adjust to match with the rising part (linear region) using **ALPHAR**, **ALPHAS** and **RD**.
4. Optimize **IPK0**, **VPKS** and **P1** using O: **IPK0,VPKS,P1{+}{_}**.
Keeping Id in view, adjust on the whole using **IPK0**, **VPKS** and **P1**.

- Optimize **ALPHAR**, **ALPHAS** and **RD** using O: ALPHAR,ALPHAS,RD{+}{_}.
Keeping Id and gds in view, adjust to match with the rising part (linear region) using **ALPHAR**, **ALPHAS** and **RD**.
- Optimize **IPK0**, **VPKS**, **P1**, **P2**, **P3**, **B1**, **B2**, **ALPHAR**, **ALPHAS** and **RD** using O: IPK0,VPKS,P1,P2,P3,B1,B2,ALPHAR,ALPHAS,RD{+}{_}.
Keeping Id and gds in view, adjust on the whole using **IPK0**, **VPKS**, **P1**, **P2**, **P3**, **B1**, **B2**, **ALPHAR**, **ALPHAS** and **RD**.
- Optimize **IPK0**, **VPKS**, **DVPKS**, **P1**, **P2**, **P3**, **B1**, **B2**, **LAMBDA**, **LAMBDA1**, **LVG**, **VKN**, **RD**, **RS** and **R THERM** using O: idvd_all{+}{_}.
Keeping Id in view, adjust on the whole using **IPK0**, **VPKS**, **DVPKS**, **P1**, **P2**, **P3**, **B1**, **B2**, **LAMBDA**, **LAMBDA1**, **LVG**, **VKN**, **RD**, **RS** and **R THERM**.

Example of Id/log-Id/gm/gm2/gm3 plot -1



Example of Id/log-Id/gm/gm2/gm3 plot -2



DC idvg

Once the Extraction and Optimization of idvg and idvd are over, the next step is to implement detailed tuning, keeping both the characteristics in view alternately. Here, you will implement Re-optimization of idvg characteristics.

1. Optimize **VPKS** and **P1** using O: VPKS,P1{+}{_}.
Keeping Id in view, adjust the characteristics using **VPKS** and **P1**.
2. Optimize **IPK0**, **VPKS**, **P1**, **P2** and **P3** using O: IPK0,VPKS,P1,P2,P3{+}{_}.
Keeping Id, log-Id, gm, gm2 and gm3 in view, adjust on the whole using **IPK0**, **VPKS**, **P1**, **P2** and **P3**.
3. Optimize **VPKS**, **P2** and **P3** using O: VPKS,P2,P3.
Keeping Log-Id and gm in view, adjust using **VPKS**, **P2** and **P3**.
4. Tuning **IPK0**, **VPKS**, **P1**, **P2** and **P3** using O: IPK0,VPKS,P1,P2,P3{+}{_}.
Keeping Id, log-Id, gm, gm2 and gm3 in view, adjust on the whole using **IPK0**, **VPKS**, **P1**, **P2** and **P3**.

DC idvd

Once the Extraction and Optimization of idvg and idvd are over, the next step is to implement detailed tuning, keeping both the characteristics in view alternately. Here, you will implement Re-optimization of idvd characteristics.

1. Optimize **ALPHAR**, **ALPHAS** and **RD** using O: ALPHAR,ALPHAS,RD{+}{_}.
Keeping Id and gds in view, adjust to match with the rising part (linear region) using **ALPHAR**, **ALPHAS** and **RD**.
2. Optimize **IPK0**, **VPKS**, **P1**, **P2** and **R THERM** using O: IPK0,VPKS,P1,P2,R THERM{+}{_}.
Keeping Id in view, adjust on the whole using **IPK0**, **VPKS**, **P1**, **P2** and **R THERM**.

DC idvg

Finally, implement the detailed tuning as the last step of DC modeling. Here, you will implement Re-optimization of idvg characteristics.

1. Optimize **IPK0**, **VPKS**, **P1**, **P2** and **P3** using O: IPK0,VPKS,P1,P2,P3{+}{_}.
Keeping Id, log-Id, gm, gm2 and gm3 in view, adjust on the whole using **IPK0**, **VPKS**, **P1**, **P2** and **P3**.
This completes the DC part of the modeling. If all the DC characteristics are good with accuracy, you can proceed next for the RF part of the modeling.

6. SP

SP vg at vd0 A1

Here, you implement the Extraction of capacitance characteristics when Vd=0.
(Implement initial Extraction at Vd=0, Vg=0, and optimization.)

1. Calculate **CGSPI**, **CGDPI**, **CDS**, **CGS0**, **CGD0**, **P10**, **P11**, **P40** and **P41** from Cgs_vs_Vg, Cgd_vs_Vg and Cds_vs_Vg using E: CGSPI,CGDPI,CDS,CGS0,CGD0,P10,P11,P40,P41{+}{_}.
In the bias input prompt that appears, enter the range as shown below:
Bias at which the lower capacitance is calculated
Bias at which the higher capacitance is calculated
And then, implement the Extraction of **CGSPI**, **CGDPI**, **CDS**, **CGS0**, **CGD0**, **P10**, **P11**, **P40** and **P41**.
- If you enter 0 for all, the whole range is specified.

Example of prompt (input low bias)

Enter the lower voltage of vg to extract capacitances.

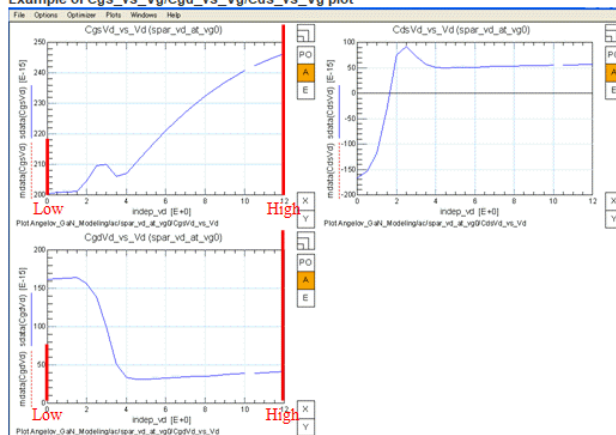
OK Cancel

Example of prompt (input high bias)

Enter the higher voltage of vg to extract capacitances.

OK Cancel

Example of Cgs_vs_Vg/Cgd_vs_Vg/Cds_vs_Vg plot



SP vd at vg0

Here, you implement the Extraction of capacitance characteristics when $V_g=0$.
(Implement initial Extraction at $V_d=0$, $V_g=0$, and optimize.)

1. Calculate **P20, P21, P30 and P31** from $C_{gs_vs_Vd}$, $C_{gd_vs_Vd}$ and $C_{ds_vs_Vd}$ using E: **P20,P21,P30,P31**
In the bias input prompt that appears, enter the range as shown below:
Bias at which the lower capacitance is calculated
Bias at which the higher capacitance is calculated
And then, implement the Extraction of **P20, P21, P30 and P31**.
- If you enter 0 for all, the whole range is specified.

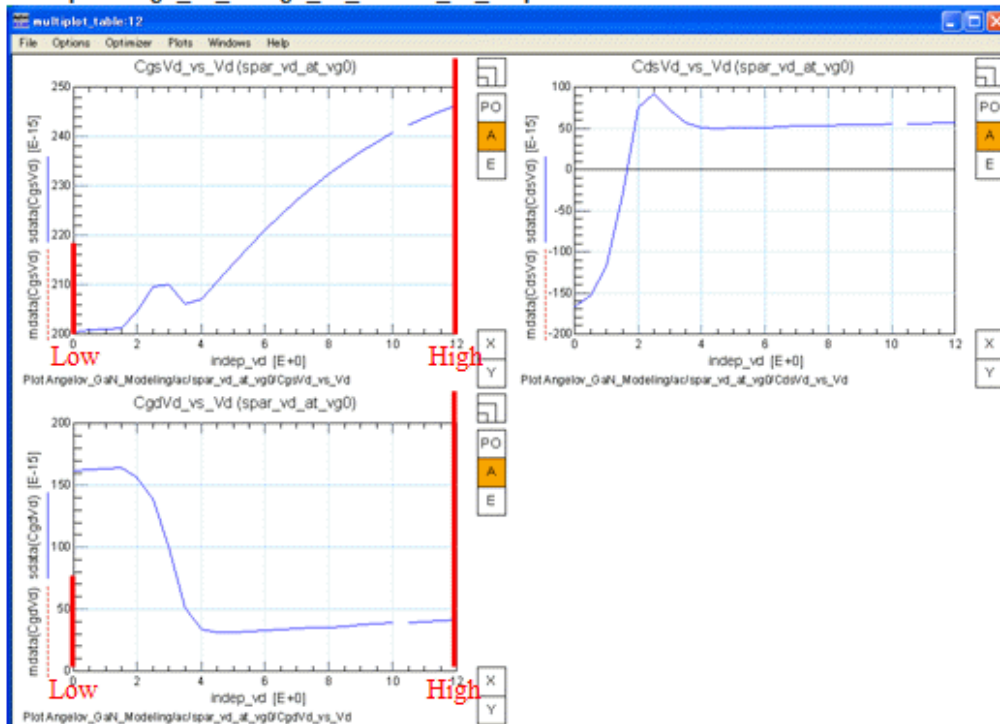
Example of prompt (input low bias)

Enter the lower voltage of vd to extract capacitances.

Example of prompt (input high bias)

Enter the higher voltage of vd to extract capacitances.

Example of $C_{gs_vs_Vd}/C_{gd_vs_Vd}/C_{ds_vs_Vd}$ plot



SP vg at vd0 A1

Once the initial Extraction of Cgs, Cgd and Cds are over, the next steps are the optimization of capacitance characteristics and S-Parameter in order. Here, first adjust the capacitance characteristics when Vd=0.

1. Optimize **CGSPI**, **CGDPI**, **CGS0**, **CGD0**, **CDS**, **P10**, **P11**, **P40** and **P41** using O: CGS,CGD{+}{_}.

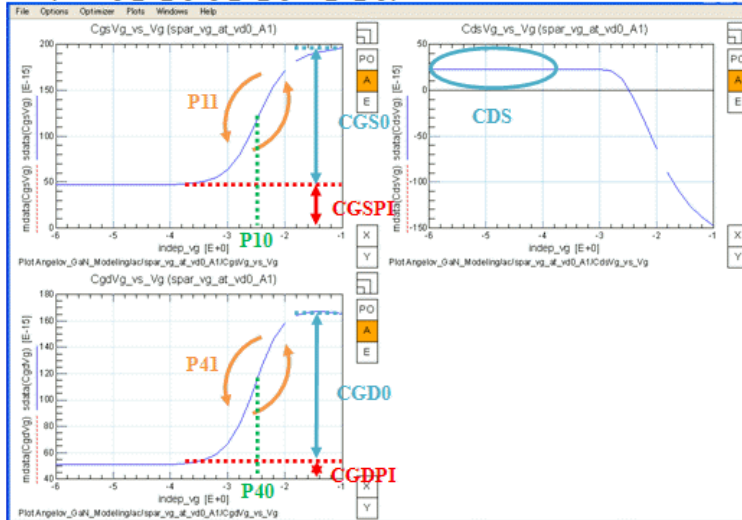
Adjust the characteristics using

CGSPI, **CGS0**, **P10** and **P11**, keeping Cgs in view

CGDPI, **CGD0**, **P40** and **P41**, keeping Cgd in view

CDS, keeping Cds in view

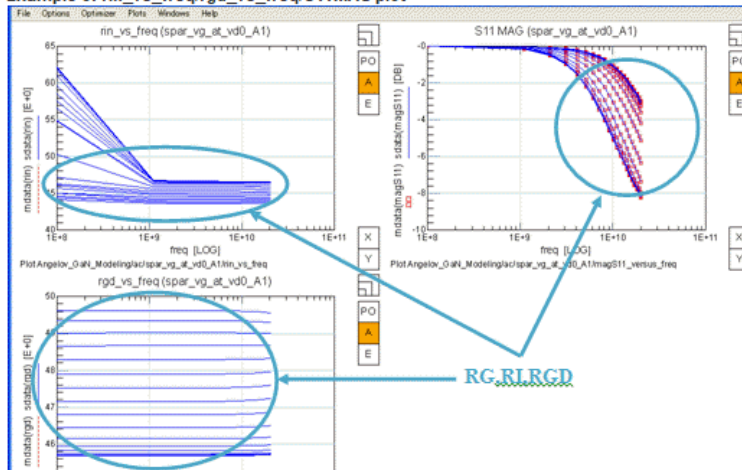
Example of Cgs_vs_Vg/Cgd_vs_Vg/Cds_vs_Vg plot



2. Optimize **RG**, **RI** and **RGD** using O: RG,RI,RGD{+}{_}.

Keeping Rin, rgd and magS11 in view, adjust on the whole using **RG**, **RI** and **RGD**.

Example of rin_vs_freq/rgd_vs_freq/S11MAG plot



SP vd at vg0

Next go on implementing the optimization of capacitance characteristics and S-Parameter at $V_g=0$.

1. Optimize **CGSPI**, **CGDPI**, **CGS0**, **CGD0**, **CDS**, **P20**, **P21**, **P30** and **P31** using O: CGS, CGD

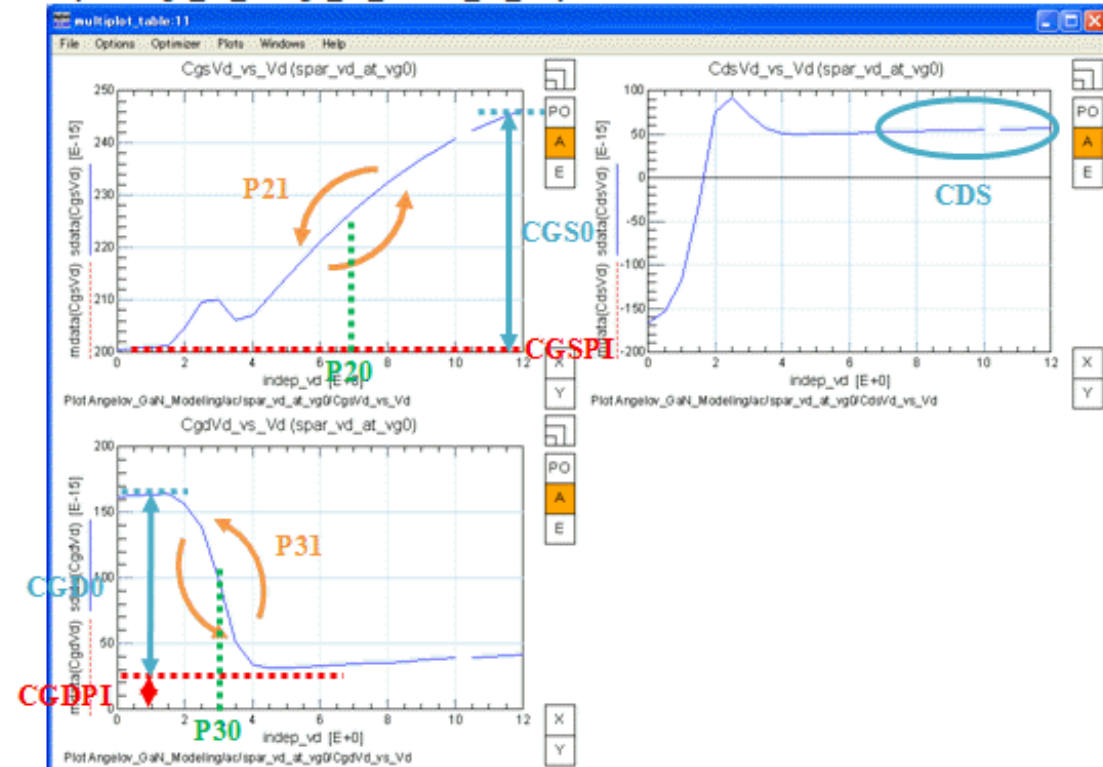
Adjust the characteristics using

CGSPI, **CGS0**, **P20** and **P21**, keeping Cgs in view

CGDPI, **CGD0**, **P30** and **P31**, keeping Cgd in view

CDS, keeping Cds in view

Example of Cgs_vs_Vd/Cgd_vs_Vd/Cds_vs_Vd plot



SP vd at vgm2

Finally, go on implementing the optimization of capacitance characteristics and S-Parameter with Target bias.

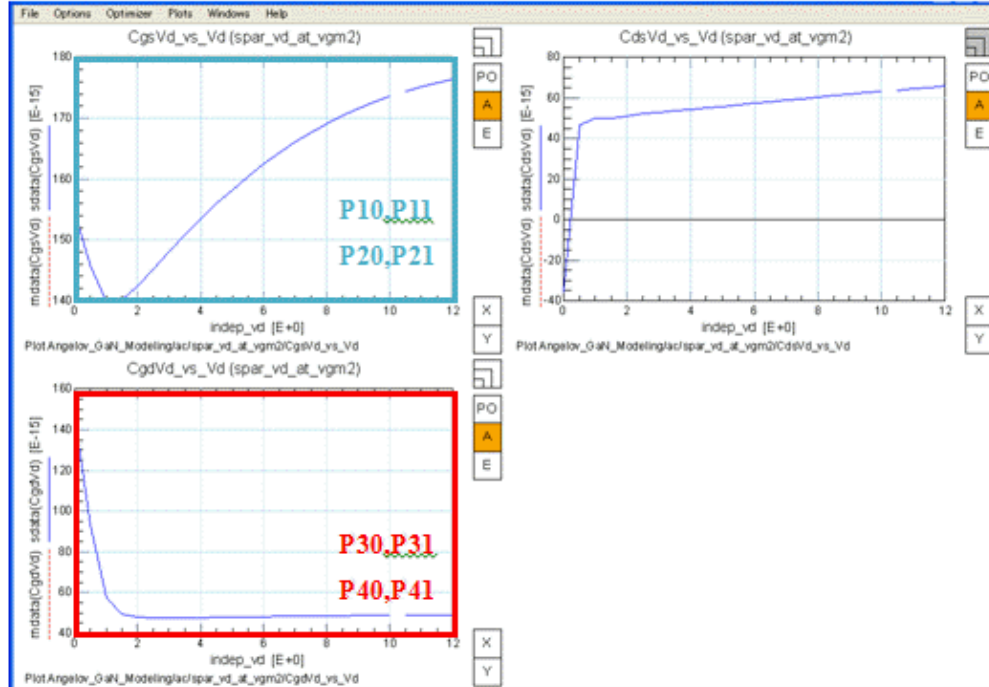
1. Optimize **P10, P11, P20, P21, P30, P31, P40** and **P41** using T: CGS,CGD{+}{_}.

Adjust the characteristics using

P10, P11, P20 and **P21**, keeping Cgs in view

P30, P31, P40 and **P41**, keeping Cgd in view

Example of Cgs_vs_Vd/Cgd_vs_Vd/Cds_vs_Vd plot



2. Optimize **CGSPI, CGDPI, CGS0, CGD0, CDS, P10, P11, P20, P21, P30, P31, P40** and **P41** using T: C_all{+}{_}.

Adjust the characteristics using

CGSPI, CGS0, P10, P11, P20 and **P21**, keeping magS11, phaseS11 and Cgs in view

CGDPI, CGD0, P30, P31, P40 and **P41**, keeping magS22, phaseS22 and Cgd in view

CDS keeping in view Cds

Example of S-para/Cgs_vs_Vd/Cgd_vs_Vd/Cds_vs_Vd/rin/rgd plot

