Description	UAL code				Bits																Flags			
	Instruction	operandes			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	C	V	N	Z
Logical Shift Left	LSLS	Rd	Rm	imm5	0	0	0	0	0	imm5					Rn			Rd			x		x	x
Logical Shift Right	LSRS	Rd	Rm	imm5	0	0	0	0	1	imm5					Rn			Rd			x		x	x
Arithmetic Shift Right	ASRS	Rd	Rm	imm5	0	0	0	1	0	imm5					Rn			Rd			x		x	x
Shift, add, sub, mov					S																			
Add register	ADDS	Rd	Rn	Rm	0	0	0	1	1	0	0	Rm			Rn			Rd			x	x	x	x
Substract register	SUBS	Rd	Rn	Rm	0	0	0	1	1	0	1	Rm			Rn			Rd			x	x	x	x
Add 3-bit immediate	ADDS	Rd	Rn	imm3	0	0	0	1	1	1	0	imm3			Rn			Rd			x	x	x	x
Sub stract 3-bit immediate	SUBS	Rd	Rn	imm3	0	0	0	1	1	1	1	imm3			Rn			Rd			x	x	x	x
Move	MOVS	Rd	imm8		0	0	1	0	0	Rd		imm8											x	x
Compare	CMP	Rd	imm8		0	0	1	0	1	Rd		imm8									x	x	x	x
Add 8-bit immediate	ADDS	Rdn	imm8		0	0	1	1	0	Rdn		imm8									x	x	x	x
Subtract 8-bit immediate	SUBS	Rdn	imm8		0	0	1	1	1	Rdn		imm8									x	x	x	x
Data processina					0	1	0	0	0	opcode														
Bitwise AND	ANDS	Rdn	Rm		0	1	0	0	0	0	0	0	0	0	Rm			Rdn			0		x	x
Exclusive OR	EORS	Rdn	Rm		0	1	0	0	0	0	0	0	0	1	Rm			Rdn			0		x	x
Logical Shift Left	LSLS	Rdn	Rm		0	1	0	0	0	0	0	0	1	0	Rm			Rdn			x		x	x
Logical Shift Right	LSRS	Rdn	Rm		0	1	0	0	0	0	0	0	1	1	Rm			Rdn			x		x	x
Arithmetio Shift Right	ASRS	Rdn	Rm		0	1	0	0	0	0	0	1	0	0	Rm			Rdn			x		x	x
Add with Carry	ADCS	Rdn	Rm		0	1	0	0	0	0	0	1	0	1	Rm			Rdn			x	x	x	x
Substract with Carry	SBCS	Rdn	Rm		0	1	0	0	0	0	0	1	1	0	Rm			Rdn			x	x	x	x
Rotate Right	RORS	Rdn	Rm		0	1	0	0	0	0	0	1	1	1	Rm			Rdn			x		x	x
Set Flags on bitwise AND	TST	Rn	Rm		0	1	0	0	0	0	1	0	0	0	Rm			Rn					x	x
Reverse Subtract from 0	RSBS	Rd	Rn		0	1	0	0	0	0	1	0	0	1	Rn			Rd			x	x	x	x
Compare Registers	CMP	Rn	Rm		0	1	0	0	0	0	1	0	1	0	Rm			Rn			x	x	x	x
Compare Negative	CMN	Rn	Rm		0	1	0	0	0	0	1	0	1	1	Rm			Rn			x	x	x	x
Logical OR	ORRS	Rdn	Rm		0	1	0	0	0	0	1	1	0	0	Rm			Rdn					x	x
Multiply Two Registers	MULS	Rdm	Rn		0	1	0	0	0	0	1	1	0	1	Rn			Rdm					x	x
Bit Clear	BICS	Rdn	Rm		0	1	0	0	0	0	1	1	1	0	Rm			Rdn					x	x
Bitwise NOT	MVNS	Rd	Rm		0	1	0	0	0	0	1	1	1	1	Rm			Rd					x	x
Load / Store					1	0	0	1	opcode															
Store Register	STR	Rt	SP	imm8	1	0	0	1	0	Rt		imm8												
Load Register	LDR	Rt	SP	imm8	1	0	0	1	1	Rt		imm8												
Miscellaneous 16-bit instructions					1	0	1	1	opcode															
Add Immediate to SP	ADD	SP	imm7		1	0	1	1	0	0	0	0	0	imm7										
Subtract Immediate from SP	SUB	SP	imm7		1	0	1	1	0	0	0	0	1	imm7										
Conditional Branch	B				1	1	0	1	cond					imm8										
égalité	BEQ	label			1	1	0	1	0	0	0	0	imm8											
différence	BNE	label			1	1	0	1	0	0	0	1	imm8											
retenue	BCS	label			1	1	0	1	0	0	1	0	imm8											
pas de retenue	BCC	label			1	1	0	1	0	0	1	1	imm8											
négatif	BMI	label			1	1	0	1	0	1	0	0	imm8											
positif ou nul	BPL	label			1	1	0	1	0	1	0	1	imm8											
dépassement de capacité	BVS	label			1	1	0	1	0	1	1	0	imm8											
pas de dépassement de capacité	BVC	label			1	1	0	1	0	1	1	1	imm8											
supérieur (non signé)	BHI	label			1	1	0	1	1	0	0	0	imm8											
inférieur ou égal (non signé)	BLS	label			1	1	0	1	1	0	0	1	imm8											
supérieur ou égal (signé)	BGE	label			1	1	0	1	1	0	1	0	imm8											
inférieur (signé)	BLT	label			1	1	0	1	1	0	1	1	imm8											
supérieur (signé)	BGT	label			1	1	0	1	1	1	0	0	imm8											
inférieur ou égal (signe)	BLE	label			1	1	0	1	1	1	0	1	imm8											
toujours vrai	B ou BAL	label			1	1	0	1	1	1	1	0	imm8											