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SAN JOSE STATE UNIVERSITY COLLEGE OF ENGINEERING

Introduction to NMOS Digital Logic

COLLEGE OF ENGINEERING SAN JOSE STATE UNIVERSITY

Introduction to NMOS Digital Logic

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Thanks to Professor David Parent for the template, resources and opportunity to make this tutorial and San Jose State for the resources.

Chapter 1: Introduction to NMOS FETs

To complete this project, you will simulate, build, test, and document a circuit that demonstrates basic functions of an NMOS FET, and the voltage across the gate and source controls the drain source current as shown by equation x, and they are three models of the transistor based on the equation. The first model is an open circuit when the V_{GS} is less than the threshold voltage, the second model is linear V_{GS} is more than the threshold voltage and the difference of V_{GS} and the threshold voltage more than the V_{DS}, and the third model is in saturation and is when V_{GS} is more than the threshold voltage and the difference of V_{GS} and the threshold voltage less than the V_{DS}. The threshold voltage depends on the doping of the substrate, thickness of the oxide and the gate metal.

$$I_{ds} = \begin{cases} 0 \; if \; V_{th} < V_{GS} \\ \frac{W}{L} C_{ox} \mu \left(V_{DS}(V_{GS} - V_{TH}) - \frac{V_{DS}^2}{2} \right) if \; V_{th} > V_{GS} \; and \; V_{DS} < V_{GS} - V_{TH} \\ \frac{W}{2L} C_{ox} \mu (V_{GS} - V_{th})^2 \; if \; V_{th} > V_{GS} \; and \; V_{DS} \geq V_{GS} - V_{TH} \end{cases} \text{ (Equation 1)}$$

The simulations will be run from the files from this folder and uncompress the ZIP file, and three simulations will be used to show the characteristics of an NMOS.

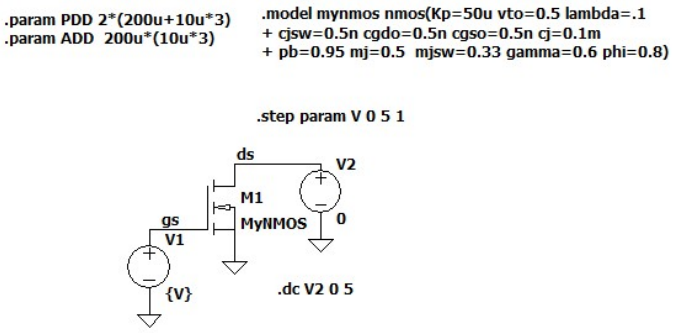

Fig. 1 NMOS circuit to show the V_{DS} vs I_{DS} curves to make inverters and other logic gates in file 20250717 NMOS FET testing varying VDS

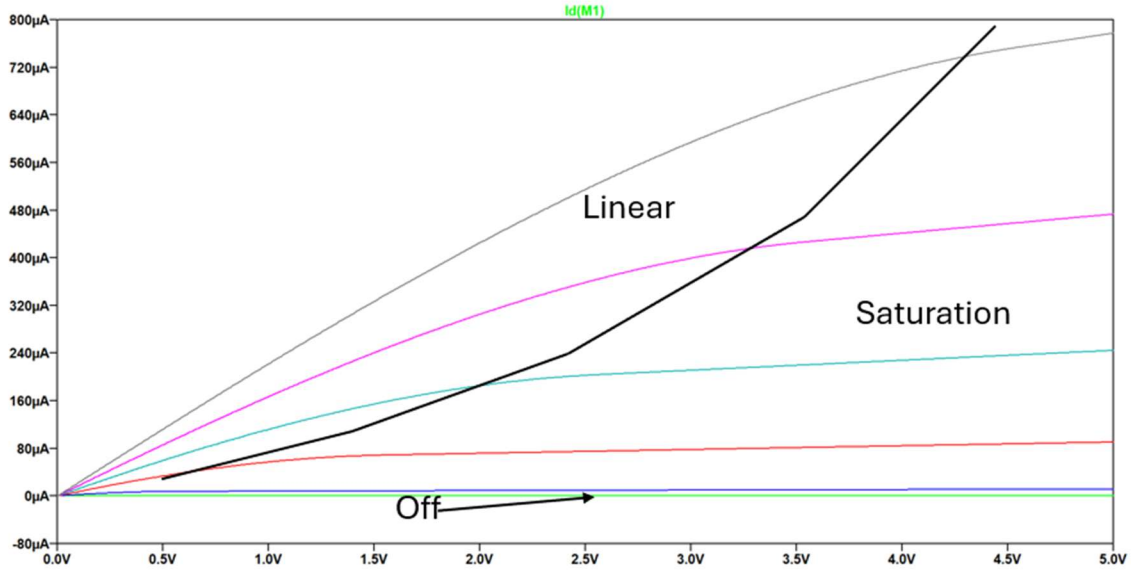

Fig. 2 DC simulation of V_{DS} and I_{DS} to see the curves needed to make an inverter

```
.param PDD 2*(200u+10u*3)
.param ADD  200u*(10u*3)
.model mynmos nmos(Kp=50u vto=0.5 lambda=.1
+ cjsw=0.5n cgdo=0.5n cgso=0.5n cj=0.1m
+ pb=0.95 mj=0.5  mjsw=0.33 gamma=0.6 phi=0.8)
```

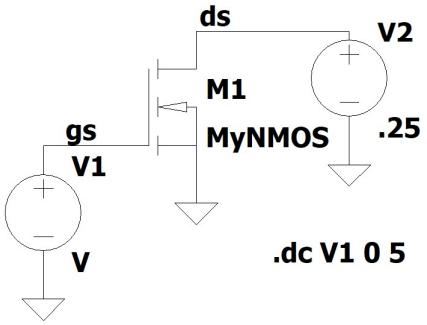

Fig. 3. Set up to vary V_{GS} and hold V_{DS} in 20250717 NMOS FET testing with steady VDS to show when the transistor is only on and in linear mode and can extract threshold voltage

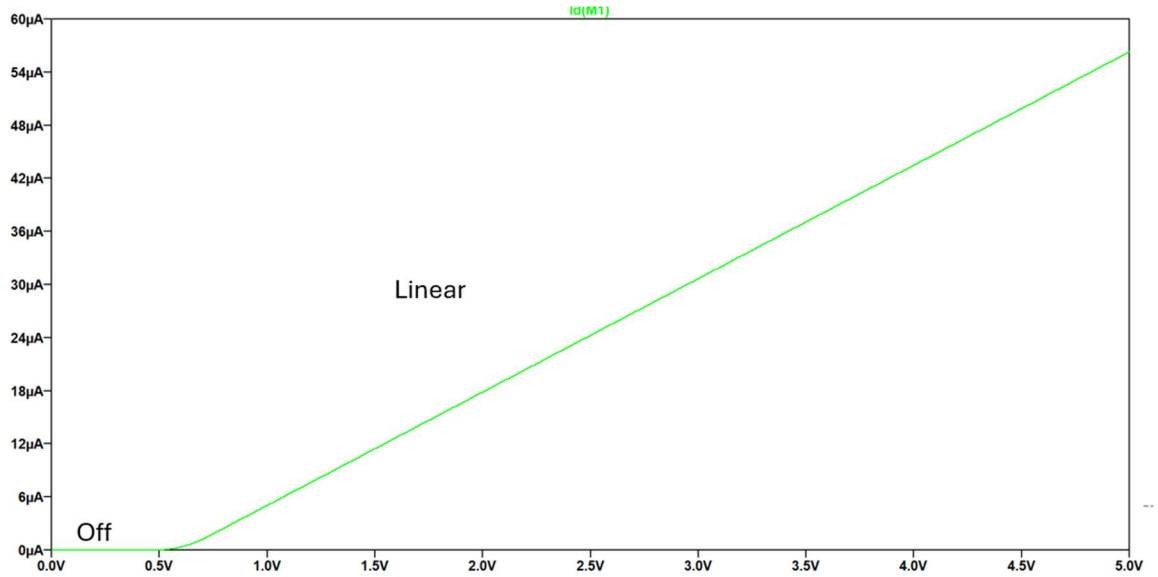

Fig. 4 DC simulation of NMOS to make the curve for I_{DS} with V_{ds} at .25V as a standard

Chapter 2: Introduction to NMOS Logic Gates

Introduction

This lab will show you how to create input vs output simulations of NMOS logic gates and show the improvements with each circuit design.

Objective

After successfully completing the work outlined in this lab, students should be able to use LTspice to generate common signals to test NMOS logic gates.

Theory:

Logic gates (NOR, NAND and NOT gates) create some of the basic building blocks for digital logic and are needed to compute operations in Boolean algebra, and the simplest model is to use is truth tables. The issue is making sure the logic gates are performing as close to ideal as possible.

Table 1: Truth Table for NOT Gate

Input	Output
0	1
1	0

Table 2: Truth Table for NOR Gate

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Table 2: Truth Table for NAND Gate

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

LTspice simulations for NMOS Logic Gates:

The first set of simulations for the NMOS Logic Gates is the NOT Gate or Inverters, To test the NOT gates, run both the file with the dc sweep (20250717 Inverter Testing DC) and transient response (20250717 Inverter Testing transient) to test the inverters to show that the gain it crosses one or negative one and then returns to 0 signals a change a logic level. The region below where the gain crosses negative one and back act the most ideal when the region minimum is the smallest and the width is the shortest, because that is the best way to prevent noise from having the output of the inverter not being in logic high or low. The transient response is to see results of the truth tables over time.

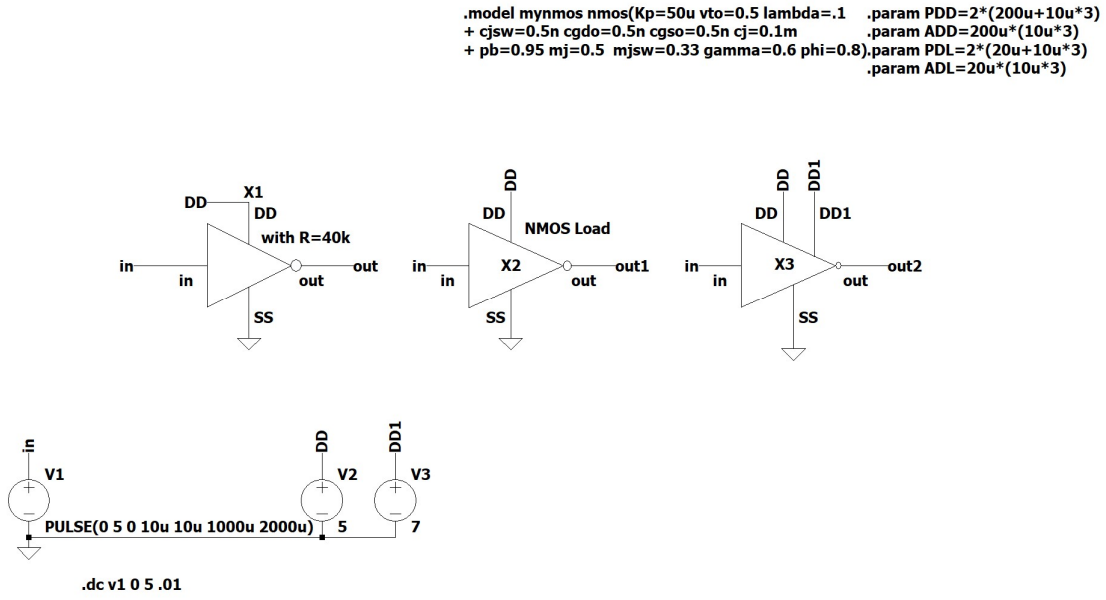

Fig. 5 NOT gate testing schematic, with the leftmost with the load as a resistor, the middle with a NMOS FET diode connected load, and the rightmost with a NMOS FET with the load gate higher than the load drain as to make sure it is in saturation and the dc sweep of the input in file 20250717 Inverter Testing DC

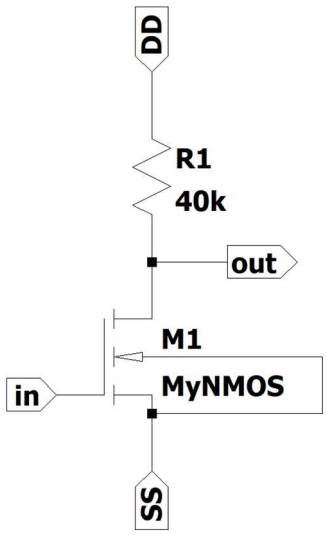

Fig. 6 Schematic of the NMOS inverter with a load resistor

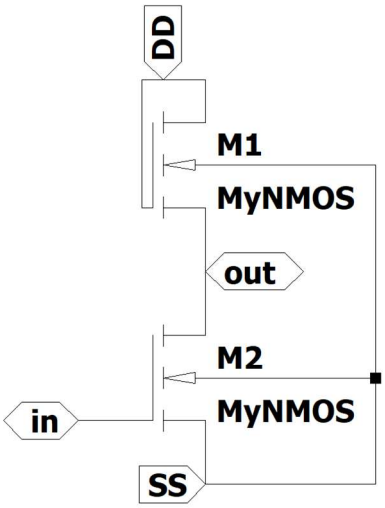

Fig. 7 Schematic of the NMOS inverter with the gate and drain of the load NMOS connected

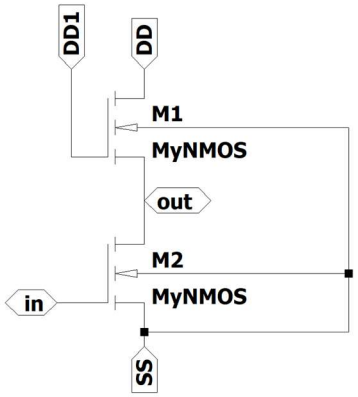

Fig. 8 Schematic of the NMOS inverter with the gate and drain of the load NMOS connected

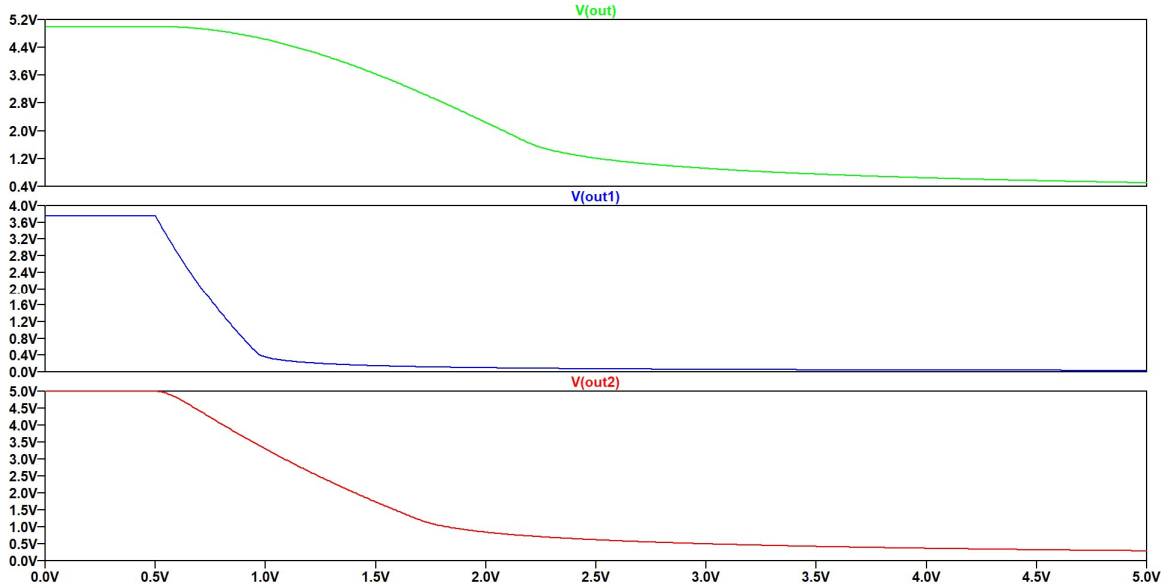

Fig. 9 Results of Fig. 5 with top showing the result for the inverter with the load resistor, middle showing the result for the inverter with the load NMOS diode connected, the bottom showing the result for the inverter with the load NMOS not diode connected

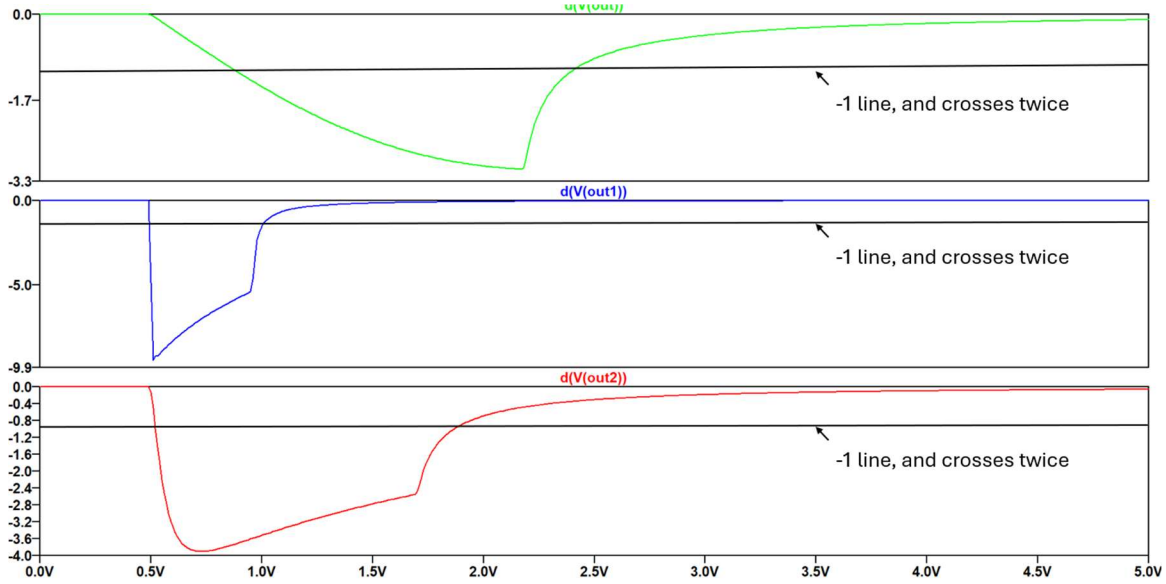

Fig. 10 Results of Fig. 5 and plotting the gain vs input with top showing the result for the inverter with the load resistor, middle showing the result for the inverter with the load NMOS diode connected, the bottom showing the result for the inverter with the load NMOS not diode connected

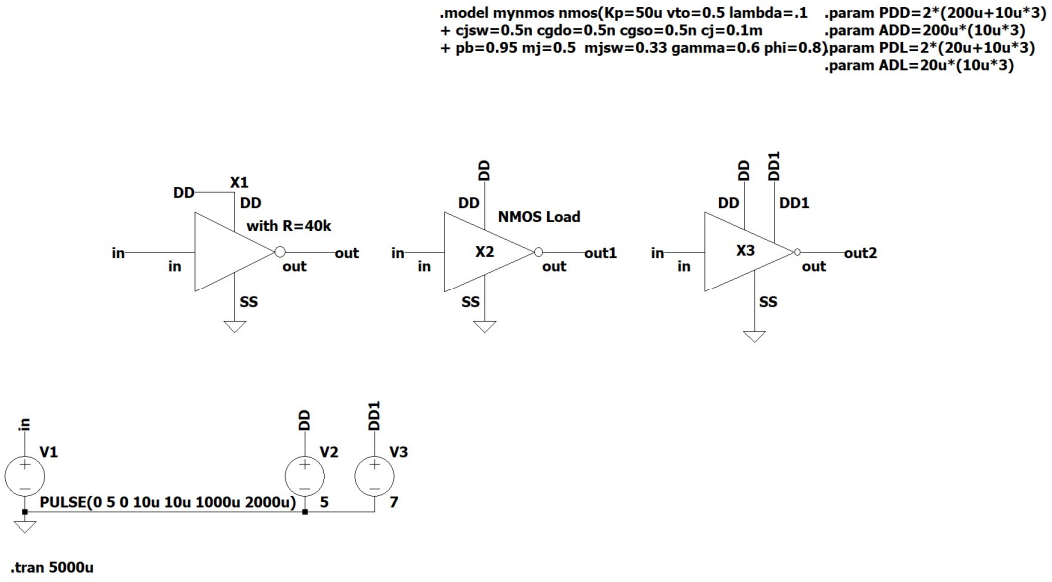

Fig. 11 NOT gate testing schematic, with the leftmost with the load as a resistor, the middle with a NMOS FET diode connected load, and the rightmost with a NMOS FET with the load gate higher than the load drain as to make sure it is in saturation and the pulse response of the input in file 20250717 Inverter Testing transient

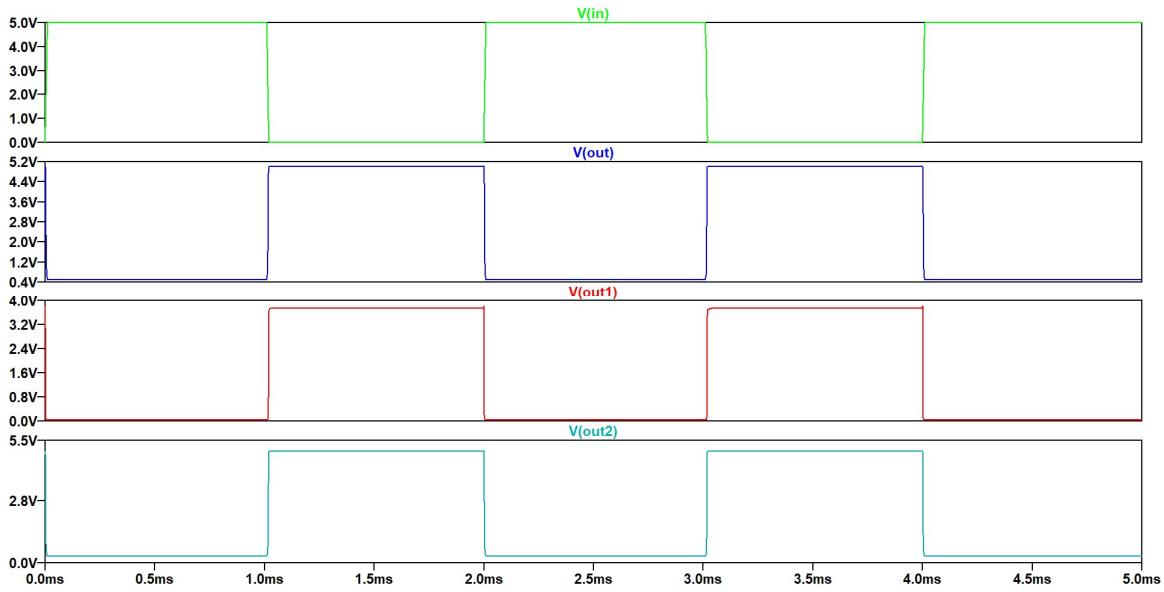

Fig. 12 Results of Fig. 11 with top showing the input, the second highest the result for the inverter with the load resistor, the second lowest showing the result for the inverter with the load NMOS diode connected, the bottom showing the result for the inverter with the load NMOS not diode connected

The second set of simulations for the NMOS Logic Gates is the NOR gates, and to test the NOR gates, run transient command to test the NOR gates plus the derivative of the output because when it crosses one or negative one and goes back to zero, it can signal a change in logic level. The file name is 20250717 NOR gate testing.

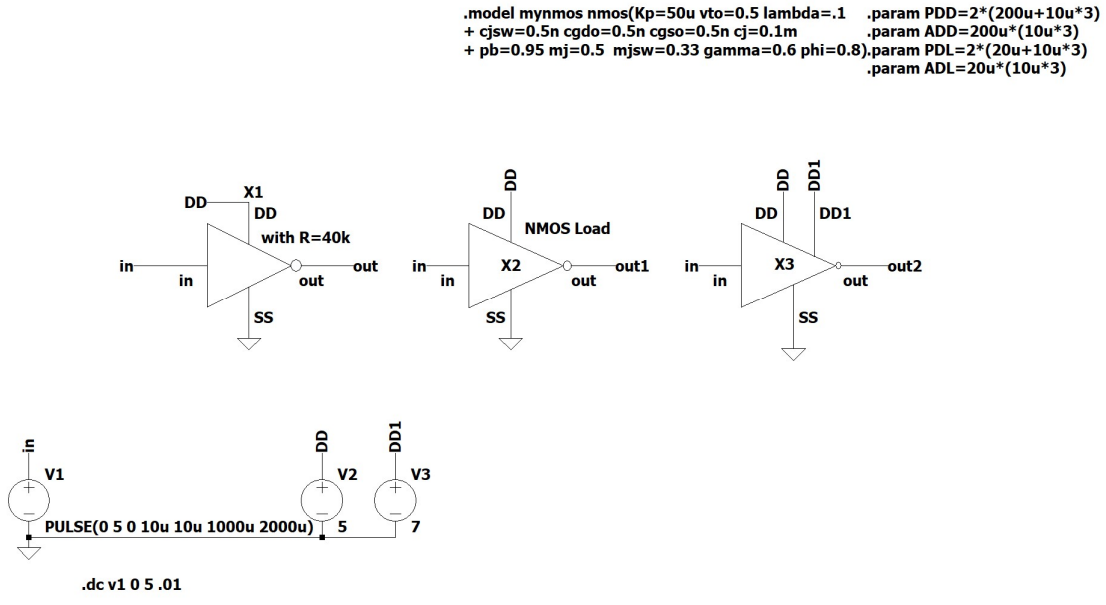

Fig. 13 NOR gate testing schematic, with the leftmost with the load as a resistor, the middle with a NMOS FET diode connected load, and the rightmost with a NMOS FET with the load gate higher than the load drain as to make sure it is in saturation

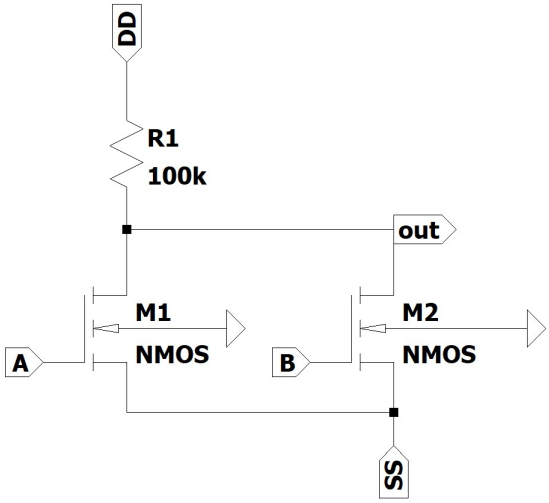

Fig. 14 Schematic of the NMOS NOR gate with a load resistor

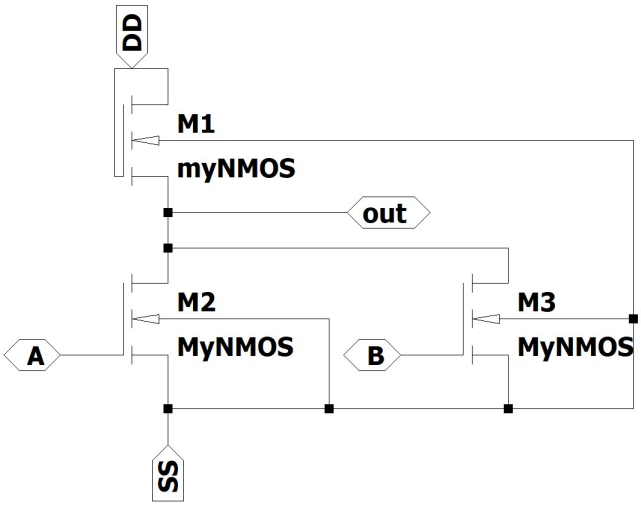

Fig. 15 Schematic of the NMOS NOR gate with the gate and drain of the load NMOS connected

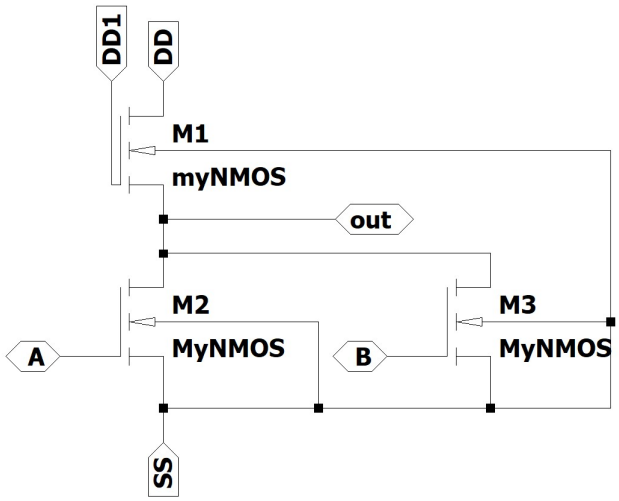

Fig. 16 Schematic of the NMOS NOR gate with the gate and drain of the load NMOS connected

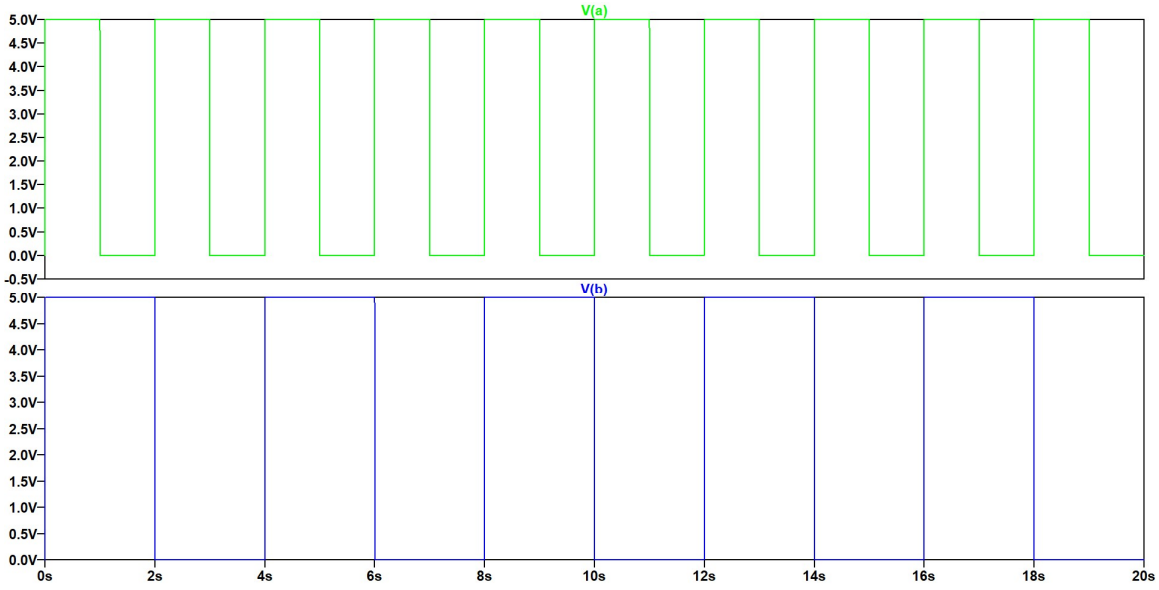

Fig. 17 Results of Fig 13 for the NMOS NOR gate showing the inputs

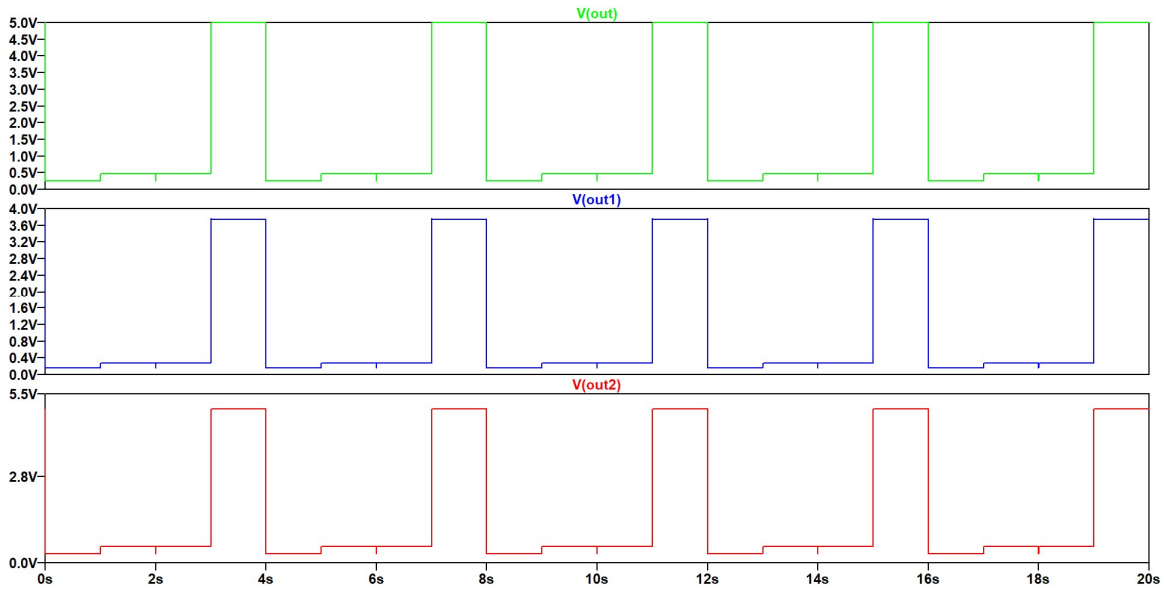

Fig. 18 Results of Fig 13 for the NMOS NOR gate showing the outputs, with the top one being the load resistor, the middle the load NMOS is diode connected and the bottom the load NMOS is not diode connected

The reason why the logic low has two voltages is due to both NMOS inputs being on vs only one with the line in between the switch of one transistor being on, and logic low having two voltages are due to the switch of the transistors since the load is always on.

The third set of simulations for the NMOS Logic Gates is the NAND gates, and to test the NAND gates, run transient command to test the NAND gates plus the derivative of the output because when it crosses one or negative one and goes back to zero, it can signal a change in logic level. The file name is 20250717 NAND gate testing.

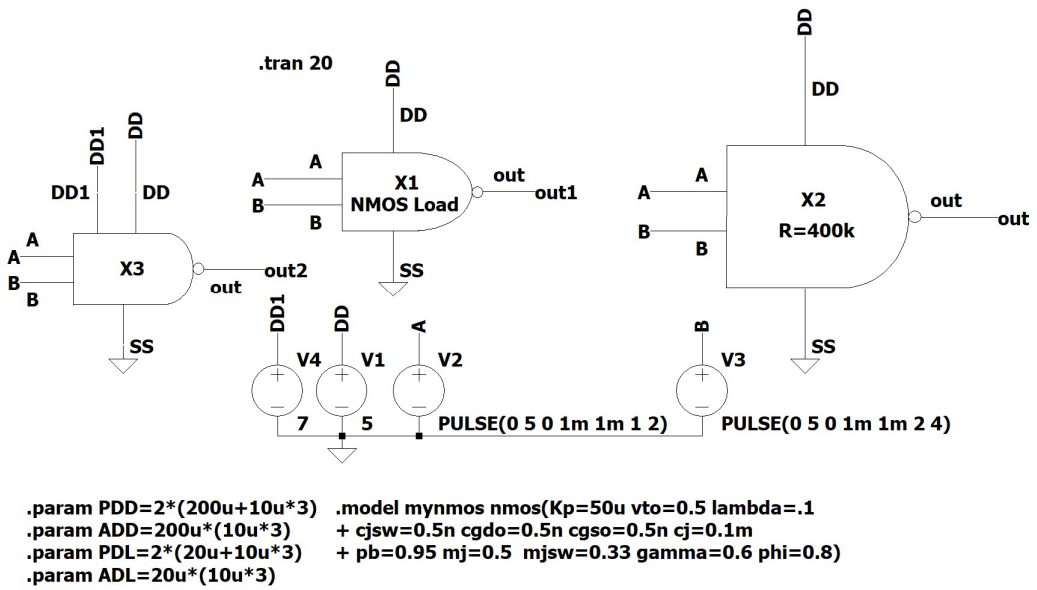

Fig. 19 NMOS NAND gate testing schematic, with the leftmost with the load as a resistor, the middle with a NMOS FET diode connected load, and the rightmost with a NMOS FET with the load gate higher than the load drain as to make sure it is in saturation

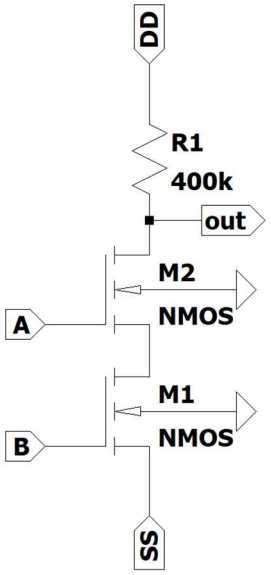

Fig. 20 Schematic of the NMOS NAND gate with a load resistor

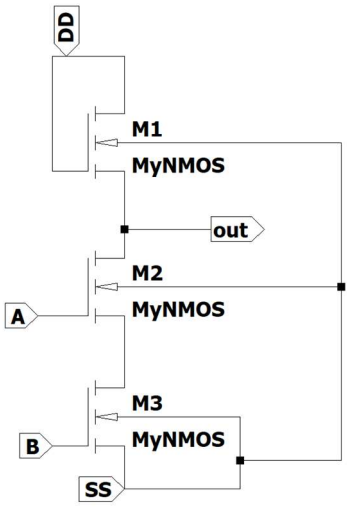

Fig. 21 Schematic of the NMOS NAND gate with the gate and drain of the load NMOS connected

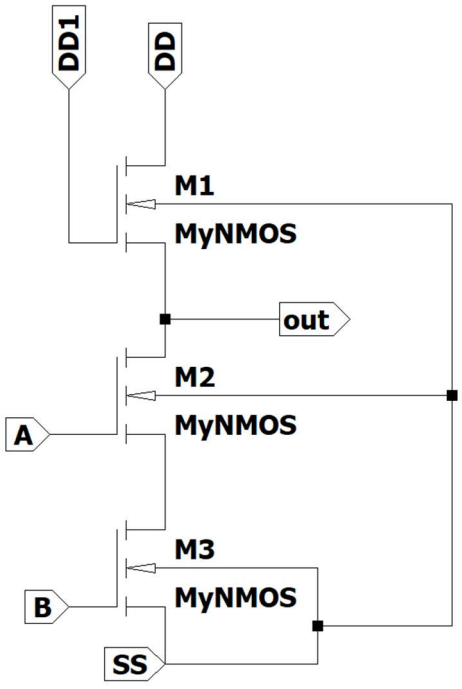

Fig. 22 Schematic of the NMOS NAND gate with the gate and drain of the load NMOS connected

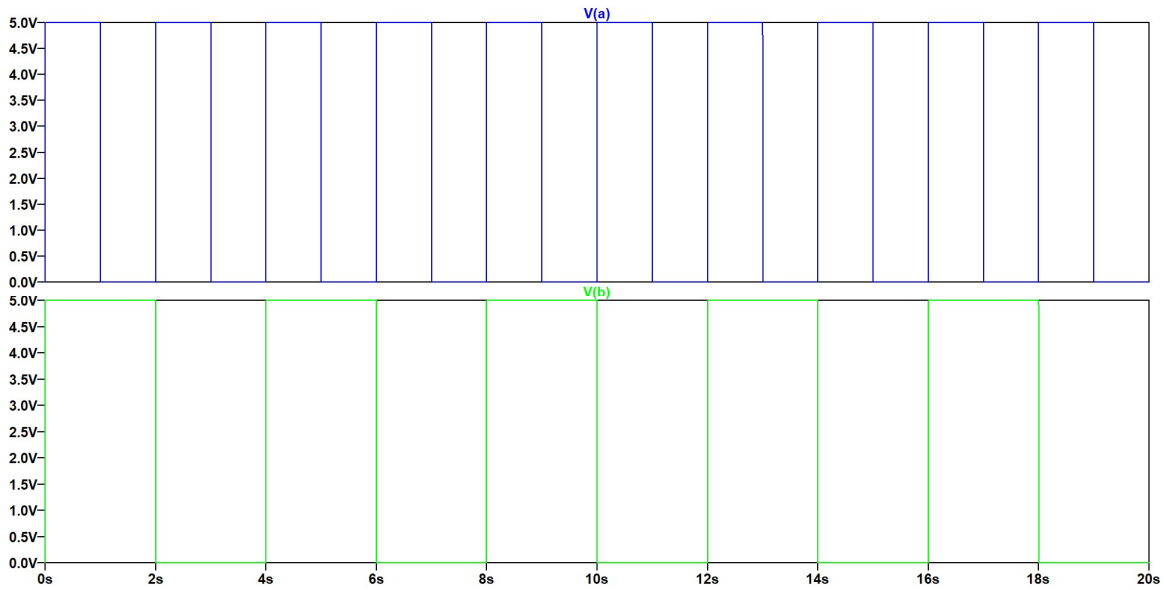

Fig. 23 Results of Fig 19 for the NMOS NAND gate showing the inputs

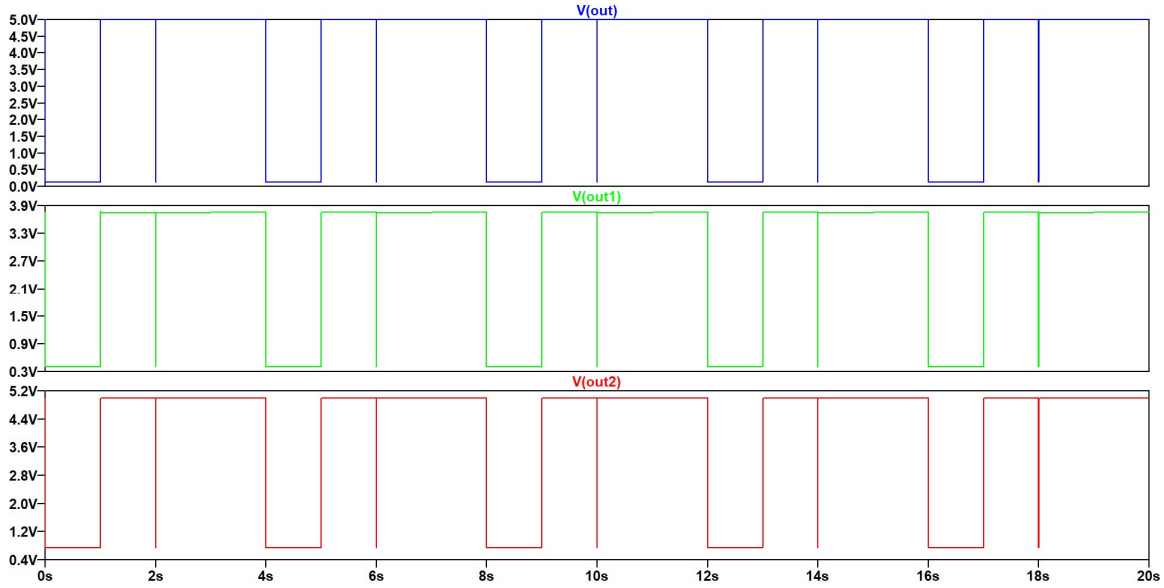

Fig. 24 Results of Fig 19 for the NMOS NAND gate showing the outputs, with the top one being the load resistor, the middle the load NMOS is diode connected and the bottom the load NMOS is not diode connected

The reason for random logic shifts where they are not supposed during the switch of transistors and for a moment none being on is because of the load being always on.

Chapter 3: Introduction to Traditional NMOS SRAM

Project: NMOS SRAM

Introduction

This lab will show you how to test a traditional NMOS SRAM with a clock cycle and having write and reset alternating being off and on

Objective

After successfully completing the work outlined in this lab, students should be able to use LTspice to generate basic input and output curves for an SRAM, using the file 20250717 SRAM testing. The word line acts as the write line, and the bit is the information needed to be stored, so the bit line is twice as fast for this simulation to test all the conditions.

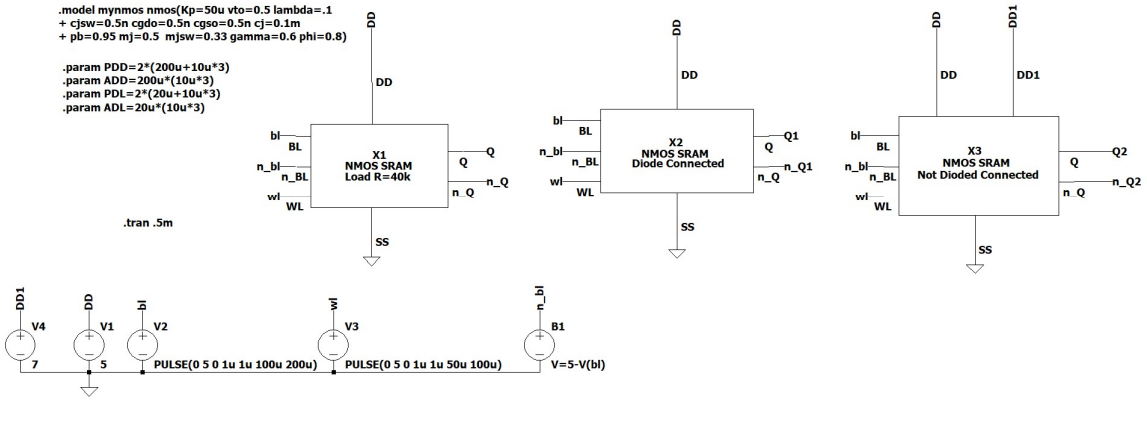

Fig. 25 NMOS SRAM testing schematic, with the leftmost with the load as a resistor, the middle with a NMOS FET diode connected load, and the rightmost with a NMOS FET with the load gate higher than the load drain as to make sure it is in saturation

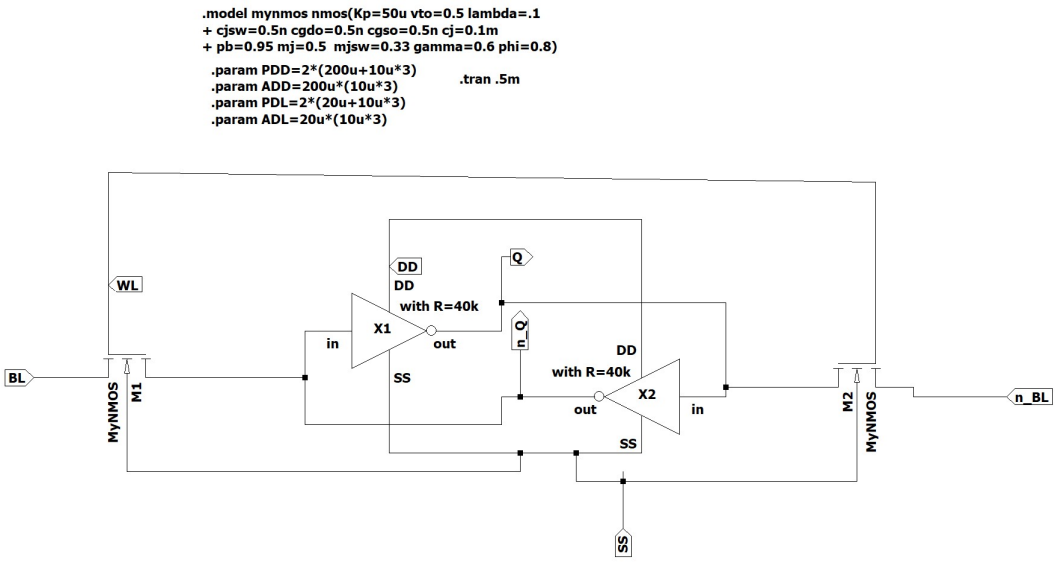

Fig. 26 Schematic of the NMOS SRAM with a load resistor

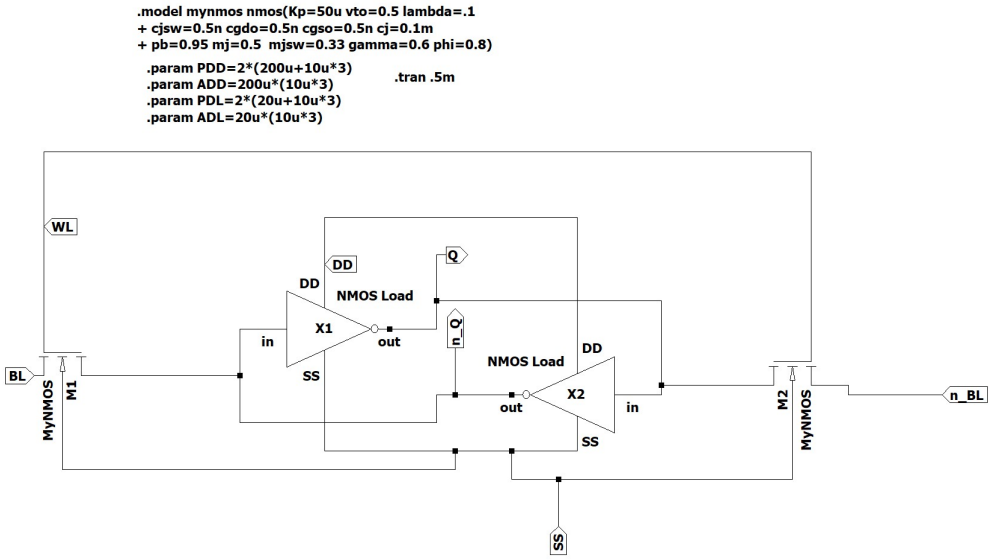

Fig. 27 Schematic of the NMOS SRAM with the gate and drain of the load NMOS connected

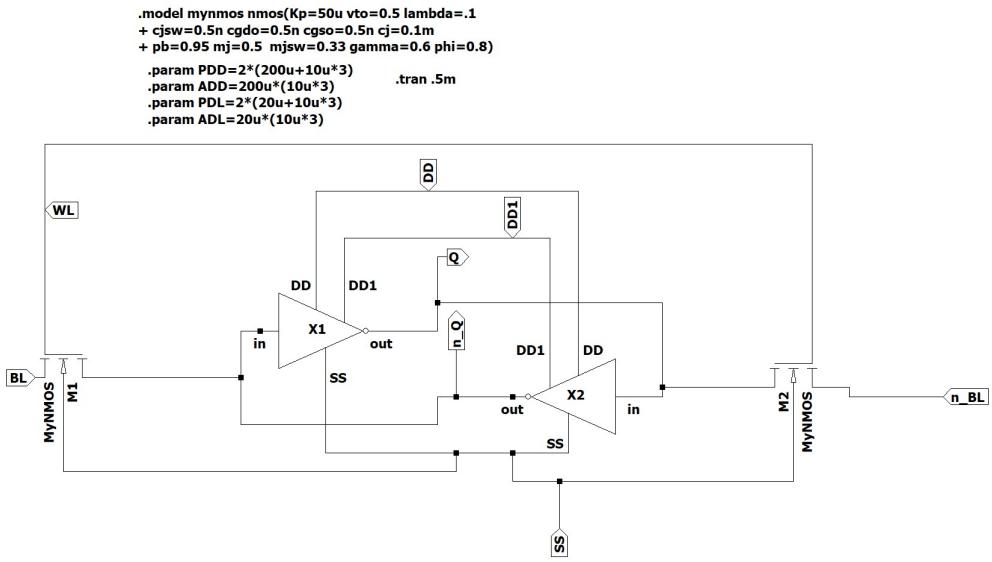

Fig. 28 Schematic of the NMOS SRAM with the gate and drain of the load NMOS connected

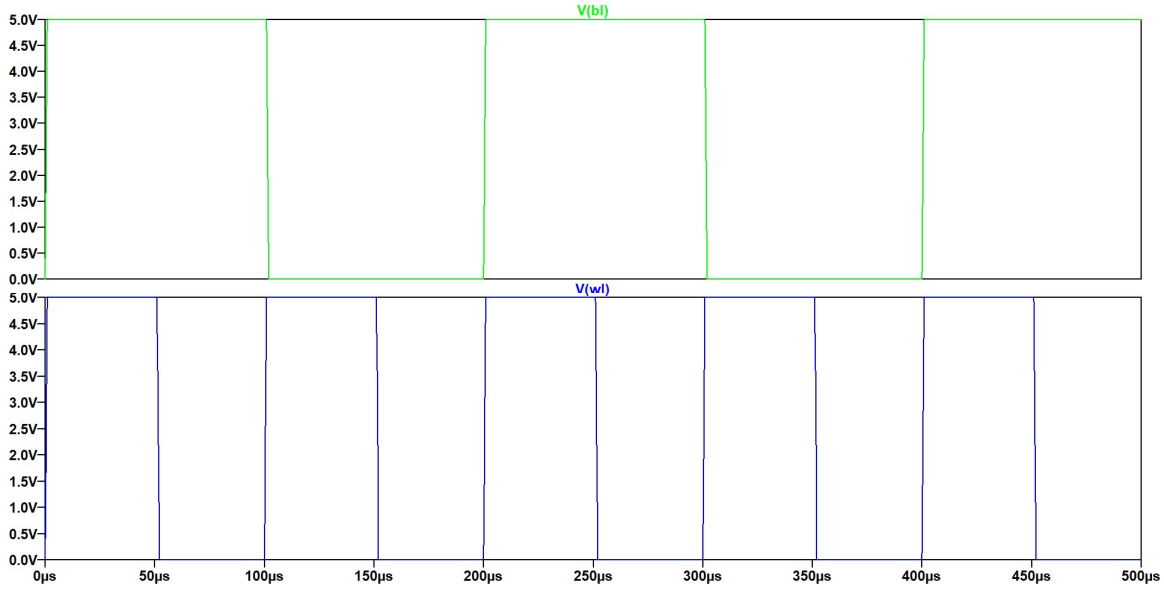

Fig. 29 Results of Fig 25 for the NMOS SRAM showing the inputs

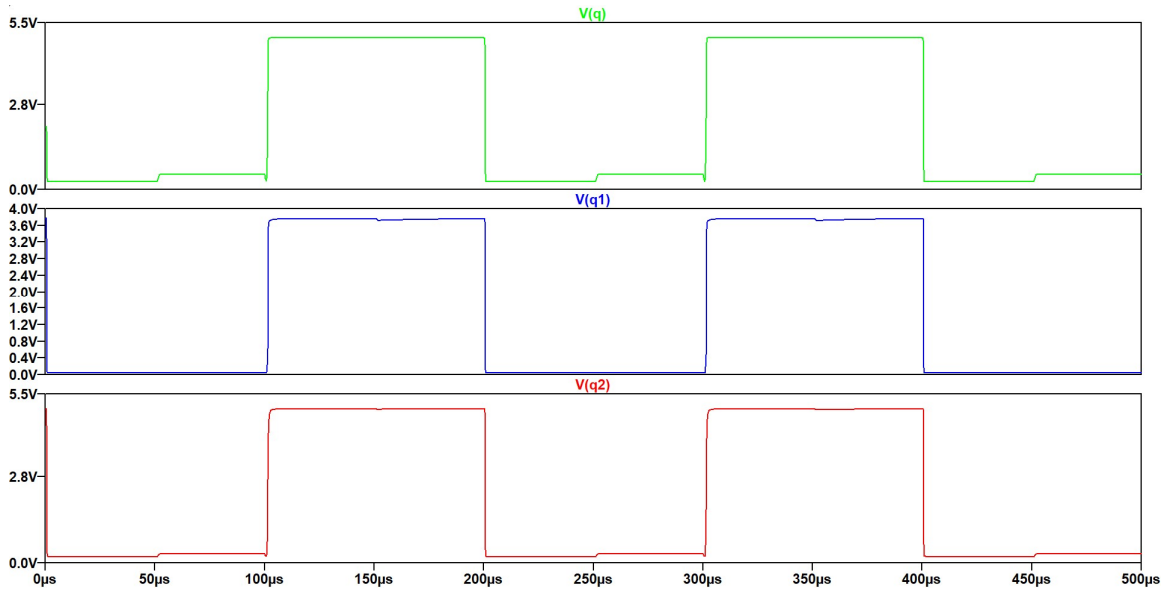

Fig. 30 Results of Fig 25 for the NMOS SRAM gate showing the output, with the top one being the load resistor, the middle the load NMOS is diode connected and the bottom the load NMOS is not diode connected