Chenxi Zhang

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Education

Lund University **September 2024 – present**
Msc.in Integrated Circuits Design, Lunds Tekniska Högskola(LTH) *Lund, Sweden*

Southern University of Science and Technology(SUSTech) **August 2019 – June 2023**
B.Eng.in Microelectronics Science and Engineering, School of Microelectronics; GPA: 3.34/4.0 *ShenZhen, China*

SKILL LIST

HDL:Verilog, SystemVerilog, VHDL
Programming:C/C++, Python, TCL, CMake
EDA Tools:Vivado, Modelsim, Cadence Virtuoso, Genus, Innovus, Spectre, Calibre, Silvaco/Sentaurus, HSPICE, COMSOL

INTERNSHIP

Optical Computing-In-Memory(CIM) Video Processing Chips Design **June 2023 – October 2023**
Research Assistant, School of Microelectronic, SUSTech *Shenzhen, China*

- Design peripheral control circuits for advanced Optoelectronic memristor arrays used for Spiking Neural Network,SNN.
- Design ASIC Chips which process signal from the sensor to finish SSN computation and analyse the efficiency, accuracy and power consumption to assess array performance.

Low Power Vision Processing Chip Design Based on Risc-V Architecture **June 2022 – October 2022**
Digital Circuit R&D Post, Pixelcore shanghai Co., Ltd. *Shanghai, China*

- Verify the Hummingbird 200 series (licensed) four-stage pipelined Risc-V processor add a bus for it.
- Analyse the algorithms to be deployed and improve the design of the three-level pipeline to increase the computational efficiency of special requirements.
- Add an extra convolutional acceleration kernel to improve image processing efficiency.
- Design exception handling module to cope with all kinds of external and internal errors, increase debugging core

PROJECT EXPERIENCE

A Convolution Acceleration Core IP Design | *ASIC Flow* **Spring 2025**

- Based on the Pulpino project, modify its clock and rewrite memory mapping.
- Design a convolutional acceleration kernel under apb bus that implements multi-stripe and multi-padding convolution.
- Synthesise and verify the design at a 100MHz clock frequency.
- Perform layout on the design and verify DRC, ERC, LVS,and DRV, then sign-off.
- Perform post-layout simulation on the properly generated netlist, SPEF and SDF files
- Verified with directed and random testbenches, achieved 100MHz target frequency with no timing violations.

An Area-Delay 4×4-Bits Array Multiplier in 180nm CMOS Technology | *Cadence Virtuoso* **Spring 2022**

- Adopted the array multiplier architecture with 16 ANDs, 4 HAs and 8 FAs.
- Designed the circuit and simulated in schematic level.
- Implemented the physical layout and verified the design through post-layout simulation.
- Improved circuitry and layout for optimal area and latency.
- Achieved a final layout area of 771.0059 nm^2 (L=53.86 nm and W=14.315 nm), which is the smallest of this project.

A 5-stage pipeline Processor based on 32-Bits ISA of ARMv7 | *Verilog, Vivado* **Fall 2021**

- Constructed each module separately and verified them by specific testbench.
- Assembled the processor through definition of wires and instantiation of modules in a top core.
- Upgraded the processor by adding 5-stage pipeline.
- Upgraded the processor by adding an improved sequential multiplier module and modifying other modules accordingly.
- Customized the instruction flow to check all possible conditions.

Honors and Awards

Scholarship

- Nation 2st Prize, Contemporary Undergraduate Mathematical Contest in Modeling (China Society for Industrial and Applied Mathematics) *2022*
- National Encouragement Scholarship (Ministry of Education of the P.R.C.) *2020-2022*
- Second Prize of Freshman Scholarship(TOP 5%,Southern University of Science and Technology) *2019*