Birla Institute of Technology & Science, Pilani

Work Integrated Learning Programmes Division

Second Semester 2020-2021

M.Tech (Data Science and Engineering)

Compre- Regular Exam (EC-3 Makeup)

Course No. : DSECLZG516
Course Title : Computer Organization and Software Systems
Nature of Exam : Open Book
Weightage : 40%
Duration : 2 Hours
Date of Exam : 10/10/2021 (Forenoon 10.00 am to 12.00 pm)

Number of Pages: 5

Number of Questions: 8

Note to Students:

1. **All parts of a question should be answered consecutively. Each answer should start from a fresh page.**
2. **Assumptions** made if any, should be stated clearly at the beginning of your answer.
3. Please follow all the Instructions to Candidates given on the cover page of the answer book
4. For all problems **relevant steps** are to be shown.

Q1 Answer the following Question **[6 Marks]**

A. State whether the below statements are True/False with proper justification(Note: Solution without justification will not be awarded any marks) [3M]

i. Any program with stride-1 reference pattern has good temporal locality.
Sol: False , Program with stride-1 has good spatial locality

ii. Main Memory holds the disk files retrieved from local disks
Sol: False, Main memory holds disk blocks not files at Level L4

iii. Devices with lower hierarchy has longer access time.
Sol: True, it tend to use larger block sizes in order to amortize these longer access times.

B. Consider the following snapshot of the system: [3M]

	Allocation					MAX					Available			
	A	B	C	D		A	B	C	D		A	B	C	D
P0	2	0	0	1		4	2	1	2		3	3	2	1
P1	3	1	2	1		5	2	5	2					
P2	2	1	0	3		2	3	1	6					
P3	1	3	1	2		1	4	2	4					
P4	1	4	3	2		3	6	6	5					

Answer the following questions using the banker's algorithm:

i. Illustrate that the system is in a safe state by demonstrating an order in which the processes may complete.

	Allocation				MAX				Available				Need			
	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
P0	2	0	0	1	4	2	1	2	3	3	2	1	2	2	1	1
P1	3	1	2	1	5	2	5	2	5	3	2	2	2	1	3	1
P2	2	1	0	3	2	3	1	6					0	2	1	3
P3	1	3	1	2	1	4	2	4	6	6	3	4	0	1	1	2
P4	1	4	3	2	3	6	6	5	7	10	6	6	2	2	3	3
									10	11	8	7				
									12	12	8	10				

Safe Sequence P0,P3,P4,P1,P2

ii. If a request from process P1 arrives for (1, 1, 0, 0), can the request be granted immediately?

3 3 2 1 > 1 1 0 0 : Can be granted

iii. If a request from process P4 arrives for (0, 0, 2, 0), can the request be granted immediately?

3 3 2 1 > 0 0 2 0 : Can be granted

Q2 Answer the following Question **[6 Marks]**

A. There is a memory system of Main and Cache memory. If the Main memory access time is 1200nS and cost is INR 0.00001 and the Cache access time is 100nS and cost is INR 0.0001. [6M]

i. What is the cost of 1Mb of main memory using Cache technology?

ii. The hit ratio was 0.90% and an improvement resulted in effective action time enhancement by 14% greater than the cache access time, compute the hit ratio?

iii. If the memory system is added with a disk such that 95% of time it is cache if it misses then 70% of time it is in main memory and if it misses this the disk is accessed and the word is accessed in 12mS with 75nS to copy to the cache and the reference is restarted.

Ans:

A) INR 1*1024*1024*8*0.0001 =INR 838.86

B) we get Ts = T1 +(1-H) (T1+T2)
= 100 + 0.10 * 1300 ns
= 240 ns

Since we need an access efficiency of 114 ns, the hit ratio has to be improved:

114 = 100 + (1-H) * 1300
14/1300 = 1-H

H = 1286/1300 = 98.92%

C) Location of referenced word Probability Total time for access in ns In cache 0.9 *20 Not in cache, but in main memory (0.1)(0.6) = 0.06 ,60 + 20 = 80 ,Not in cache or main memory (0.1)(0.4) = 0.04 12ms + 60 + 20 = 12,000,080 So the average access time would be: Avg = (0.9)(20) + (0.06)(80) + (0.04)(12000080) = 480026 ns

Q3 Answer the following Question **[6 Marks]**

Calculate the average Finish time, average Turnaround time, average waiting time and average response time for the following set of processes in RR with a time quantum of 4 units.

Process	AT	BT		
		CPU	I/O	CPU
P1	0	6	9	4
P2	3	9	5	6
P3	4	3	8	2
P4	6	5	10	5

Sol: recheck

Processes	Arrival Time	CPU-I/O Burst	Finish Time	Waiting time	Turn around	Response Time
P1	**0**	**6+9+4**	29	10	29	0
P2	**3**	**9+5+6**	40	17	37	1
P3	**4**	**3+8+2**	24	7	20	4
P4	**6**	**5+10+5**	41	15	35	7
Average				**12.25**	**30.25**	**3.00**

Q4 Answer the following Question **[5 Marks]**

A. A new application makes the CPU 12 times faster than an earlier version .The application spends 45% of its time in computation and 60% in I/O. There is no

changes made on IO performance. How much enhancement(faster) is the application overall? [2M]

Sol: only 45% is the change so

Overall performance is= 1/((1.0-0.45)+(0.45/12))

= 1((0.55)+ 0.0375)= 0.5875

= 1.70.

B. Consider a Virtual memory systems, that contains a single level paging structure with page size 16 KB and The page table size is 16 KB and entry size of 4 Bytes Calculate the page number, offset and virtual address space. [3M]

Given-

- Page size = 16 KB
- Page table entry size = 4 bytes
- Page table size = 16 KB

Let the number of bits in virtual address = n bits

Number of Bits in Page Offset-

We have,

Page size = 16 KB = 2^{14} B

Thus, Number of bits in page offset = 14 bits

Process Size-

Number of bits in virtual address = n bits

Thus, Process size = 2^n bytes

Number of Pages of Process-

Number of pages the process is divided

= Process size / Page size = 2^n B / 16 KB = 2^n B / 2^{14} B= 2^{n-14} pages

Page Table Size-

Page table keeps track of the frames storing the pages of process.

Page table size = Number of entries in page table x Page table entry size

= Number of pages the process is divided x Page table entry size

= 2^{n-14} x 4 bytes

= 2^{n-14+2} bytes

= 2^{n-12} bytes

But we are given page table size = 16 KB

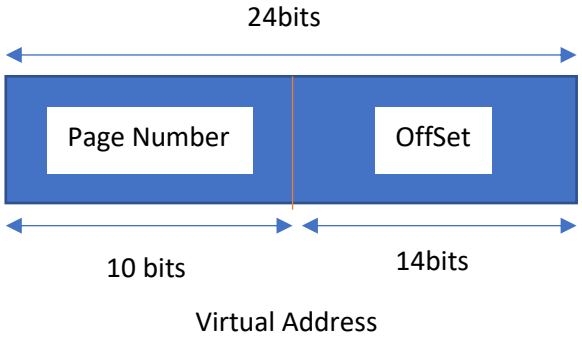
Thus, 2^{n-12} bytes = 4 KB

$2^{n-12} = 2^{12}$

$n - 12 = 12$

$n = 24$

Thus, number of bits in virtual address = 24 bits



Q5 Answer the following Question **[2 Marks]**

A. There are 4 processes that are running on a system currently - Process P1 is an OS initiated Job scheduler. Process P2 is a process that requires frequent interaction of giving inputs based on the last output given by the process. Process P3 is an editor process in which a file is getting edited. Unfortunately, all these three processes are currently in a deadlock waiting for the same resource and Banker's algorithm has detected that the system is currently in a deadlock state. Based on your understanding in the COSS course, if you have to recover these three processes out of the deadlock with minimal impact to the entire system, what would you resort to? WHY? (Note: For the marks to be awarded, the reason has to be correctly stated) [1M]

Solution:

We will abort/terminate the P3 process because this is the lowest priority process among the three processes that are mentioned in the system (Session #11, Slide 6). After the P3 process is terminated, the remaining P1 and P2 processes might get out of the deadlock and run to completion.

B. Your reporting manager is asking you to put your learnings on Operating System in this course to practice by asking you to fine tune the performance of the *Operating System* in the main application server that is running in your organization. For this purpose, you can assume that the hardware for this server is a 16-core machine and is highly optimized already. [1M]

Solution:

Choose between the different process scheduling algorithms and choose the one with least average waiting time and least response time. Since the given hardware is 16-cores, parallelize as much as possible the entire set of applications running on the server with each part bound to a core for having the least clock time of completion. Have a much bigger page size for page faults to be lesser.

Q6 Answer the following Question **[6 Marks]**

A. A computer has 32-bit instructions and 12-bit addresses. Opcode field of the instruction has fixed number of bits. [2M]

i. There are 245 two address instructions. How many one address instructions can be formulated?

ii. Draw instruction format for one address instruction and two address instruction.

Ans –

i) Instruction Length – 32 Bit
Address Field = 12 bit
Therefore opcode field length = 8 bit, total opcode = 2^8 = 256 instructions possible.
Hence one address instruction = (256-245) = 11 instructions

ii) Format of Two Address Instruction

Opcode (8 Bit)	Address (12 bit)	Address (12 bit)

Format of One Address Instruction

Opcode (8 Bit)	Don't care	Address (12 bit)

OR

Opcode (8 Bit)	Address (12 bit)	Don't care

B. Consider the following sequence of addresses(represented in decimal):

100, 0500, 1101, 1999, 3000, 3500, 1024, 2048

Assume 500 byte page. Find out the reference string representing page numbers [1M]

ANS: 0, 1, 3, 4, 7, 8, 3, 5, 7, 7, 9, 10, 12, 6, 3

Given six memory partitions of 100KB, 500KB, 200KB, 300KB, 600KB and 700KB (in order), how would each of the first fit, best fit and worst fit algorithms place processes of 212KB, 417KB,112KB, 426 KB and 545 KB(In order)? Which algorithm makes the most efficient use of memory? Justify your answer. [3M]

Sol: Best fit makes the most efficient use of memory. FF - 545 waiting. WF - 426, 545 waiting.

Q7 Answer the following Question **[6 Marks]**

A. Consider a four stage instruction pipeline (Fetch (F), Decode field (D), Execute (E), and Result Write (W)). As indicated in the table below, each of the five instructions in a given instruction sequence requires these phases for a different number of clock cycles.

Instruction	F	D	E	W
1	1	3	1	1
2	2	1	3	2
3	1	2	2	1
4	1	2	2	1
5	1	2	1	2

a) Draw the Time Space diagram for this pipeline with Time(Tx) on the X-axis and Instructions (Iy) on Y axis or vice versa. [2M]

b) If pipelined, How many Time cycles will be taken for executing these instructions [0.5 M]

c) If non-pipelined, how many time cycles would be needed to execute the instructions? [0.5M]

Solution:

	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13	t14	t15
I1	F	D	D	D	E	W									
I2		F	F		D	E	E	E	W	W					
I3				F		D	D		E	E	W				
I4					F			D	D		E	E	W		
I5						F				D	D		E	W	W

Clock Cycle time for pipeline=15

Clock cycle time for non-pipeline =32

B. Consider the following C programming segment. Assume a;; relevant header files are added in the program.

```
int main()
{
        int p=5;
      for(int i=0; i<p; i++)
     {
```

```
        if(p<5)
          {
                fork();
                fork();
               printf("COSS\n");
           }
      else
           {
              fork();
               printf("Welcome \n");
           }
    }
}
```

i. How many child processes are created? Justify your answer with tree structure [2.5 M]

31 child processes are created and one parent process

ii. How many times "COSS" and "Welcome" will be printed. [0.5M]

COSS = 0 times
Welcome = 32 times

Q8 Answer the following Question **[3 Marks]**

A. State whether the following statements are **True** or **False** with proper justification. Answers without proper justification will not be given any marks

i. Mutex Lock is best suitable for short duration.

Sol: False, Spin Lock is best for short duration of 3-4 cycles.

ii. Spin Lock is held for Longer duration for multi-processing cores

Sol: False, Mutex Lock is best for long term.

iii. Always user level threads have highest priority to use processors

Sol: False, Kernel Threads has higher priority.