Birla Institute of Technology & Science, Pilani

Work Integrated Learning Programmes Division

First Semester 2020-2021

M.Tech (Data Science and Engineering)

Mid-Semester Exam (EC-3 Makeup)

Course No. : DSECLZG516
Course Title : Computer Organization and Software Systems
Nature of Exam : Open Book
Weightage : 30%
Duration : 90 minutes
Date of Exam : 18/07/2021

Number of Pages: 04

Number of Questions: 06

FN (10:00 AM to 12:00 PM)

Note to Students:

1. **All parts of a question should be answered consecutively. Each answer should start from a fresh page.**
2. **Assumptions** made if any, should be stated clearly at the beginning of your answer.
3. For all problems **relevant steps** are to be shown.

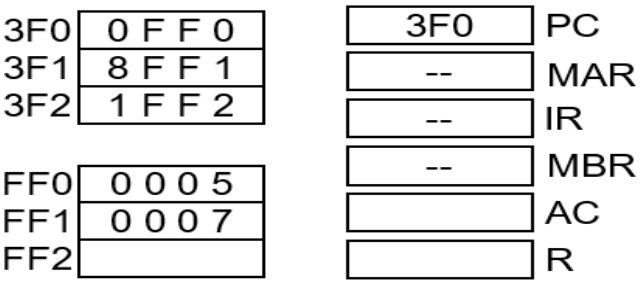
Q1: Answer the following questions. **[1+1+2+1 MARKS]**

A. Answer the Following Questions.

i. What is the size of Address bus and data bus, if the memory size is 32GB and each location stores one bit of information.

ii. A Processor has 24 bits data bus and 32 bits address bus calculate the amount of memory that can be addressed by the computer.

iii. We need to add two numbers that are in memory locations FF0 and FF1, and finally store the result in memory location FF2. We assume that 5 is present in FF0 and 7 is present in FF1. So, 5 and 7 have to be added and the result is stored in accumulator. The first instruction is stored in location 3F0**.**1st Instruction **LDA FF0 (**machine code of **LDA is 0)**: The contents in memory location FF0 are loaded into accumulator. After its execution, accumulator stores value 5.



Immediately after the fetch cycle of the 1stinstruction (**LDA FF0**), the values in MAR, IR and MBR.

iv. Consider a direct mapped with 4K main memory and cache with 32 lines and a block size of 8 bytes. To what line number(Cache) and block number(Main memory) does byte address 800 maps.

Q2 Answer the following Questions **[2.5 + 2.5 Marks]**

A. Consider a direct mapped cache with 8 cache blocks (0 – 7). A process accesses memory blocks in the following order: 2, 5, 15, 1, 8, 4, 0, 16, 19, 2, 13, 25, 18, 30, 24, 0, 67, 35, 5, 25.

i. What is the hit ratio if the system starts with a cold cache?

ii. Show the content of each block after the last reference.

B. Consider a Associative Mapped cache with 8 cache blocks (0 – 7). A process accesses memory blocks in the following order: 3, 6, 12, 17, 5, 13, 45, 3, 12, 24, 17, 20, 28, 45, 3, 27, 64, 6, 20, 12. If LRU is used as the cache replacement policy,

i. which cache block will memory block 12 reside?

ii. Find the number of Hits and also suggest how to improve the Hit ratio?

Q3. Answer the following questions. **[2 + 3 MARKS]**

A. A computer system has a main memory access time as 60ns. you as a computer organization expert has been asked to reduce the memory access time to 20ns by adding a suitable cache. Assume that the miss probability is 10%. What should be the fastness of cache (in terms of access time) for this requirement?

B. Consider the instruction ADD R1, X, which adds the contents of location X from the contents of register R1, and places the result in R1. Show the micro-operations used during fetch and execution phase of the instruction.

Q4 : Answer the following questions. **[5 MARKS]**

Consider the following program and assume that the Initial content of all the registers are zero

```
START: MOV R1, #2
       MOV R2, #1
       MOV R3, #2
       ADD  R1,R2
       SUB   R1,R3
       CMP  R1, R2
       JNZ   Next    (Jump if  Not Zero)
       MOV R3, #10
```

Next: print " EQUAL"

HLT

i. Write the timing of instruction pipeline with 5 stage (Neglect all types of hazard)
ii. What is the content of various registers after the execution of the program?
iii. Identify the type of Hazards with above program. and also step's to avoid the hazard.
iv. What is the minimum time taken to execute the program in pipelined and Non Pipelined Manner.
v. What is speedup, Efficiency and Throughput for the above program and also mention the ways to improve all three parameters.

Q5 : Answer the following questions. [3+2 MARKS]

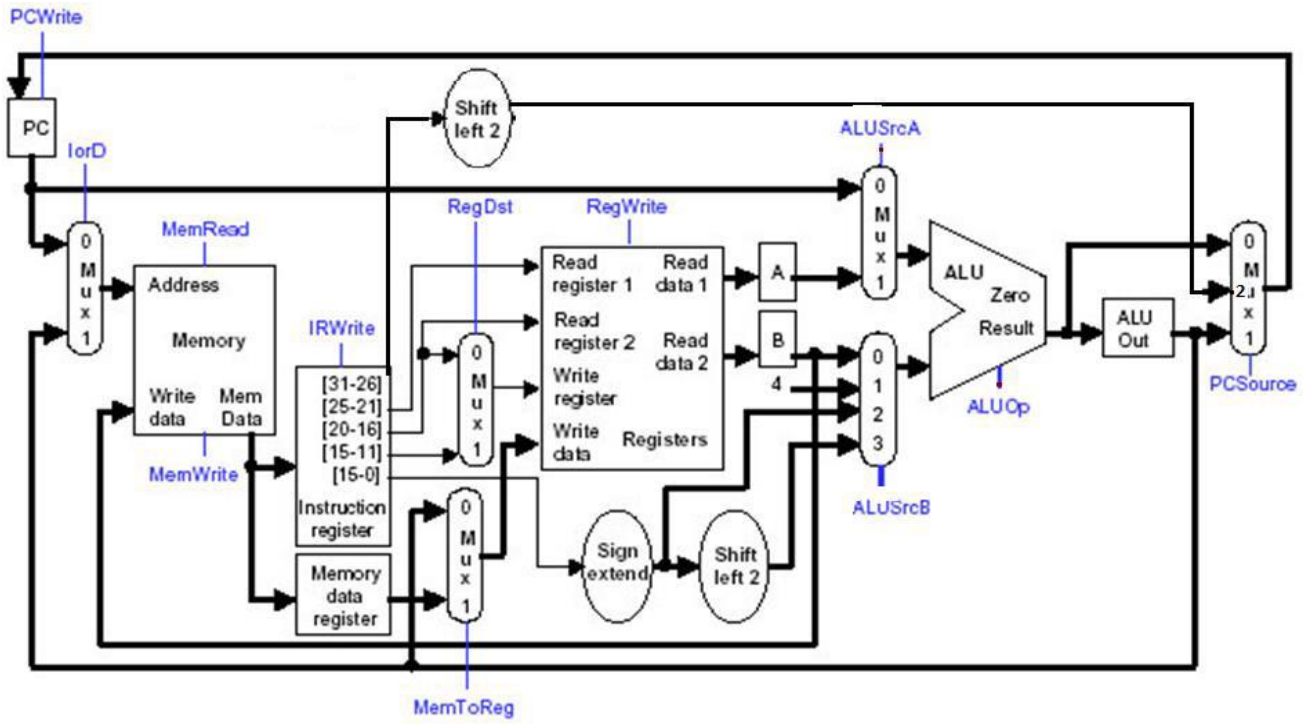
A. Check whether the statements are true or false. And also justify the same.(Solution without justification will not be considered for full marks)
i. DMA is best suitable for cache memory.
ii. In Direct Addressing Mode the operand is specified in the instruction.
iii. A bus consisting of 32 lines can transmit 32-bit unit of data sequentially.

B. Write a 0 addressing Instruction for the below equation.
A = ((100 – (20 + 50)) * 20

Q6: Answer the following questions. [5 MARKS]

Consider the structure of the multicycle data path implementation shown in figure. Answer the following questions with reference to instruction "lw $s0, 100[$s1]"

i. Fill in the following table indicating actions and the state of the control signals required for the steps listed to execute the instruction..



Note : Mention the Action and Control Signal required for each step as shown in the below table:

Step #	Action	Value of Control signals used
Step1		IorD = IRWrite = MemRead = ALUSrcA = ALUSrcB = ALUop = PCSource = PCwrite = MemToReg =
Step 2		IorD = IRWrite = MemRead = ALUSrcA = ALUSrcB = ALUop = PCSource = PCwrite = MemToReg =
Step 3		IorD = IRWrite = MemRead = ALUSrcA = ALUSrcB = ALUop = PCSource = PCwrite = MemToReg =
Step 4		IorD = IRWrite = MemRead = ALUSrcA = ALUSrcB = ALUop = PCSource = PCwrite = MemToReg =
Step 5		IorD = IRWrite = MemRead = ALUSrcA = ALUSrcB = ALUop = PCSource = PCwrite = MemToReg =