Birla Institute of Technology & Science, Pilani
Work Integrated Learning Programmes Division
Second Semester 2019-2020
M.Tech (Data Science and Engineering)
Mid-Semester Exam (EC-2 Makeup)

Course No.	: DSEIDZG516
Course Title	: Computer Organization and Software Systems
Nature of Exam	: Open Book
Weightage	: 30%
Duration	: 90 minutes
Date of Exam	: 05/07/2020 (FN), 10:00 am to 11:30 am

No. of Pages = 3
No. of Questions = 4

Note to Students:

1. **All parts of a question should be answered consecutively. Each answer should start from a fresh page.**
2. **Assumptions** made if any, should be stated clearly at the beginning of your answer.
3. For all problems **relevant steps** are to be shown.

Q1: Answer the following questions. **[7 MARKS]**

A. Games can be played in any device ranging from Xbox to mobiles. However, games must be conceptualized, designed and developed in computers with high end configurations. Desktops are powerful, but they do not give flexibility to game development companies. Game development companies are slowly shifting towards laptops as it encourages collaboration and agility. It also gives perfect work-life balance to their employees as they can continue their work from home with help of laptops. Due to this, there is a huge demand for laptops and their performance metrics. CPU manufacturing companies buy these performance metrics from "Mybenchmark" which is a benchmarking organization. "Mybenchmark" uses standard programs to assess the performance of CPUs.

Two new processors meant to be used in gaming laptops is designed with frequencies of 2 GHz and 1 GHz. These processors execute one instruction at a time. The table below gives instruction counts for the benchmark program - as well as number of cycles each instruction take, for the different classes of instructions.

Instruction Type`	Purpose	Processor 1 (2 GHz)		Processor 2 (1 GHz)	
		Instruction Count	Cycles	Instruction count	Cycles
Load & Store	Memory access instructions take higher number of cycles ; added to benchmark programs to simulate industry scenarios	3000	5	2000	2
Arithmetic Instructions	Floating point and integer arithmetic instructions are predominantly used in business transactions and programs	4000	3	6000	1
All others	These are instructions such as program control transfer	3000	4	2000	1

Benchmark comparisons looks at few critical parameters such as CPI, MIPS and cycle time. Calculate the following parameters for both processors:

i. What is the CPI for Processor1 and Processor2? [2]

Processor 1
(3000*5)+(4000*3)+(3000*4)=15000+12000+12000=39000 Cycles/10000 Instructions
therefore 3.9 CPI

Processor 2
(2000 *2) + (6000 * 1) + (2000 * 1) = 12000/ 1000 = **1.2 CPI**
1 marks each.

ii. What is the processor speed for Processor1 and Processor2 in millions of instructions per second (MIPS)? [2]

Processor 1 : MIPS = Clock rate/(CPI * 10^6)

The clock rate is 2GHz so **MIPS = (2 * 10^9)/(3.9 * 10^6) = 512.820**

Processor 2 : MIPS = Clock rate / (CPI * 10^6)

Clock rate is 1GHz, **MIPS = (1 X 10^9)/ *(1.2 X 10^6) = 833.33**

1 marks each.

iii. Which is the fastest processor among Processor1 and Processor2? Justify your answer. [1]
Processor 2 is faster as it a) it takes less cycles per instruction and more MIPS.
Performance of processor 1 in MIPS/ Performance of processor 2 in MIPS 512.82/833.33=0.615
Performance of Processor 1 is 0.615 times the performance of Processor 2 Hence, processor 2 is better.
1 marks

B. A disk track holds 60 Kbytes and its sector size is 2048 bytes. If it takes 2 ms to transfer a sector, what is the disk's rotational speed in rpm? [2]
Disk track =60Kbytes
Sector size=2048bytes
Sector transfer time=2ms
Disk rotational speed=?
Ans: Number of sectors in the disk = 60 x 1024 /2048 = 30 Sectors
Tavg = 2 ms = b/rN = 2048 * 60/RPM * 1/ (30*2048) = 1000 /1024

2 marks

Q2 . Answer the following questions. [8 MARKS]

A. A company named CacheFul is designing a machine with a byte addressable main memory. The size of the main memory is 2^{18} Bytes and block size is 16 Bytes. The machine employs a direct mapping cache consisting of 32 lines. This machine is specifically configured to run a classification algorithm.

i. When the algorithm is run it is noted that a memory access to main memory on a cache "miss" takes 30 ns and memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", how much time does it take to access memory on average? [1.5]

(0.8 × 3 ns) + (0.2 × (30+3) ns) = 2.4 ns + 6.6 ns
= 9 ns

ii. Recommended average memory access time for the algorithm to perform optimally is not more than 5 ns, what option as a **developer**, do you have to keep it near to 5ns? [1.5]
Re-Design the algorithm to increase the hit ratio to 93% or reduce the miss rate to 7%

B. Scientists at Indian Science Research Institute, wanted to check whether implementing cache replacement using two existing cache memory replacement algorithm LFU and FIFO would help reducing miss rate. The proposed new algorithm would work in two phases. The first 6 clocks (0-5) follow LFU and next 6 clocks (6-11) follow FIFO. The main memory block sequence is

0, 4, 0, 2, 1, 5, 0, 1, 2, 5, 0, 2

i. What is the Hit Ratio for the proposed new replacement algorithm? Justify your answer by filling in the following table. In LFU, in case of tie between cache lines for replacement, select the line which has been there for longer time in the cache. [4]

	LFU						FIFO					
Time	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Block #	**0**	**4**	**0**	**2**	**1**	**5**	**0**	**1**	**2**	**5**	**0**	**2**
L0	0_1	0_1	0_2	0_2	0_3	0_2	0_0	0_0	0_0	0_0	0_0	0_0
L1		4_1	4_1	4_1	4_1	5_1	5_5	5_5	5_5	5_5	5_5	5_5
L2				2_1	2_1	2_1	2_3	2_3	2_3	2_3	2_3	2_3
L3					1_1	1_1	1_4	1_4	1_4	1_4	1_4	1_4
Hit/Miss	M	M	H	M	M	M	H	H	H	H	H	H

7/12

Last line correct and hit ratio = 7/12 then ➔ 4marks ; if hit ratio is wrong deduct 0.5 marks.
Line 8 is correct ➔ 3 marks
Line 5 is correct ➔ 2 marks
Line 2 is correct ➔ 1 mark

ii. A hit ratio of 7/12 and 6/12 is achieved if LFU and FIFO replacement algorithms respectively are used. Scientists at Indian Science Research Institute would want you recommend appropriate replacement algorithm out of three schemes (LFU, FIFO and Proposed new scheme specified in part (i)) with proper justification. [1]

LFU is better compared to proposed new algorithm. If we use New algorithm, both counter and timing information needs to be maintained. Hence it becomes complex.
1 Marks

Q3. Answer the following Questions. **[8 Marks]**

A. Consider a reservation table for an instruction pipeline with four stages: where IF- Instruction Fetch, ID - Instruction decode and operand fetch, EX- Execute and WR - write operand.

	0	1	2	3
IF	X			
ID		X		
EX			X	
WR				X

i. Draw time space diagram showing 3 instruction execution (I1, I2 and I3). [1]

	0	1	2	3	4	5
IF	I1	I2	I3			
ID		I1	I2	I3		
EX			I1	I2	I3	

WR				I1	I2	I3

1 Marks if everything is correct

ii. Calculate speed up and efficiency for 100 instruction execution. [2]

Speedup = nk / k + (n-1)

= 100 x 4 / (4 + 99)

= 400/ 103 = 3.883

Efficiency = n / k + (n-1)

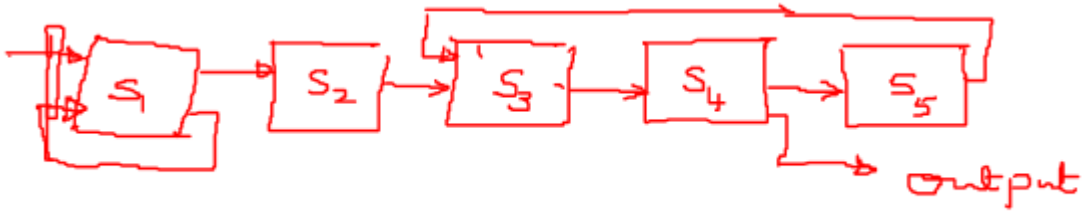
= 100/103

= 0.9708

1 Marks each

B. Consider a reservation Table for a pipeline with 5 stages and inter-stage buffers. It takes 8 clock cycles to execute a task. Draw the pipeline structure and identify the category to which this pipeline belongs to. [2]

	0	1	2	3	4	5	6	7
S1	X	X						
S2			X					
S3				X			X	
S4					X			X
S5						X		



1.5 Marks for diagram and 0.5 marks for category

If output taken is wrong - 0.5

First loop is missing - 0.5

Second loop is missing -0.5

C. Indicate whether the following statements are **True** or **False** with proper justification. Writing only True or False **without proper justification will not be awarded any marks**. [3]

i. In case of direct mapped cache, LFU replacement is preferred compared to LRU and FIFO.
False. Direct mapped cache has specific place for each block. Hence, no replacement algorithms are needed in direct mapped cache

ii. The time that is required for tag comparison in case of direct mapped cache more compared to associative and set associative cache memory.
False : time that is required for tag comparison in case of direct mapped cache less compared to associative and set associative cache memory because once the line is identified, then that

line's tag is compared with the tag of address. Whereas in case of associative and set associative cache memory, more tags are compared.

iii. The level 1 cache is of DRAM type and the level 2 cache is of SRAM type.
False : Both the tags are SRAM types as it gives faster performance.

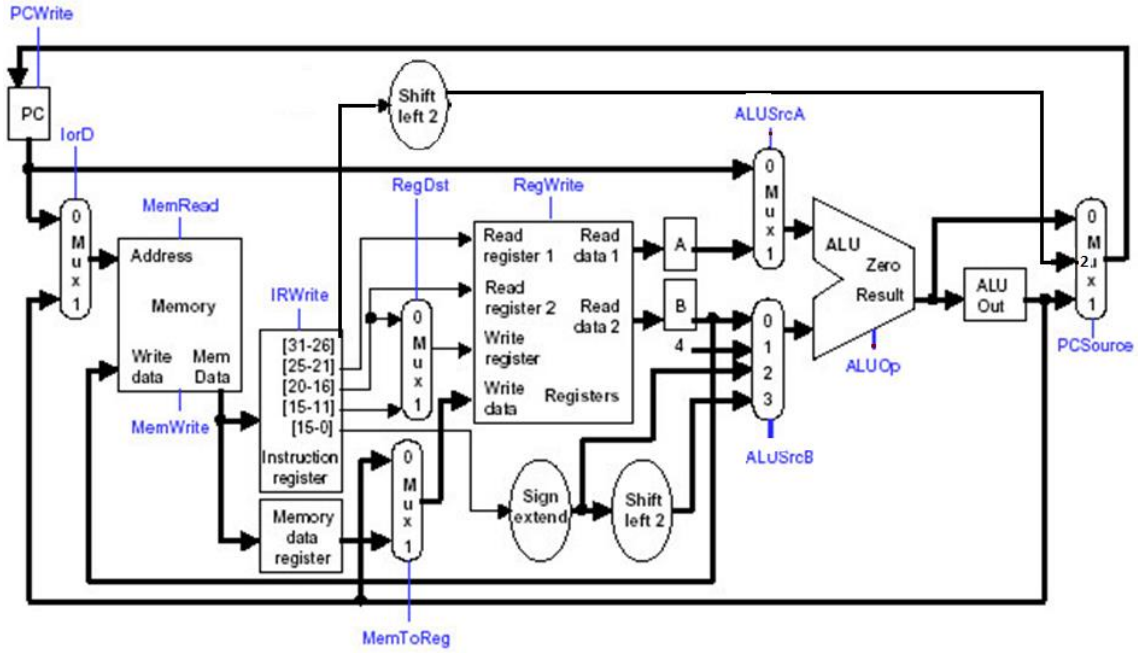
One Marks each. No marks will be awarded if just True or false is written

Q4: Answer the following questions. **[7 Marks]**

Consider the structure of the multicycle datapath implementation shown in figure. Answer the following questions with reference to instruction "beq $s0, $s1, 100H"

i. Fill in the following table indicating actions and the state of the control signals required for the steps listed to execute the instruction. [5]

ii. What will be the contents of PC after the execution of the instruction? [2]



Step #	Action	Value of Control signals used
Step 3	Branch Completion: if (A == B) PC ← ALUout	IorD = X IRWrite = X MemRead = X ALUSrcA = 1 ALUSrcB = 00 ALUop = 01 PCSource = 01 PCwrite = 1 MemToReg = X
Step 4	This step is not needed	IorD = IRWrite = MemRead = ALUSrcA = ALUSrcB = ALUop = PCSource = PCwrite = MemToReg =

If S0 = S1, then PC ← PC + 4 + 100 * 4 = PC + 404
If S0 != S1 then PC ← PC + 4

For Part (i) 0.5 marks each for step 3 and 0.5 marks for step 4
For Part (ii) 1 marks for each