Birla Institute of Technology & Science, Pilani

Work Integrated Learning Programmes Division

First Semester 2020-2021

M.Tech (Data Science and Engineering)

Mid-Semester Exam (EC-3 Regular)

Course No. : DSECLZG516
Course Title : Computer Organization and Software Systems
Nature of Exam : Open Book
Weightage : 30%
Duration : 90 minutes
Date of Exam : 11/07/2021 FN (10:00 AM to 12:00 PM)

Number of Pages: 04

Number of Questions: 04

Note to Students:

1. **All parts of a question should be answered consecutively. Each answer should start from a fresh page.**
2. **Assumptions** made if any, should be stated clearly at the beginning of your answer.
3. For all problems **relevant steps** are to be shown.

Q1: Answer the following questions. **[5 + 3 MARKS]**

A. In 1990, Simplex Company came up with a simple processor with a clock rate of 4.5GHz and average CPI of 6. Later, they decided to upgrade the system by replacing simple processor with 5 stage pipelined processor. Due to internal pipeline delay, the processor clock is reduced to 2.5GHz. Assume that the new system does not implement any techniques to avoid hazards. Find out the following:

i) Clock time in non-pipeline Processor

ii) Execution Time of non-pipeline Processor

iii) Clock time in pipeline Processor

iv) Execution Time of pipeline Processor for 100 tasks

v) Speed up achieved in pipeline processor.

B. A Netcom systems developed two computer systems C1 and C2. where C1 has machine instructions for floating point (FP) operations as part of its processor ISA and C2 does NOT have floating point instructions as part of its processor ISA. Since C2 does not have floating point instructions, all floating point instructions will be implemented in Software level with non-FP instructions. You can assume that both systems are operating at a clock speed of 300 Mhz. We are trying to run the SAME program in both the systems which has the following proportion of commands:

Instruction type	% instructions in Program	Instruction Duration (Number of clock periods CPI)	
		C1	C2
Addition of FP numbers	16%	6	20
Multiplication of FP numbers	10%	8	32
Division of FP numbers	8%	10	66
Misc. Instructions (non-FP)	66%	3	3

Answer the following :

a. Find the MIPS for both C1 and C2.

b. Assume that there are 9000 instructions in the program that is getting executed on C1 and C2. What will be the CPU program execution time on each system C1 and C2 ?

c. For the two systems to have the fastest speed and at the same time have equal speed, what would be the possible mixture of the instructions that would be required in the program? WHY?

Q2: Answer the following questions. **[2+ 1 + 4 MARKS]**

A. A SanDisk designed a cache system of two-level, with level 1and level 2 with cache access times 2 and 16 clock cycles respectively. The miss penalty from level 2 cache to main memory is 36 clock cycles. The miss rate of the level1 cache is 3 times of the level 2 cache. The average memory access time of the cache system is 4 cycles. Calculate the miss rate for both L1 and L2 Cache.

B. Indicate whether the following statements are **True** or **False** with proper justification. Writing only True or False **without proper justification will not be awarded any marks**.

i. In case of arithmetic left shift MSB bit is replaced with Zero.

ii. The hard wired design is flexible to design and add new instructions..

C. The configuration of a byte addressable computer is given as 16-bit memory addresses,4K-byte cache which is direct-mapped, each line is of 32 bytes and a clock of 1GHz .

i. Find Tag, Block, and Word. in bits.

ii. Find the total number of bits in the cache.

iii. CPU issues the following addresses 125,126,127,0,127,126,125 all decimal . Compute the number of misses.?

iv. If the Cache access takes 3 cycles and main memory access takes 19 cycles, and for a particular code the miss time is 5%. what is the Average Memory Access Time?

Q3: Answer the following questions. **[2+1+3+2 MARKS]**

A. Consider a BEST developers who is well known for developing computer systems developed a 16 bit computer with an address bus of 24 bits. Answer the following :

i. How many address locations can be accessed in Bytes?

ii. If using Memory mapped I/O totally how many memory and I/O Locations can be accessed?

iii. If using I/O mapped I/O totally how many memory and I/O Locations can be accessed?

iv. How many more bits are need to be added to access 32 Giga Memory locations?

B. Which type of hazard results in Von-Neumann bottleneck? Is there a solution to overcome this problem?

C. A Data Analytic Server need to be designed with two options given below

Option1: A Business intelligence Module having a speedup of 2.5 which process 60% of calculations

Option2: A Statistical module with a speedup of 1.5 which process 40% of calculations.

Which option is better to design and justify your answer?

D. Find the Locality of Reference for the below statement.

i. A program with stride-1 reference pattern.

ii. Loops are good with respect to Instruction Fetches.

Q4: Answer the following questions. **[1+1+2+3 MARKS]**

The single cycle implementation of MIPS is as shown below. Answer the following questions with reference to "sw $S5,200($S6)" instruction. Assume that the contents of the registers S2 = 0FEEAA00H, and PC = 1E, pointing to the instruction under consideration.(Consider 200 as Hexa Value)

i. What is the addressing mode of the instruction and also mention the updated PC Value?

ii. Which part of the instruction format, address of S1 and S2 are stored?

iii. What is the Effective address generated by the instruction ?

iv. Fill the status of different control signal to execute the instruction. Answer should be present in the form of table given below . Indicate Don't care as 'X'.

Signal	Status
RegDst	
Branch	
MemtoReg	
ALUOP	
ALUSrc	
RegWrite