PRATEEK GUPTA

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EDUCATION

NATIONAL INSTITUTE OF TECHNOLOGY ARUNACHAL PRADESH **08 2023 – 08 2027**
Bachelor Of Technology- Electronics and Communication Engineering- CGPA- ***8.70*** *Arunachal Pradesh, India*

Tathagat Gyansthli Senior Secondary School **07 2021 – 08 2022**
12th - PCMC - ***87%*** *Atarra, Banda*

COURSEWORK / SKILL

- Verilog Hdl
- OOPS Concept
- Data Structures & Algorithms
- Semiconductor Devices
- Digital Electronics
- Analog Circuits
- Communication

PROJECTS

ARITHMETIC AND LOGICAL UNIT | Verilog HDL **12 2024**

- **About Project**
  - **1. Operation Selection**: User can choose from various option like Addition, Substraction, Multiplication, Division, Equality checker, Inequality checker with the help of operator input.
  - **2. Input Insertion**: There are two operands each of 8 bits, User can enter data as per instructions mention in ALU Testbence (instructions may vary for different operation).
  - **3. Output Generation**: Two Answer output each of 8 bits, output will be shown as per operations.
  - **4. Simulation**: Output simulation waveform will show all types of input, output, other wires and registers.

TRAFFIC LIGHT CONTROLLER | Verilog HDL (Finite State Machine) **01 2025**

- **About Project**
  - **1. Working**: The traffic signal operates between Main Road and County Road (with priority given to Main Road). When the sensor detects a vehicle on County Road, the signal will transition. After a certain period, the signal will return to its previous state.
  - **2. Input Sensor**: The sensor will send input to the circuit by setting its input value to high.
  - **3. Taffic Light Transition**: Upon getting input, the transition of the main road signal will go from green to yellow to red, while the county road signal changes from red to green.

SEQUENCE DETECTOR | Verilog HDL (Finite State Machine) **02 2025**

- **About Project**
  - **1. Properties**: It can detects all forms of 3-bit number without getting stuck in overlapping issues.
  - **2. Input Sequence**: User can give any set of pattern or array.
  - **3. Output Detection**: Specified output signal will set to high for some time after getting sequence.

TECHNICAL KNOWLEDGE

Languages: Verilog, C/C++, Python, Java,
Developer Skills: Circuit Simulation, Waveform Analysis
Developer Tools: Xilinx Vivado, Modelsim, Icarus Verilog, Gtkwave, Ltspice, VS Code, Pycharm
Technologies/Frameworks: GitHub

CERTIFICATIONS/COURSES

- **ATF (AlgoUniversity) 2024:** Stage 2 Candidate
- **CeNSE Winter School on semiconductor Technology**: Certificate of Completion