

# Tugas Praktikum SKJ

## Ke -3

Nama : Bagus Cipta Pratama

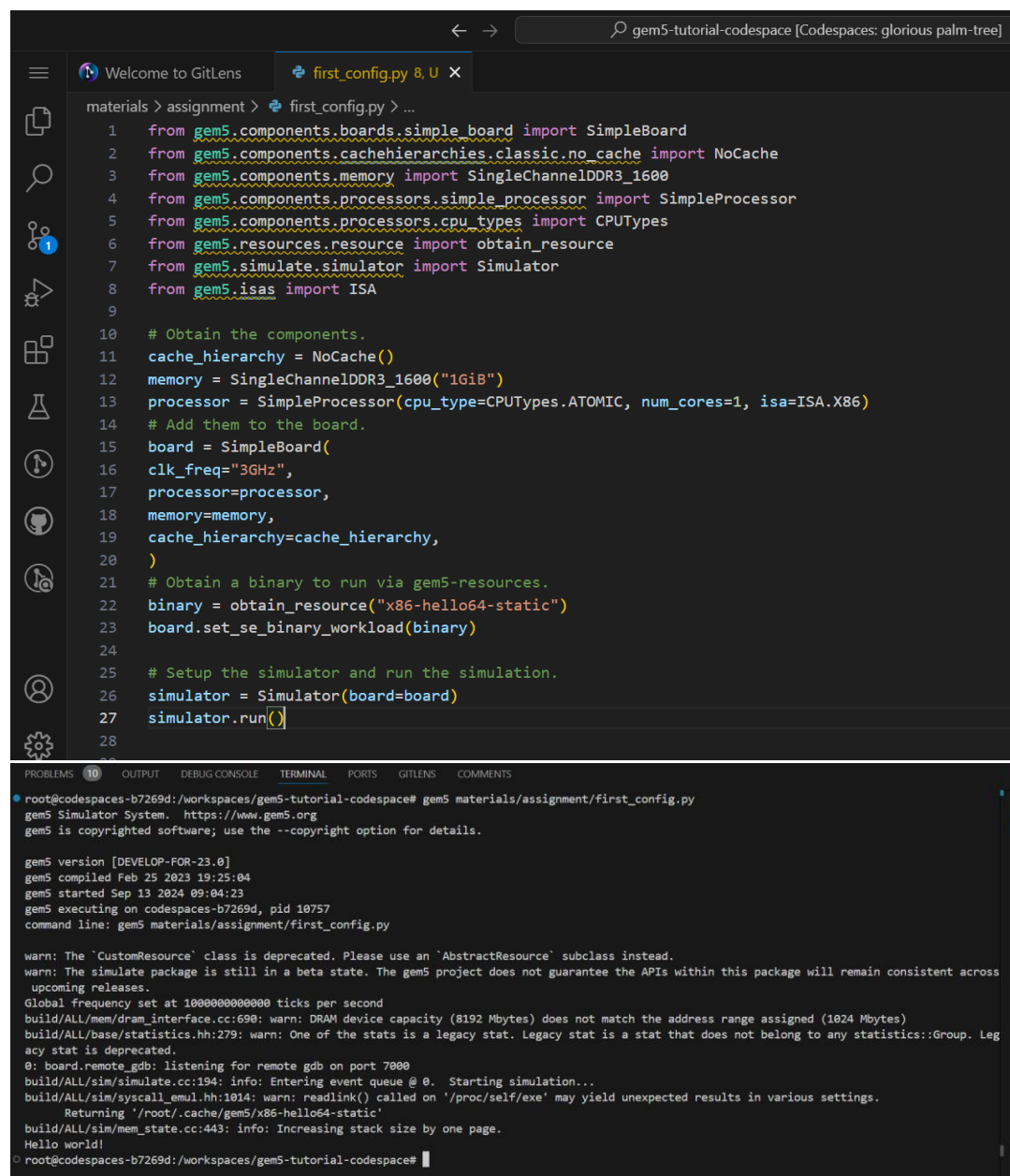
NIM : 23/516539/PA/22097

Kelas : KOMC

## A. First Assignment : Hello World! (30 poin)

Dalam assignment pertama, kita akan membuat sebuah simulasi "hello world" minimal menggunakan gem5. Kita akan membuat file konfigurasi `first_config.py` yang mencakup impor komponen-komponen penting dari gem5, definisi komponen sistem komputer seperti prosesor, memori, dan cache, serta menghubungkan komponen-komponen tersebut ke board. Selanjutnya, kita akan menambahkan binary "hello world" untuk dijalankan pada simulasi. Akhirnya, kita akan mengkonfigurasi dan menjalankan simulasi. Tujuan utama dari assignment ini adalah memperkenalkan kita pada dasar-dasar konfigurasi dan simulasi menggunakan gem5, memberikan kita pengalaman praktis dalam menyiapkan simulasi sederhana.

Berikut adalah bukti screenshotnya ,



```
gem5-tutorial-codespace [Codespaces: glorious palm-tree]

Welcome to GitLens
first_config.py 8, U X

materials > assignment > first_config.py > ...
1 from gem5.components.boards.simple_board import SimpleBoard
2 from gem5.components.cachehierarchies.classic.no_cache import NoCache
3 from gem5.components.memory import SingleChannelDDR3_1600
4 from gem5.components.processors.simple_processor import SimpleProcessor
5 from gem5.components.processors.cpu_types import CPUTypes
6 from gem5.resources.resource import obtain_resource
7 from gem5.simulate.simulator import Simulator
8 from gem5.isas import ISA
9
10 # Obtain the components.
11 cache_hierarchy = NoCache()
12 memory = SingleChannelDDR3_1600("1GiB")
13 processor = SimpleProcessor(cpu_type=CPUTypes.ATOMIC, num_cores=1, isa=ISA.X86)
14 # Add them to the board.
15 board = SimpleBoard(
16     clk_freq="3GHz",
17     processor=processor,
18     memory=memory,
19     cache_hierarchy=cache_hierarchy,
20 )
21 # Obtain a binary to run via gem5-resources.
22 binary = obtain_resource("x86-hello64-static")
23 board.set_se_binary_workload(binary)
24
25 # Setup the simulator and run the simulation.
26 simulator = Simulator(board=board)
27 simulator.run()
28

root@codespaces-b7269d:/workspaces/gem5-tutorial-codespace# gem5 materials/assignment/first_config.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

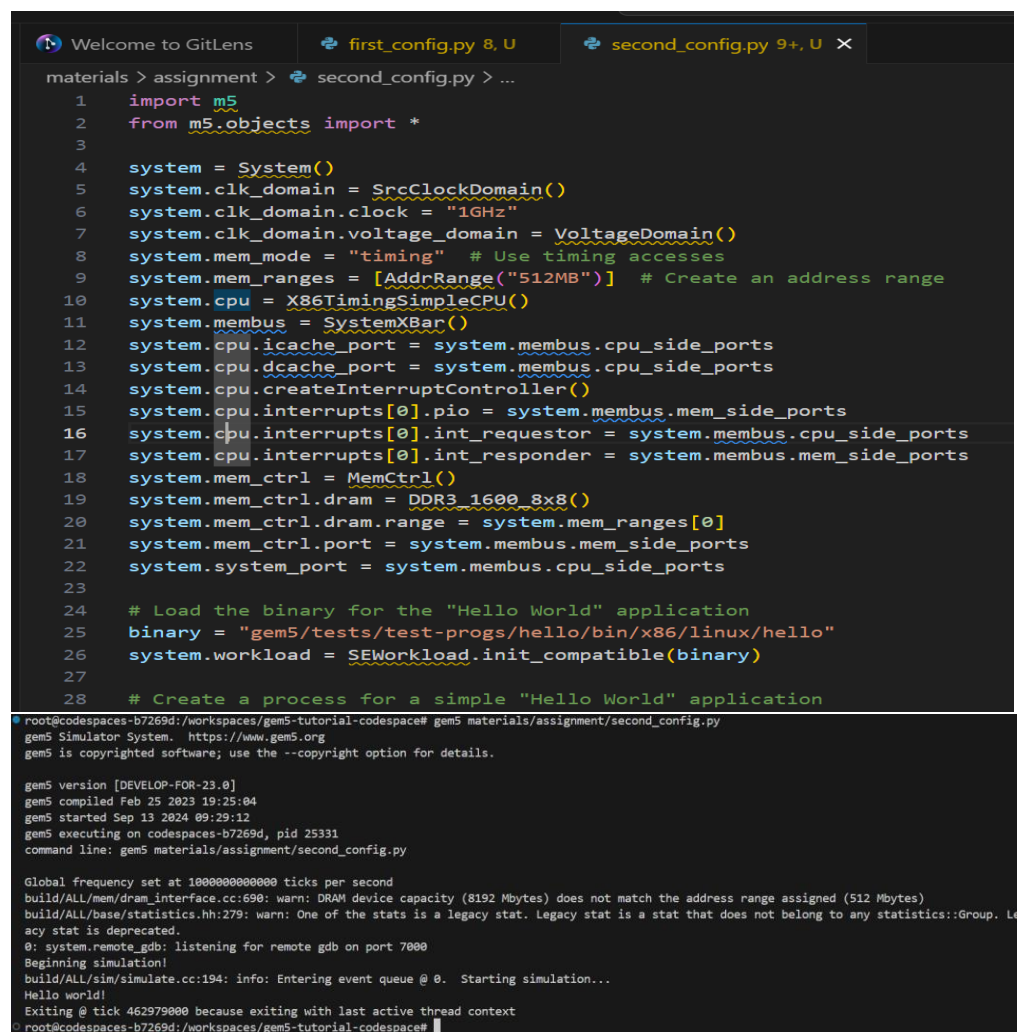
gem5 version [DEVELOP-FOR-23.0]
gem5 compiled Feb 25 2023 19:25:04
gem5 started Sep 13 2024 09:04:23
gem5 executing on codespaces-b7269d, pid 10757
command line: gem5 materials/assignment/first_config.py

warn: The 'CustomResource' class is deprecated. Please use an 'AbstractResource' subclass instead.
warn: The simulate package is still in a beta state. The gem5 project does not guarantee the APIs within this package will remain consistent across upcoming releases.
Global frequency set at 100000000000 ticks per second
build/ALL/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (1024 Mbytes)
build/ALL/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
0: board.remote_gdb: listening for remote gdb on port 7000
build/ALL/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
build/ALL/sim/syscall_emul.hh:1014: warn: readlink() called on '/proc/self/exe' may yield unexpected results in various settings.
Returning '/root/.cache/gem5/x86-hello64-static'
build/ALL/sim/mem_state.cc:443: info: Increasing stack size by one page.
Hello world!
root@codespaces-b7269d:/workspaces/gem5-tutorial-codespace#
```

## B. Second Assignment : Simulasi Sistem Komputer Sederhana (30 poin)

Assignment kedua mengajak kita untuk membuat simulasi sistem komputer yang lebih kompleks. Kita akan membuat file `second_config.py` untuk mensimulasikan sistem yang terdiri dari CPU, memory bus, dan memory controller. Proses ini melibatkan impor library `m5` dan `SimObjects` yang diperlukan, pembuatan dan konfigurasi objek `System` termasuk clock domain dan memory range, serta pembuatan dan penghubungan CPU, memory bus, dan memory controller. Kita juga akan mengatur proses yang akan dijalankan oleh CPU, dalam hal ini program "Hello world". Akhirnya, kita akan menginisialisasi dan menjalankan simulasi. Assignment ini bertujuan untuk memberikan pemahaman yang lebih mendalam tentang konfigurasi komponen-komponen sistem dalam `gem5` dan bagaimana komponen-komponen tersebut berinteraksi.

Berikut adalah bukti screenshotnya ,



```
Welcome to GitLens  first_config.py 8, U  second_config.py 9+, U X
materials > assignment > second_config.py > ...
1  import m5
2  from m5.objects import *
3
4  system = System()
5  system.clk_domain = SrcClockDomain()
6  system.clk_domain.clock = "1GHz"
7  system.clk_domain.voltage_domain = VoltageDomain()
8  system.mem_mode = "timing" # Use timing accesses
9  system.mem_ranges = [AddrRange("512MB")] # Create an address range
10 system.cpu = X86TimingSimpleCPU()
11 system.membus = SystemXBar()
12 system.cpu.icache_port = system.membus.cpu_side_ports
13 system.cpu.dcache_port = system.membus.cpu_side_ports
14 system.cpu.createInterruptController()
15 system.cpu.interrupts[0].pio = system.membus.mem_side_ports
16 system.cpu.interrupts[0].int_requestor = system.membus.cpu_side_ports
17 system.cpu.interrupts[0].int_responder = system.membus.mem_side_ports
18 system.mem_ctrl = MemCtrl()
19 system.mem_ctrl.dram = DDR3_1600_8x8()
20 system.mem_ctrl.dram.range = system.mem_ranges[0]
21 system.mem_ctrl.port = system.membus.mem_side_ports
22 system.system_port = system.membus.cpu_side_ports
23
24 # Load the binary for the "Hello World" application
25 binary = "gem5/tests/test-progs/hello/bin/x86/linux/hello"
26 system.workload = SEWorkload.init_compatible(binary)
27
28 # Create a process for a simple "Hello World" application

root@codespaces-b7269d:/workspaces/gem5-tutorial-codespace# gem5 materials/assignment/second_config.py
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version [DEVELOP-FOR-23.0]
gem5 compiled Feb 25 2023 19:25:04
gem5 started Sep 13 2024 09:29:12
gem5 executing on codespaces-b7269d, pid 25331
command line: gem5 materials/assignment/second_config.py

Global frequency set at 100000000000 ticks per second
build/ALL/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
build/ALL/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Le
acy stat is deprecated.
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/ALL/sim/simulate.cc:194: info: Entering event queue @ 0.  Starting simulation...
Hello world!
Exiting @ tick 462979000 because exiting with last active thread context
root@codespaces-b7269d:/workspaces/gem5-tutorial-codespace#
```

### C. Third Assignment : Menambahkan Cache (30 poin)

Dalam assignment ketiga, kita diminta untuk memperluas konfigurasi dari assignment kedua dengan menambahkan hierarki cache. Kita akan menambahkan cache L1 dan L2 ke sistem, mengkonfigurasi parameter cache seperti ukuran, associativity, dan ukuran blok. Kita juga perlu memperbarui koneksi antara cache, CPU, dan memory bus untuk memastikan integrasi yang benar. Setelah konfigurasi selesai, kita akan menjalankan simulasi untuk memverifikasi bahwa cache telah terintegrasi dengan benar. Tujuan dari assignment ini adalah memberikan kita pengalaman praktis dalam mengkonfigurasi cache pada simulator gem5 dan memahami bagaimana penambahan cache dapat mempengaruhi kinerja sistem. Ini merupakan langkah penting dalam memahami arsitektur komputer modern dan peran cache dalam meningkatkan kinerja sistem.

Berikut adalah bukti screenshotnya ,

```
materials > assignment > third_config.py > ...
1  import m5
2  from m5.objects import *
3  from cache import L1ICache, L1DCache, L2Cache
4
5  system = System()
6  system.clk_domain = SrcClockDomain()
7  system.clk_domain.clock = "1GHz"
8  system.clk_domain.voltage_domain = VoltageDomain()
9  system.mem_mode = "timing"
10 system.mem_ranges = [AddrRange("512MB")]
11 system.cpu = X86TimingSimpleCPU()
12 system.membus = SystemXBar()
13
14 system.cpu.icache = L1ICache()
15 system.cpu.dcache = L1DCache()
16
17 system.cpu.icache.connectCPU(system.cpu)
18 system.cpu.dcache.connectCPU(system.cpu)
19
20 system.l2bus = L2XBar()
21
22 system.cpu.icache.connectBus(system.l2bus)
23 system.cpu.dcache.connectBus(system.l2bus)
24
25 system.l2cache = L2Cache()
26 system.l2cache.connectCPUSideBus(system.l2bus)
27 system.membus = SystemXBar()
28 system.l2cache.connectMemSideBus(system.membus)
```

```

34  import m5
35  from m5.objects import Cache
36
37  # Add the common scripts to our path
38  m5.util.addToPath("../..")
39
40  # Some specific options for caches
41  # For all options see src/mem/cache/BaseCache.py
42
43
44  class L1Cache(Cache):
45      """Simple L1 Cache with default values"""
46
47      assoc = 2
48      tag_latency = 2
49      data_latency = 2
50      response_latency = 2
51      mshrs = 4
52      tgts_per_mshr = 20
53
54      def _init_(self, options=None):
55          super()._init_()
56          pass
57
58      def connectBus(self, bus):
59          """Connect this cache to a memory-side bus"""
60          self.mem_side = bus.cpu_side_ports
61

```

PROBLEMS 38 OUTPUT DEBUG CONSOLE TERMINAL PORTS GITLENS COMMENTS

```

root@codespaces-b7269d:/workspaces/gem5-tutorial-codespace# gem5 materials/assignment/third_config.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version [DEVELOP-FOR-23.0]
gem5 compiled Feb 25 2023 19:25:04
gem5 started Sep 13 2024 20:48:37
gem5 executing on codespaces-b7269d, pid 3548
command line: gem5 materials/assignment/third_config.py

Global frequency set at 1000000000000 ticks per second
build/ALL/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match
build/ALL/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is deprecated.
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/ALL/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
Hello world!
Exiting @ tick 56435000 because exiting with last active thread context
root@codespaces-b7269d:/workspaces/gem5-tutorial-codespace#

```

#### **D. Link Repository GitHub :**

berikut adalah link repository github yang memuat semua kode diatas :

<https://github.com/mobssspro/Bagus-Cipta-Pratama-SKJ-Lab.git>