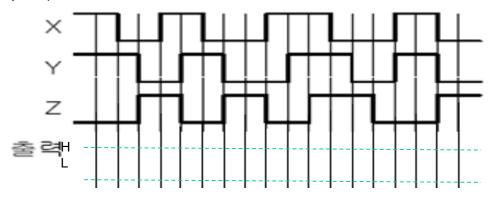
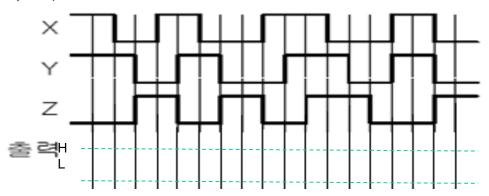
[실습] Chapter 1.5~1.6 :: 연습문제

1. [기본게이트] <mark>3입력 NAND</mark> 게이트의 심벌, 부울식, 진리표, 출력파형을 작성하시오. (관련연습문제 p49 - 71, 72)



2. [기본게이트] <mark>3입력 XOR</mark> 게이트의 심벌, 부울식, 진리표, 출력파형을 작성하시오. (관련연습문제 p49 - 71, 72)



[실습] Chapter 1.5~1.6 :: 연습문제

3. 여러 개의 스위치를 가진 회로에서 어느 한 스위치만 닫았더니, 램프가 켜졌다. 이것은 어떤 유형의 스위치 회로인가?

4. 여러 개의 스위치를 가진 회로에서 한 개 이외의 모든 스위치들을 닫았으나 램프는 켜지지 않았다. 이것은 어떤 유형의 스위치 회로인가?

[실습] Chapter 1.5~1.6 :: 연습문제

5. DDCA2e_Ch1_0에서1까지_ex: p49 연습문제 73 진리표 작성:

문제 1.73 다수결 게이트(majority gate)는 입력의 과반 수 이상이 TRUE일 때만 출력이 TRUE가 된 다. 그림 1.41에 보인 다수결 게이트의 진리 그림 1.41 3-입력 다수결 게이트 표를 완성하라

6. DDCA2e_Ch1_0에서1까지_ex: p49 연습문제 75 진리표 와 논리식 작성:

문제 1.75 그림 1.43에 보인 3-입력 OR-AND-INVERT(AOI) 게이트는 C가 TRUE이고 A 또는 B가 TRUE일 때 출력이 FALSE가 된다. 이외의 다른 경우는 TRUE를 출력한다. 이 게이트에 대한 진리표를 완성하라.

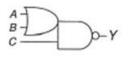


그림 1.43 3-입력 OR-AND INVERT 게이트

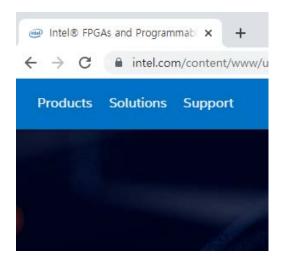
[실습] 응용문제

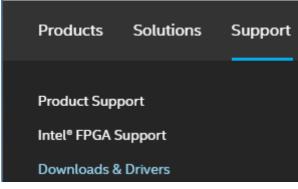
7. [응용문제] 어떤 의사결정 회의에서 각 위원들은 안건에 대한 의견을 표명하기위한 스위치를 한 개씩 가지고 있다. 각 위원은 안건에 찬성하면 스위치를 누르고, 반대한다면 스위치를 누르지 않는다. 두 위원(A,B)의 의견이 같은 경우에 한해 C 위원의 찬성이 있을 경우 출력(F)을 '1'로 발생하는 회로를 구성하시오. 스위치는 누르면 '1'을 발생하고, 누르지 않으면 '0'을 발생한다.

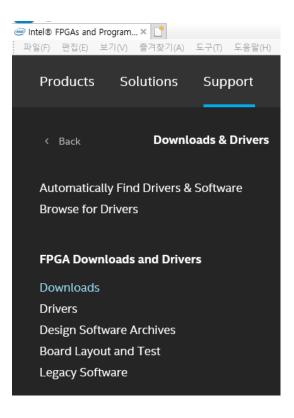
8. 위 [응용문제]를 다음페이지에서 설명하는 쿼터스를 이용하여 구현하고 시뮬레이션 결과가 예상한 진리표와 일치하는지 확인하시오.

0. Altera Quartus 다운로드 설치

- http://www.altera.com
- support download Quartus II Web Edition



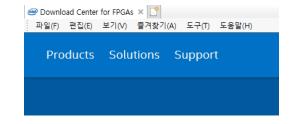




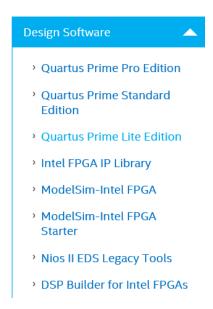


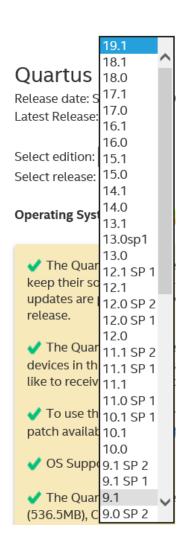
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Quartus II Web Edition	Platform	File Name	Size
Quartus II Web Edition	Windows	91_quartus_free.exe	1.4 GB

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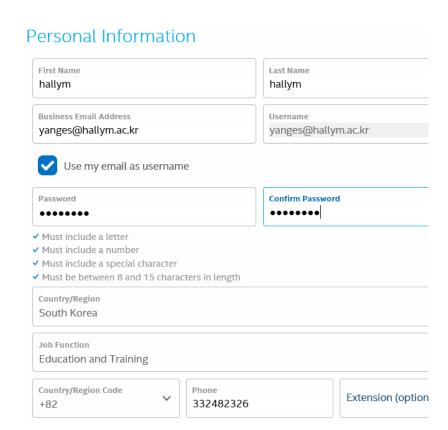
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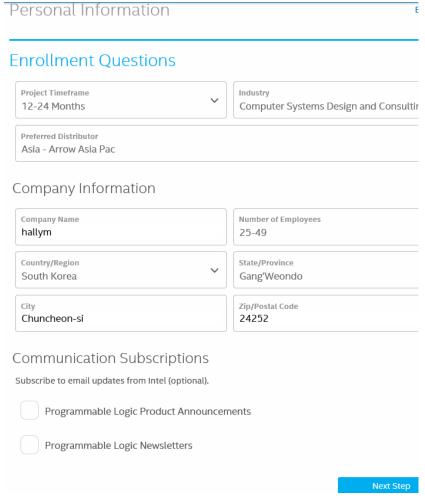
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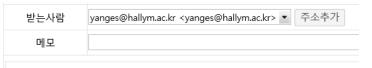


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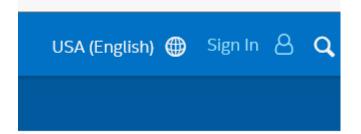
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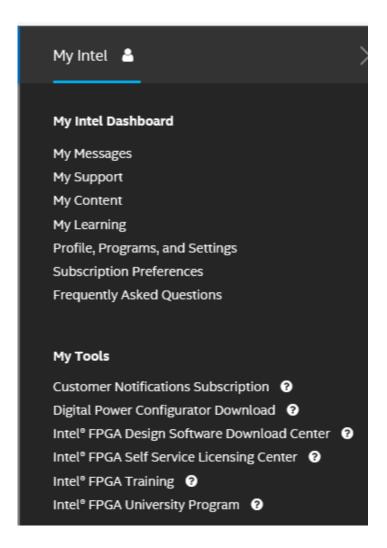
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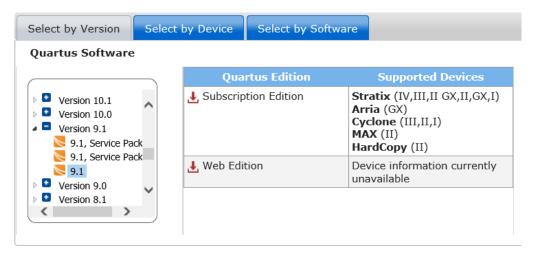


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Quartus II Web Edition	Platform	File Name	Size
Quartus II Web Edition	Windows	91_quartus_free.exe	1.4 GB
Quartus II Web Edition	Linux	91_quartus_free_linux.tar	1.7 GB

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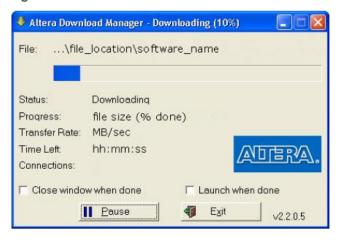
Quartus II Web Edition Software Version

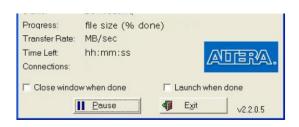
Next Steps

- Get licenses
- › Get licensing and installation support

If the Altera Download Manager window, as shown in figure 1, troubleshooting steps below.

Figure 1. Altera download window





Download Troubleshooting Steps

- 1. Disable your pop-up blocker
 - If a yellow pop-up blocker bar appears just below your Internet Explorer menu bar (see Fi the yellow bar and select "Temporarily Allow Pop-ups." Any third-party pop-up blockers I disabled to download a file.

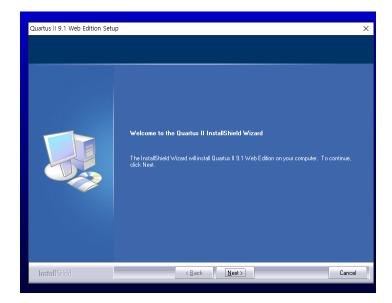
Figure 2. Windows Explorer Pop-Up Blocker

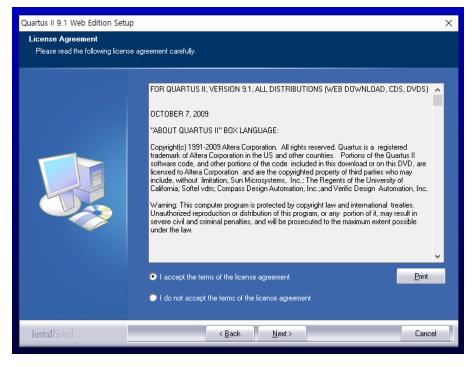


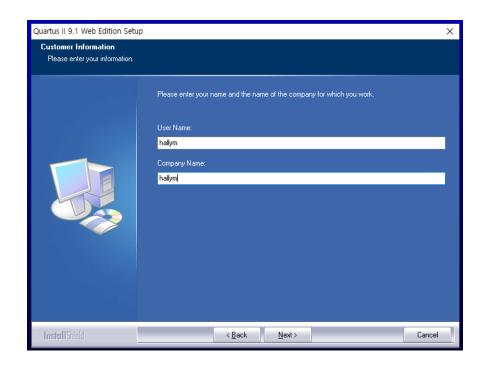
- You may also by-pass the pop-up blocker by following this link: Download your file now.
- 2. The Altera Download Manager, as shown in figure 1, will appear. Click "Run" to initiate the do

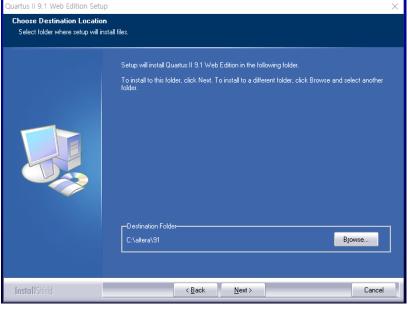
My Intel Account Help

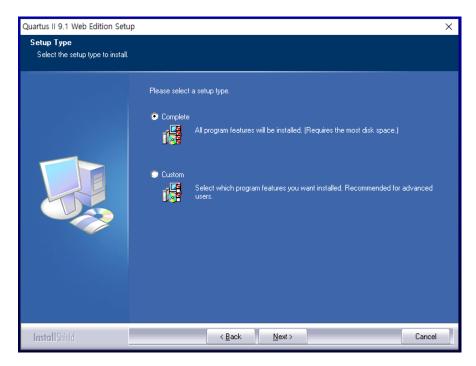
91_quartus_free.exe(1.42GB) 글(물) 실행하거나 저장하시겠습니까? 실행(R) 저장(S) ▼ 취소(C)

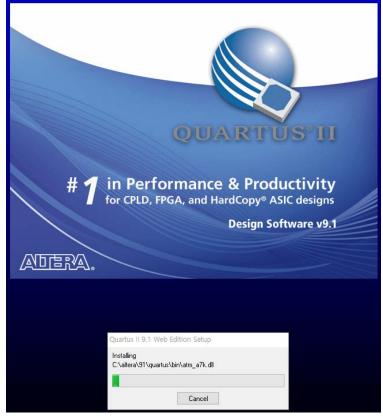




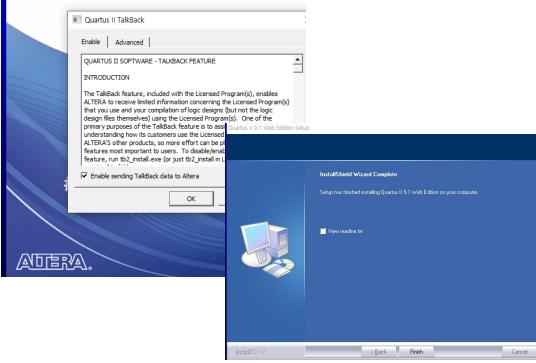




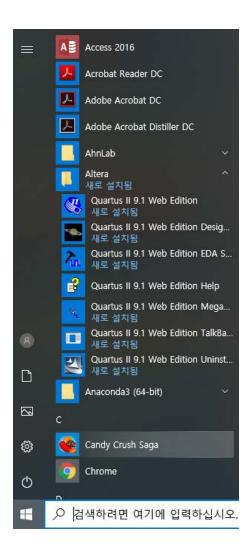


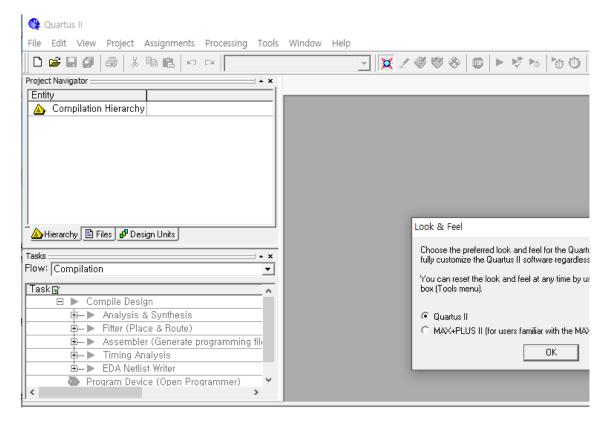






[실습] Quartus 소프트웨어 실행





[실습] New Project Wizard

1. Project 만들기

<주의사항> 프로젝트 이름에 한글이 들어가면 안됨.

- File -> New Project Wizard -> next -> 프로젝트 폴더이름
- 프로젝트 이름을 줄 때는 모듈 명과 같게 해야 한다.
- Family Device 셋팅: Family를 사이클론 2 로 설정(또는 Stratix II)
- available : ep2c35f672C8 -> next -> next -> finish

2. 블럭 다이어그램 설계

- File 메뉴 -> new -> Block Diagram/Schematic File -> 설계에 들어간다

3. 컴파일

- Processing 메뉴 -> Start compilation

[실습] Vector Waveform

4. Vector Waveform

- File 메뉴 -> new -> Vector Waveform
- vwf 파일이름을 프로젝트 이름과 동일하게 변경하여 저장
- -> Name/Value 부분 더블클릭 -> Node Finder -> Filter(Pins all) -
- > List -> Input과 Output 핀 선택 -> OK
- -> 컨트롤 하려는 핀을 선택 -> Overwrite Clock을 선택하고 input 값들의 Period을 조정

[실습] Vector Waveform

5. simulation

- processing 메뉴 -> start simulation
- * Simulation이 성공적으로 실행되면 Output핀의 Value가 기록된다. 유의할 점은 Gate 마다 딜레이가 있기 때문에 결과값이 밀려 보이는 것이 이상한 것이 아니다.

6. Delay 조정

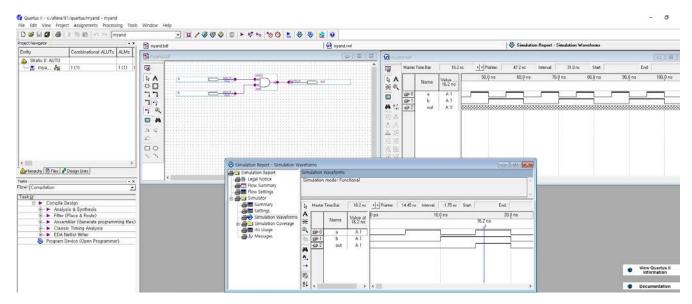
- delay를 없애기 위해서 Simulator tool에서 Simulation mode를 timing에서 functional로 바꾸어 delay를 처리한다.

7. 이후의 모든 Vector Waveform 컴파일은 Simulator tool 사용

- Simulator tool -> Simulation mode -> functional -> "Generate Functional Simulation Netlist" -> Start -> Report

[과제] O4주차 실습과제

>> 저의 실행 예는 and 게이트를 테스트 한 것입니다. 여러분께서는 or 게이트를 테스트 해서 과제로 제출하시면 됩니다.



- [과제] 지금까지의 모든 과정을 수행하여 위 예제의 그림처럼 결과 화면(1장)을 제출하세요.(제출파일명 : d_03_이름_학번)
- 1. myor2 프로젝트를 생성 (입력은 a,b, 출력은 out_자신의학번)
- 2. Block Diagram 설계
- 3. Vector Waveform 의 Report 결과