OSFP-RHS 400GBASE-DR4 Optical Transceiver

LOR400-DR4MC

Description

Fly Global Trading Limited's LOR400-DR4MC modules are designed and optimized for 400G Ethernet and Data center applications. They are compliant with IEEE 802.3bs & IEEE 802.3ck and OSFP MSA. The modules offer 4 independent transmit and receive channels, each is capable of 100Gb/s operation for an aggregate data rate of 400Gb/s over 500m of MPO12 SM fiber . Digital diagnostics functions are available via a 2-wire serial interface.

Applications

- 400G BASE-DR4 Ethernet
- Data Center
- InfiniBand NDR

Standard

- Compliant to IEEE 802.3bs 400GAUI-8
- Compliant to IEEE 802.3ck 400GBASE-DR4
- Compliant to CMIS5.2
- Compliant to OSFP MSA V5.0

Features

- Hot-pluggable OSFP-RHS module
- Single MPO12 receptacle
- 4 duplex channels transceiver module
- Single 3.3V power supply
- Maximum power consumption <9W
- Commercial operating temperature range: 0°C ~ 70°C
- Link distance up to 500m on MPO12 SM fiber
- 4 x 100Gb/s PAM4 SIP Modulator
- Built-in digital diagnostic functions
- I^2C management interface

Ordering Information

Part Number	Description
LOR400-DR4MC	OSFP-RHS, 400GBASE-DR4, 500m, 0°C ~ 70°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Note
Maximum Voltage Supply	V_{cc}	-0.3		3.6	V	
Storage Temperature	T_{st}	-40		85	°C	
Relative Humidity	RH	5		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage (Vcc-GND)	V_{cc}	3.135	3.3	3.465	V	
Power Supply Current	I_{cc}			2700	mA	1
Operating Temperature (Case)	T_{op}	0		70	°C	
Power Consumption				9	W	
Transmission Distance	L1			500	m	
Data Rate	DR		53.125		GBd	
Notes:						
1. Max. current at V_{cc}=3.3V.						

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Input Differential Impedance	Z_{in}	90	100	110	Ω	
Input Amplitude	V_{in-pp}			900	mV	
Receiver						
Output Differential Impedance	Z_{out}	90	100	110	Ω	
Differential Data Output Swing	V_{out-pp}			900	mV	

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Wavelength (range)	λ	1304.5	1311	1317.5	nm	
Side-mode suppression ratio (SMSR),	SMSR	30			dB	
Optical Output Power	P_o	-2.9		4.0	dBm	
Outer Optical Modulation Amplitude (OMA)	P_{oma}	-0.8		4.2	dBm	
Launch power in OMAouter minus TDECQ, each lane (min): for extinction ratio >= 4.5 dB		-2.2			dBm	
Launch power in OMAouter minus TDECQ,		-1.9			dBm	

each lane (min): for extinction ratio < 4.5 dB						
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5			dB	
Average launch power of OFF transmitter, each lane				-15	dBm	
Optical Return Loss Tolerance	T_{RL}			21.4	dB	
Transmitter reflectanced				-26	dB	
Receiver						
Wavelength (range)	λ	1304.5	1311	1317.5	nm	
Average Receive Power, per channel	P_{IN}	-5.9		4.0	dBm	
Receive power (OMAouter), each lane				4.2	dBm	
Receiver sensitivity (OMAouter), each lane	P_{sens}			-4.4	dBm	
Stressed Receiver Sensitivity (OMA), per Lane	SRS			-1.9	dBm	
Overload Input Optical Power	P_{OL}	4.5			dBm	
Receiver Reflectance	R_{RX}			-26	dB	

Principle diagram

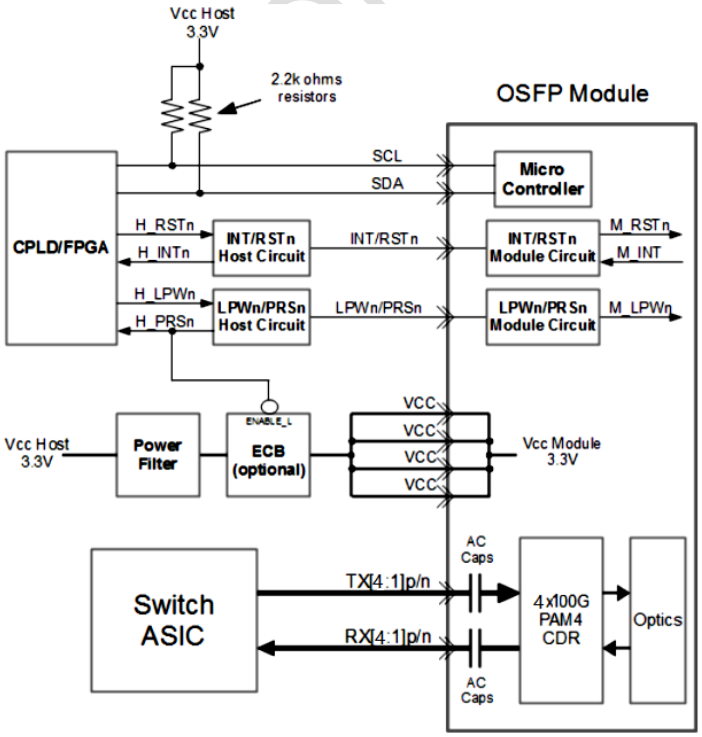


Figure 1. Module Principle Diagram

PIN Definition

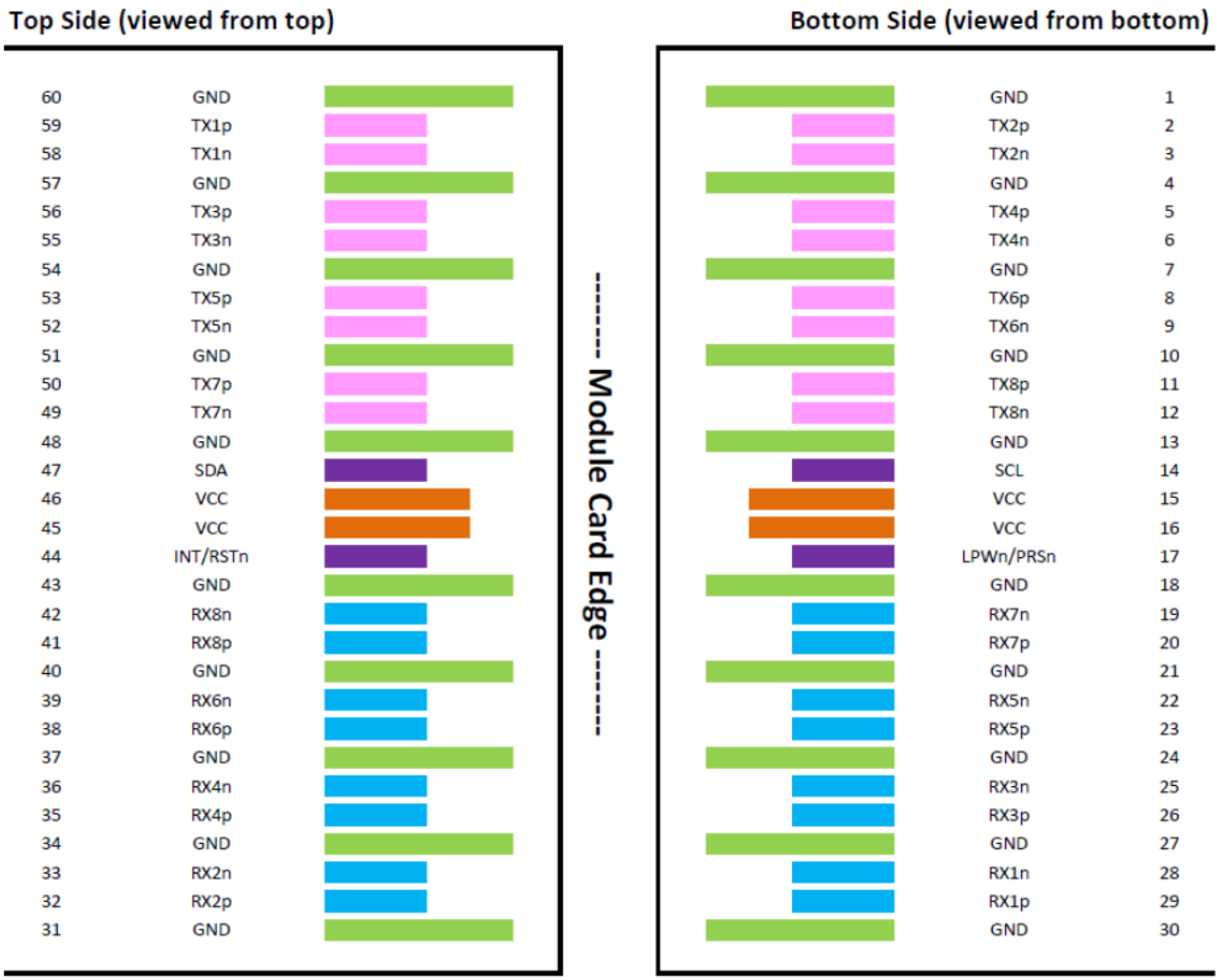


Figure 2. Electrical Pin-out Details

Pin Description

Name	Direction	Description
TX[8:1]p	Input	Transmit differential pairs from host to module
TX[8:1]n	Input	
RX[8:1]p	Output	Receive differential pairs from module to host
RX[8:1]n	Output	
SCL	Bi-directional	2-wire Serial interface clock signal.Requires pull-up resistor to 3.3V on host
SDA	Bi-directional	2-wire Serial interface data signal.Requires pull-up resistor to 3.3V on host
LPWn/PRSn	Bi-directional	Multi-level signal for low power control from host to module and module presence indication from module to host.
INT/RSTn	Bi-directional	Multi-level signal for interrupt request from module to host and reset control from host to module.

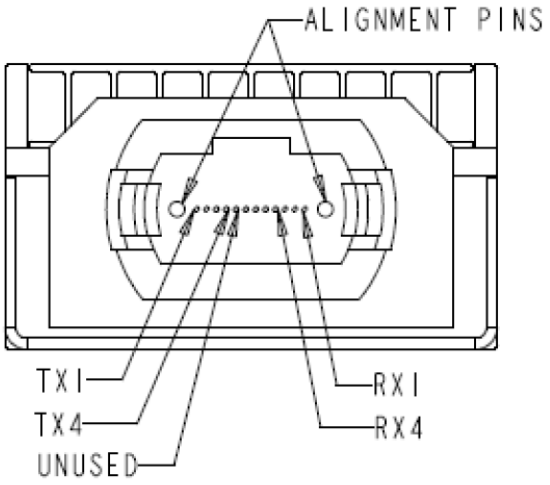
Pin List

Pin	Logic	Symbol	Description	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data	CML-I	Input	3	
3	TX2n	Transmitter Data	CML-I	Input	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data	CML-I	Input	3	
6	TX4n	Transmitter Data	CML-I	Input	3	
7	GND	Ground			1	
8	TX6p	Underfined	CML-I	Input	3	
9	TX6n	Underfined	CML-I	Input	3	
10	GND	Ground			1	
11	TX8p	Underfined	CML-I	Input	3	
12	TX8n	Underfined	CML-I	Input	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS- I/O	Bi-directional	3	Open-Drain with pull up resistor on Host
15	VCC	+3.3V Power		Power	2	
16	VCC	+3.3V Power		Power	2	
17	LPWn/PRSn	Low-Power Mode / Module	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Underfined	CML-O	Output	3	
20	RX7p	Underfined	CML-O	Output	3	
21	GND	Ground			1	
22	RX5n	Underfined	CML-O	Output	3	
23	RX5p	Underfined	CML-O	Output	3	
24	GND	Ground			1	
25	RX3n	Receiver Data	CML-O	Output	3	
26	RX3p	Receiver Data	CML-O	Output	3	
27	GND	Ground			1	
28	RX1n	Receiver Data	CML-O	Output	3	
29	RX1p	Receiver Data	CML-O	Output	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data	CML-O	Output	3	
33	RX2n	Receiver Data	CML-O	Output	3	
34	GND	Ground			1	
35	RX4p	Receiver Data	CML-O	Output	3	
36	RX4n	Receiver Data	CML-O	Output	3	
37	GND	Ground			1	
38	RX6p	Underfined	CML-O	Output	3	
39	RX6n	Underfined	CML-O	Output	3	
40	GND	Ground			1	

41	RX8p	Underfined	CML-O	Output	3	
42	RX8n	Underfined	CML-O	Output	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power	2	
46	VCC	+3.3V Power		Power	2	
47	SDA	2-wire Serial interface data	LVCMOS- I/O	Bi-directional	3	Open-Drain with pull up resistor on Host
48	GND	Ground			1	
49	TX7n	Underfined	CML-I	Input	3	
50	TX7p	Underfined	CML-I	Input	3	
51	GND	Ground			1	
52	TX5n	Underfined	CML-I	Input	3	
53	TX5p	Underfined	CML-I	Input	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data	CML-I	Input	3	
56	TX3p	Transmitter Data	CML-I	Input	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data	CML-I	Input	3	
59	TX1p	Transmitter Data	CML-I	Input	3	
60	GND	Ground			1	

Optical Interface Lanes and Assignment

The optical interface port is a male MPO-12 connector. The four fiber positions on the left as shown in below Figure, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1).



Channels Tx1 Tx2 Tx3 Tx4 x x x x Rx4 Rx3 Rx2 Rx1
(x: unused position)

Figure 3. Optical lane sequence

Note：Optical interface is 8° APC MPO-12. Lane sequence is shown in figure 3.

Mechanical Dimensions

LOR400-DR4MC transceiver modules mechanical dimensions. (Unit: mm)

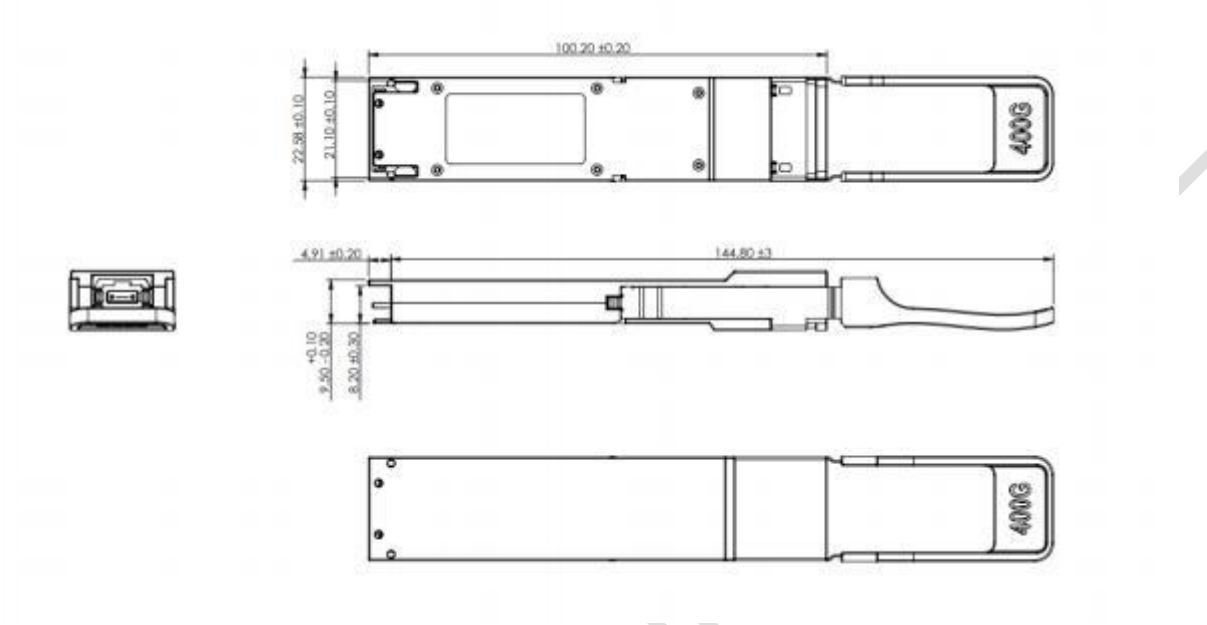


Figure 4: mechanical dimensions

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.