

LQ400-DR4MC

QSFP112 400GBASE-DR4 Optical Transceiver

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Description

Fly Global Trading Limited's LQ400-DR4MC linear driver modules are designed and optimized for 400G Ethernet and Datacenter applications. They are compliant with IEEE P802.3bs and QSFP112 MSA SFF-8665. The modules offer 4 independent transmit and receive channels, each is capable of 100Gb/s operation for an aggregate data rate of 400Gb/s over 500m of single mode fiber. Digital diagnostics functions are available via a 2-wire serial interface.

Applications

- 400G BASE-DR4 Ethernet
- Data Center
- InfiniBand NDR

Standard

- Compliant to IEEE 802.3-2022 400GBASE-DR4
- Compliant to OIF-CEI-5.0
- Compliant to CMIS5.2
- Compliant to RoHS

Features

- Hot-pluggable QSFP112 module
- Single MPO12/APC receptacle
- 4 channels full-duplex transceiver module
- Single 3.3V power supply
- Maximum power consumption < 9W
- Commercial operating temperature range: 0°C ~ 70°C
- Link distance up to 500m over single mode fiber
- 4*112G electrical interface
- Built-in digital diagnostic functions
- I²C management interface

Ordering Information

Part Number	Description
LQ400-DR4MC	QSFP112, 400GBASE-DR4, 500m on SMF, 0°C ~ 70°C

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Note
Maximum Voltage Supply	V _{cc}	-0.3		3.6	V	
Storage Temperature	T _{st}	-20		85	°C	
Relative Humidity	RH	5		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage (Vcc-GND)	V _{cc}	3.135	3.3	3.465	V	
Power Supply Current	I _{cc}			2727	mA	1
Operating Temperature (Case)	T _{op}	0		70	°C	
Power Consumption				9	W	1
Transmission Distance	L	2		500	m	
Data Rate	DR		53.125		Gb/s	
Notes:						
1. Max. current at V _{cc} =3.3V.						

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Input Differential Impedance	Z _{in}		100		Ω	
Input Amplitude	V _{in-pp}		800	1000	mV	
Receiver						
Output Differential Impedance	Z _{out}		100		Ω	
Differential Data Output Swing	V _{out-pp}		400		mV	

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Signaling Rate, each lane(range)			53.125±100ppm		GBd	
Modulation Format			PAM4			
Wavelength (range)	λ	1304.5	1311	1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Optical Output Power,each lane	P _o	-2.9		4.0	dBm	
Optical Modulation Amplitude (OMA),each lane	P _{oma}	-0.8		4.2	dBm	

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Laser Off Power,each lane	P _{off}			-15	dBm	
Extinction Ratio,each lane	ER	3.5			dB	
Optical Return Loss Tolerance	T _{RL}			21.4	dB	
Receiver						
Signaling Rate, each lane(range)		53.125±100ppm			GBd	
Modulation Format		PAM4				
Wavelength (range)	λ	1304.5	1311	1317.5	nm	
Average Receive Power, each lane	P _{IN}	-5.9		4.0	dBm	
Receiver Sensitivity (OMA)	P _{sens}			-4.4	dBm	
Stressed Receiver Sensitivity (OMA), each lane	SRS			-1.9	dBm	
Damage Threshold	P _{DT}	5.0			dBm	
Receiver Reflectance	R _{RX}			-26	dB	

PIN Definition



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Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModselL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode/optional TX Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes

1. GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A.

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ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP112 modules on a single TWI bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any TWI communication from the host. ModSelL signal input node must be biased to the “High” state in the module.

ResetL Pin

The ResetL pin must be pulled to Vcc in the QSFP112 module. A low level on the ResetL pin for longer than the minimum pulse length (t_{Reset_init}) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_{init}) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_{init}) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode/TxDis Pin

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the TWI except during the execution of a reset.

ModPrsL Pin

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector.

IntL/RxLOSL Pin

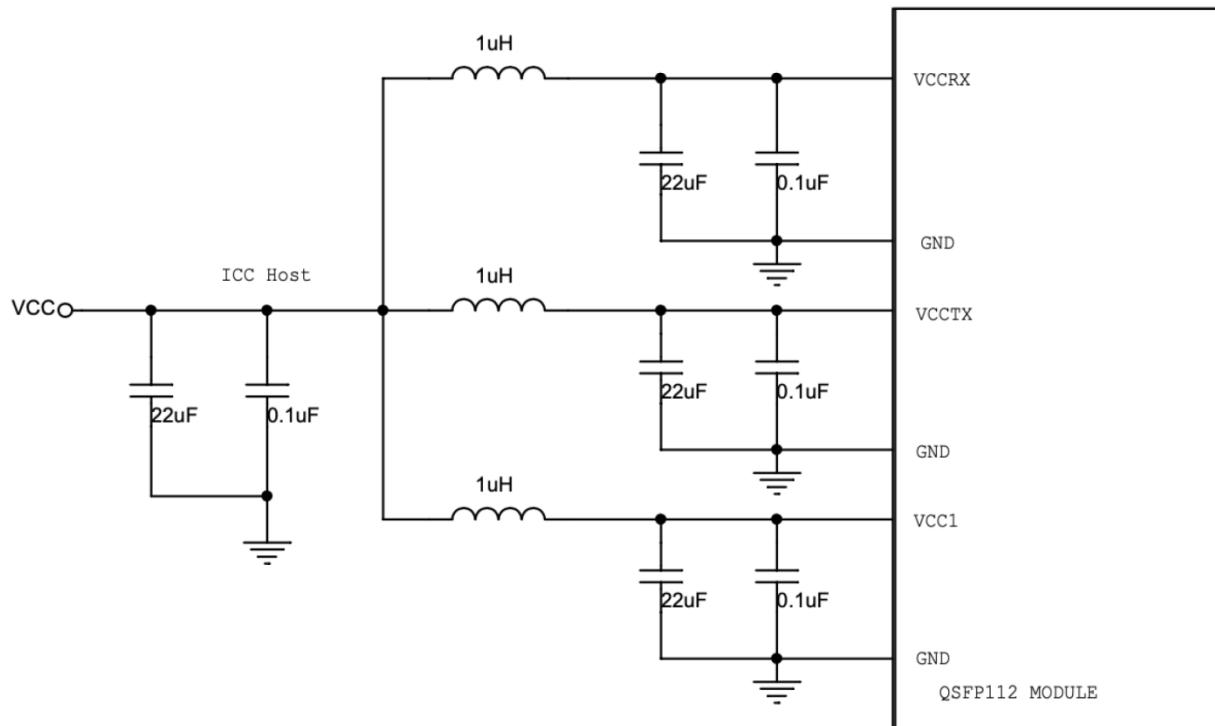
IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board (see Table 4). At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.

If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. “high” indicates that there is no loss of received optical power. Timing requirements

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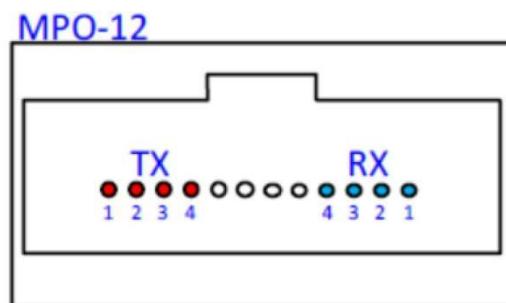
for IntL/RxLOSL including fast RxLOSL mode are found in Table 15. The actual condition of loss of optical receive power is specified by other governing documents, as the alarm threshold level is application specific. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.

Recommended Host Power Supply Filtering



Optical Interface Lanes and Assignment

The optical interface port is a male MPO connector. The four fiber positions on the left as shown in below Figure, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1).



Management Interface

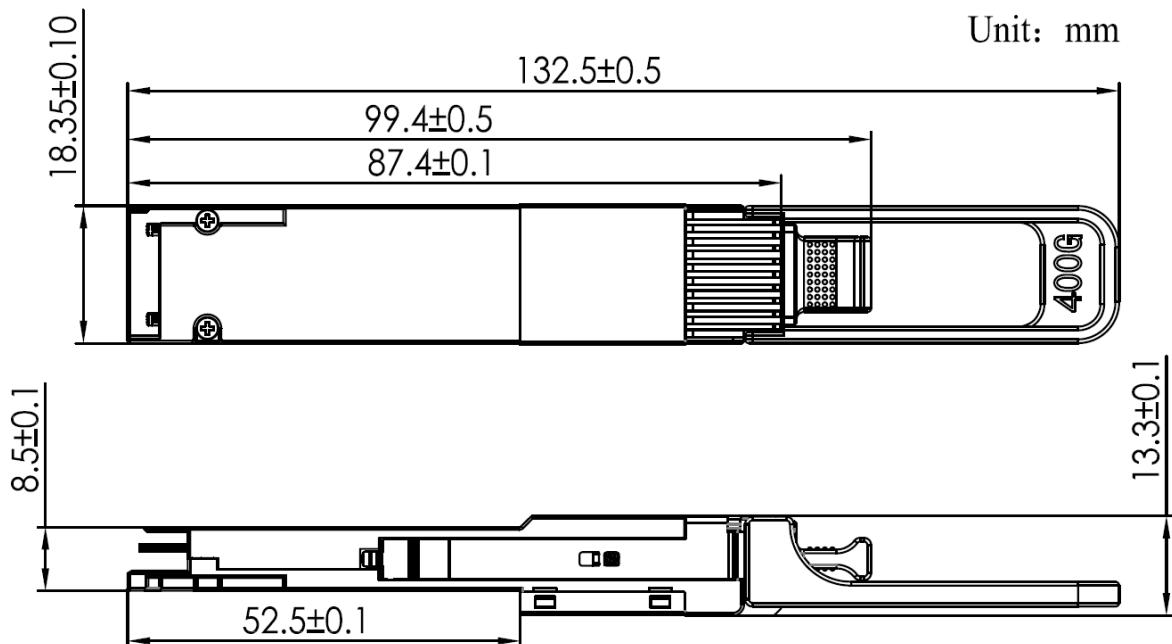
Digital diagnostics monitoring function is available on all 400G QSFP112 SMF modules. The 2-wire serial interface provides path to contact with module in user side. Memory space is arranged into a

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lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Selection function. The interface address A0h is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, then IntL has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

Mechanical Dimensions

LQ400-DR4MC transceiver modules mechanical dimensions. (Unit: mm)



⚠ CAUTION

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.