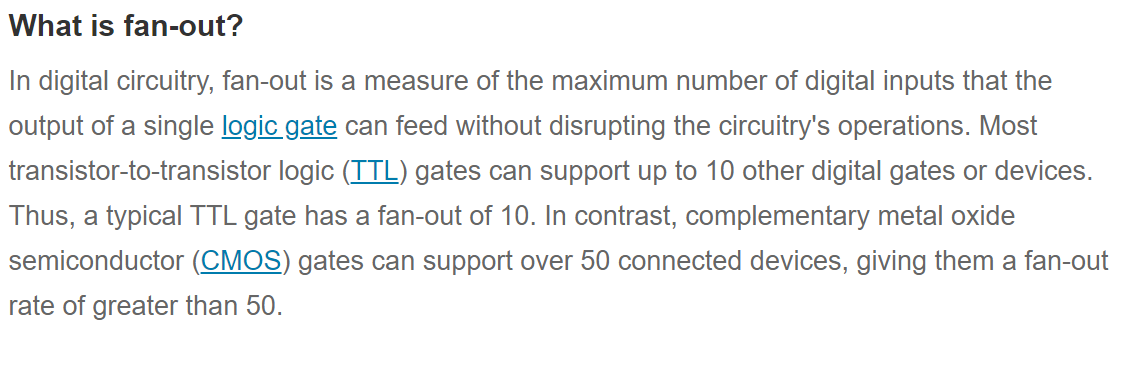
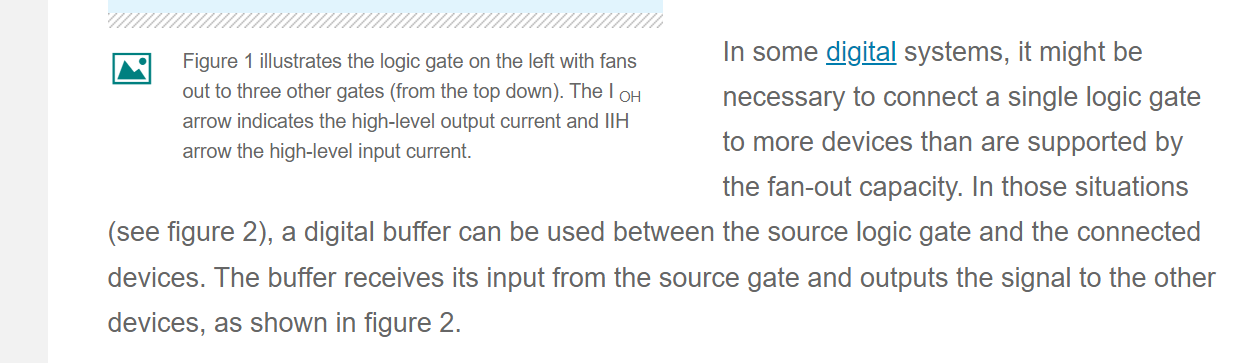
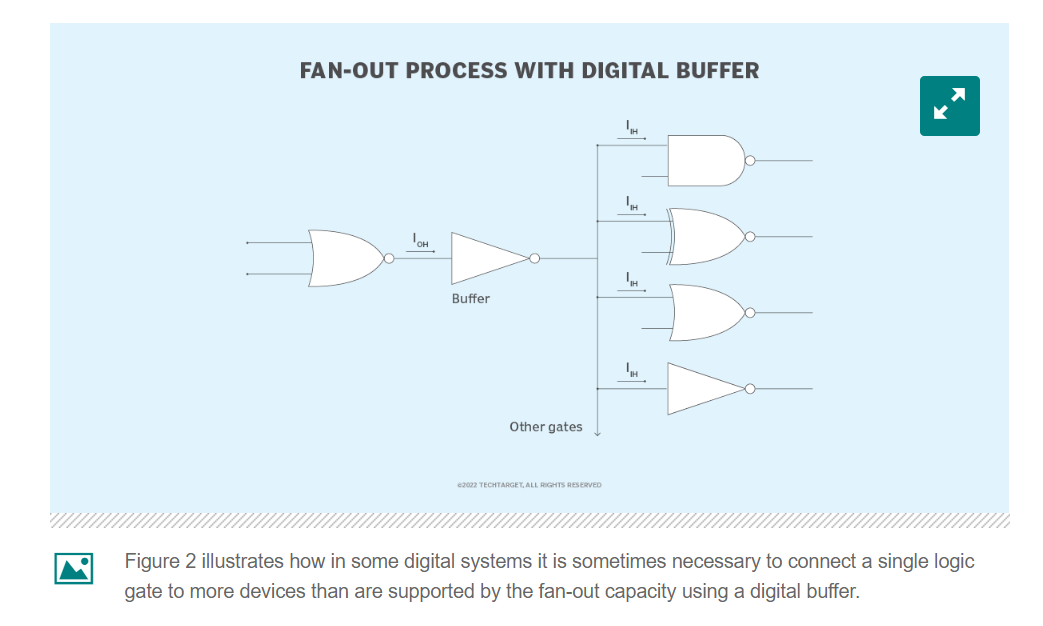
**lecture -1**

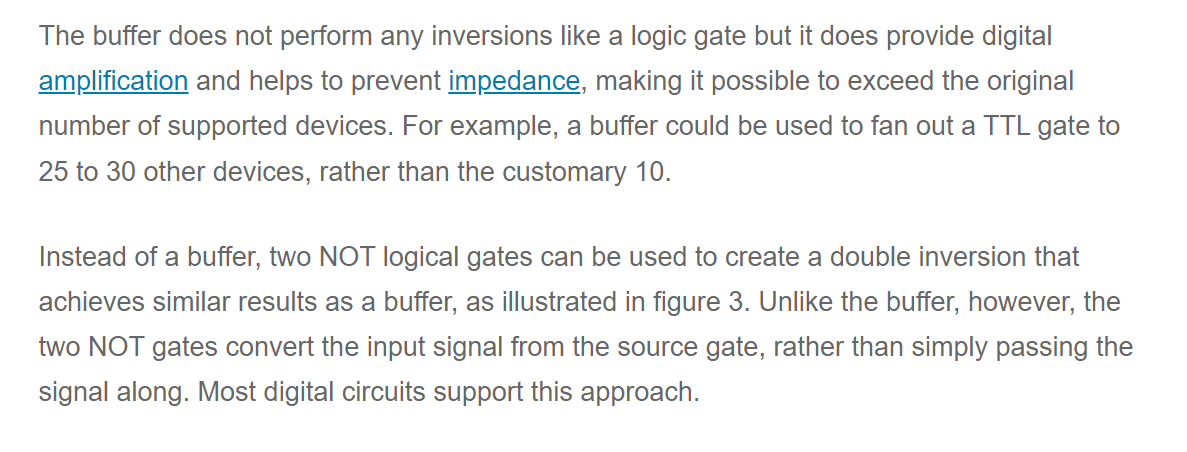
Fanout–

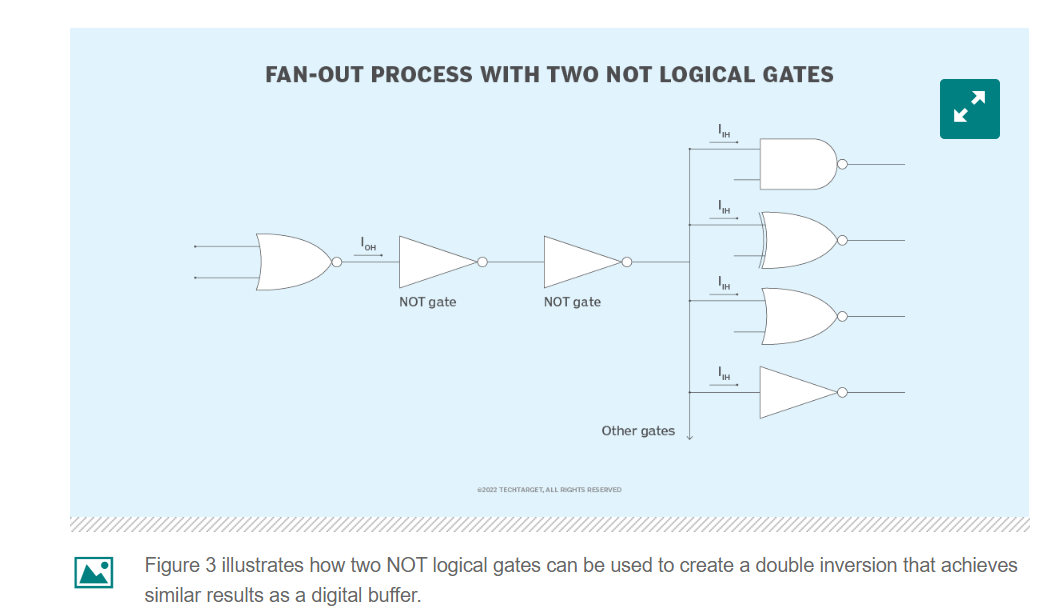


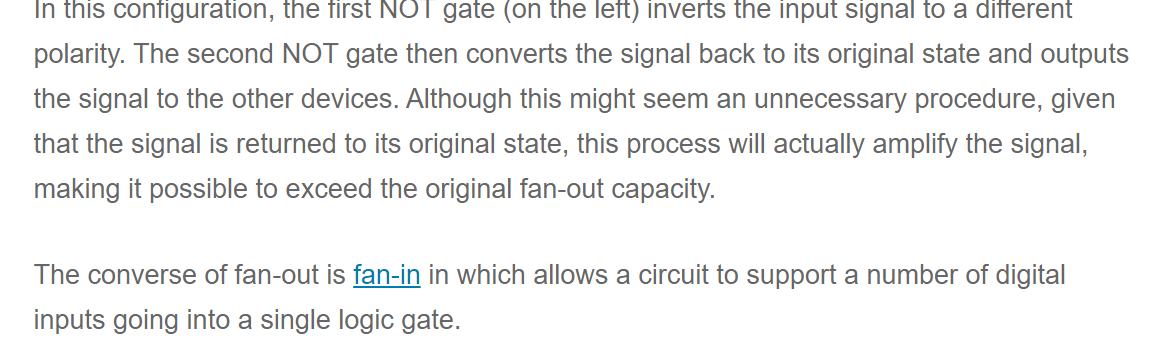










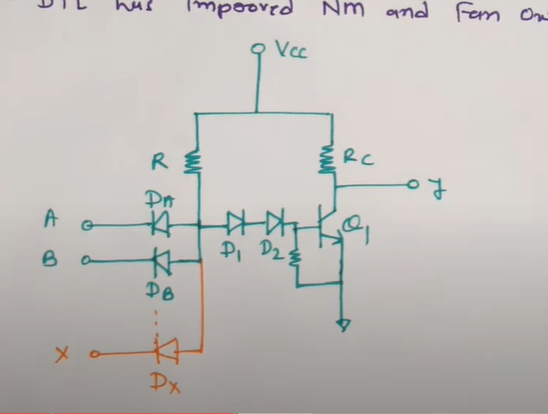


Lecture- (DTL NAND GATES) [ENGINEERING FUNDA]

DISADVANTAGES OF RTL GATES WERE–

1. Rtl families has low noise margin, low fan out, slow speed and higher power dissipation so we dont need rtl in recent ic’s
2. Dtl has improved noise margin and fan out compared to rtl

Diagram of dtl nand gate:



When A=B=0

Voltage supply vcc comes to the path of Diode Da and Db and these diodes works in the forward bias direction as potential difference between terminals having in fb, thats why diodes d1 and d2 works in the reverse bias and base current to this q1 that will be minimum and as base current to this q1 is minimum this q1 will be off and because of the off of q1 , output y will be vcc and vcc means active high signal so here for 0 0 output will be 1

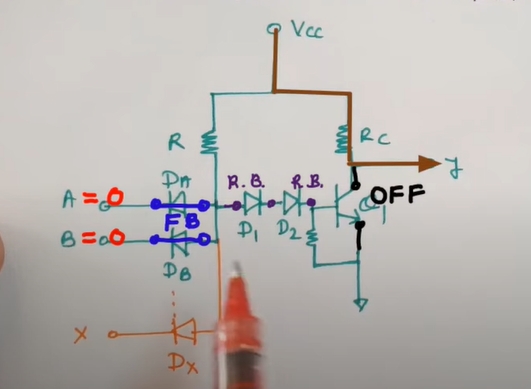
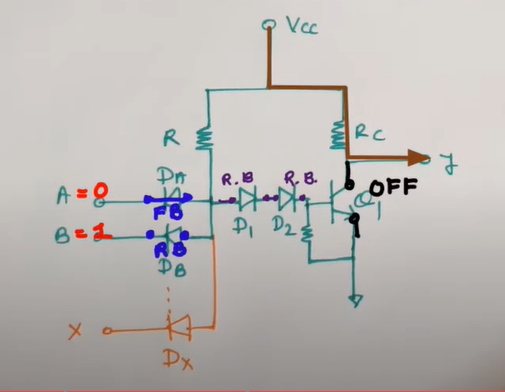


Diagram when a=b=0

2. When A=0,B=1



As A=0 so Diodes dA will come into forward bias and dB will come in the reverse bias. But as dA is in forward bias so the diodes d1, d2 will stay in reverse bias and for this base current q1 that will be zero one can say ideally and as this q1 is off so our output that will be happening as per vcc so that is active high so output will be 1

3.A=1,B=0

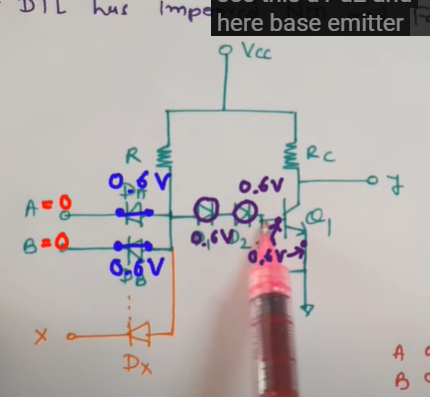


As A=1 so diode da will be in reverse bias and B=0 so dB will be in forward bias so the vcc that is having the path through dB and diodes d1,d2 that will stay the reverse bias and for this base current to this q1 will be minimum which will make the q1 off and as this is off our output is happening per vcc directly to the y direction so here also the output is in the active high so output is 1

4 A=1, B=1

For when A=B=1 so dA and dB will stay in the reverse bias so vcc will find the path in that way which will make diodes d1 d2 on means in forward bias and base current to this q1 that will trigger this q1 and that will turn it on and as if it is on our output voltage that will be vc voltage and Vce is 0.2 in case of q1 is on so 0.2 means logic 0 that one can say so this truth table that indicates this circuit is nand gate circuit.

Q. Why do we have this d1 and d2?

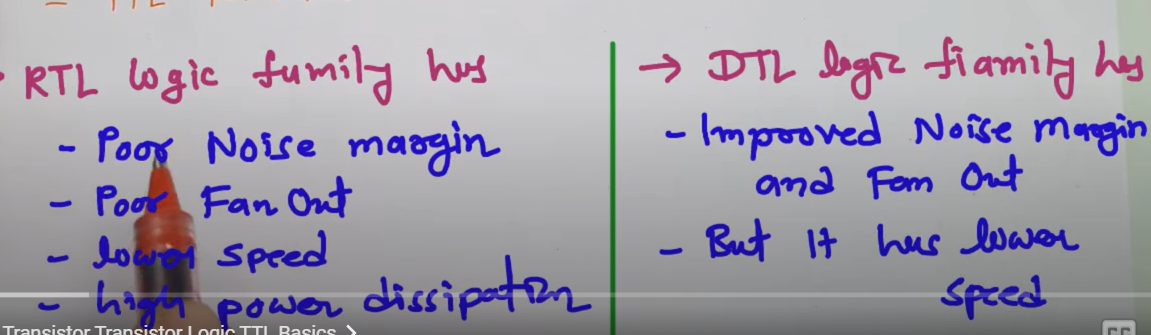
* 

=>when we provide A and B at a time Vcc is having supply over here at this point and as if this is 0 0 in that case as voltage drop across Da or Db that will be 0.6 voltage it will trigger this diode right and the path from Vcc to D1,D2 ,Q1 ,base emitter junction =0.6 to the ground 0.6+0.6+0.6=1.8 volt so the Vcc voltage will trigger Da and Db path rather than d1 d2 path( it will trigger 0.6 voltage rather than 1.8 voltage) so here noise margin of this circuit is getting improved because of this d1 and d2 connection over here, this is how we improve noise margin here compared to the rtl family

Disadvantage of Dtl: - low speed

* Power dissipation as heat

Rtl disadvantages and dtl good-bad sides at a glance



TTL Family

It has 3 section:

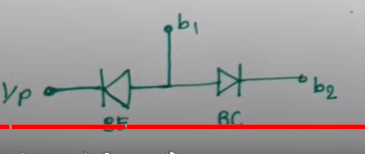
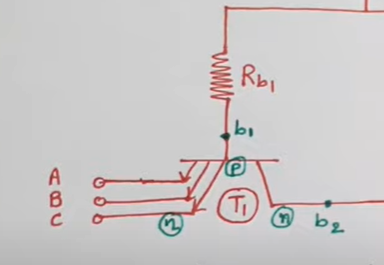
Multi ammeter transistor(input section)

Phase splitter

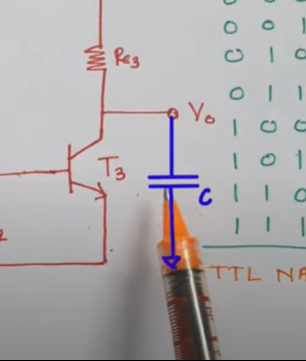
Output section

1. In the input section:

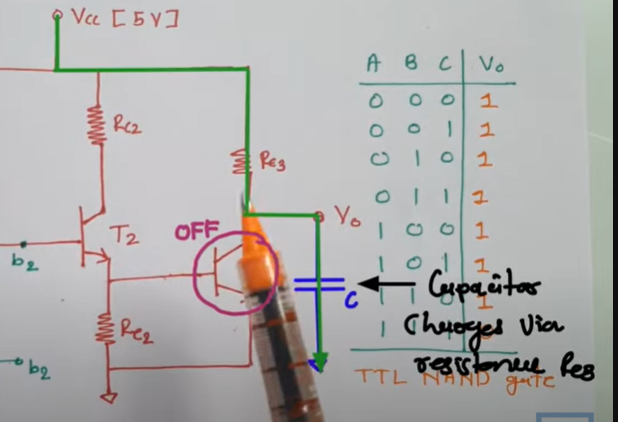
Equivalent input transistor T1–



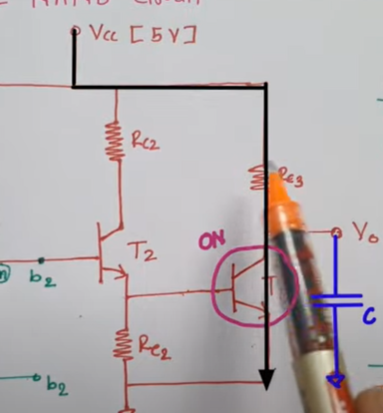
This nand gate that ould be connected to any other further logic gate there will be load capacitance over here ,say that have value c—--



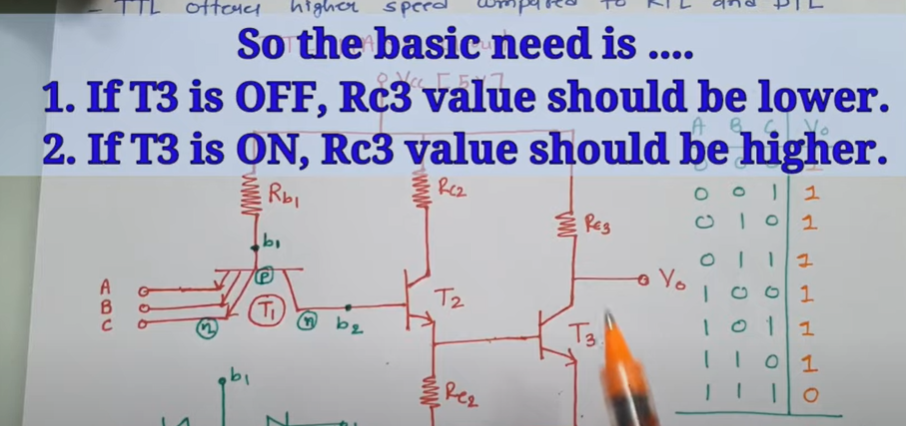
So there can 2 cases when load capacitance is c,



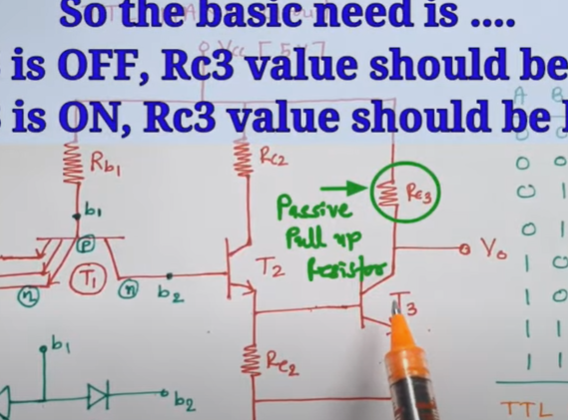
1. If T3 is off then the c will charged via resistance Rc3, then the charging time constant will define the speed of operation, so when capa getting charged and the charging time constant= Rc3XC , to have lower charging time constant, Rc3 have to be lower,
2. But when T3 is on, we will find this Vcc will draw current like the below pic(the black line path)–



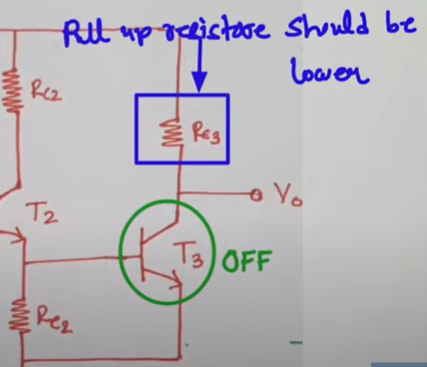
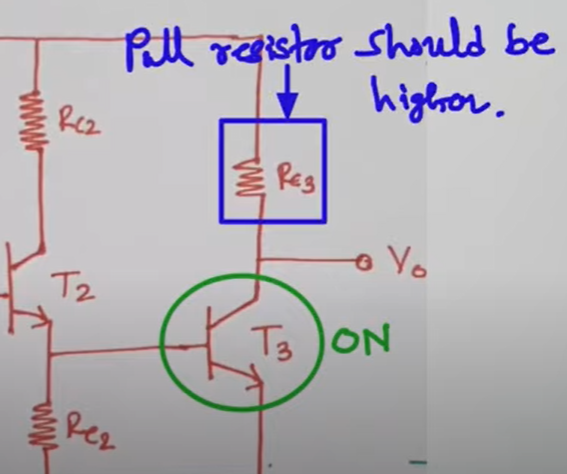
So if Rc3 value is lower, it will draw high current through T3 which requires higher base current on the line of T3, so there (at T3) will be higher power dissipation which will happen through T3 ,so the requirement is—

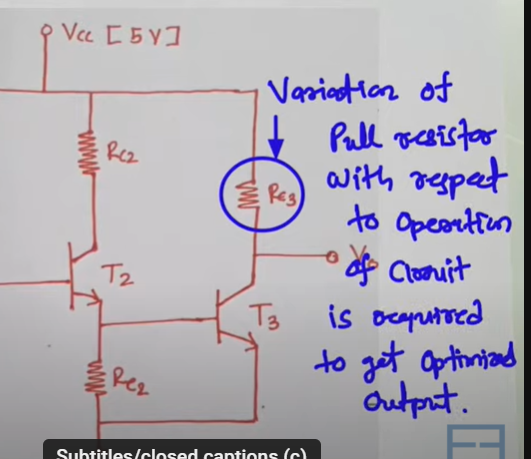


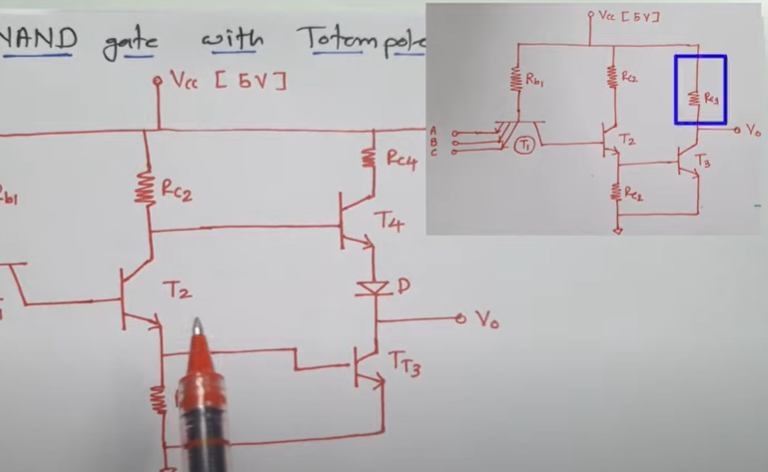
But as Rc3 is a passive resistance so here the resistance cannot due the advantage which we wanted to have right now and this is referred as the passive pull up resistor



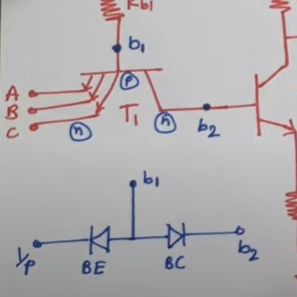
**TTL Nand gate with totem pole output:**

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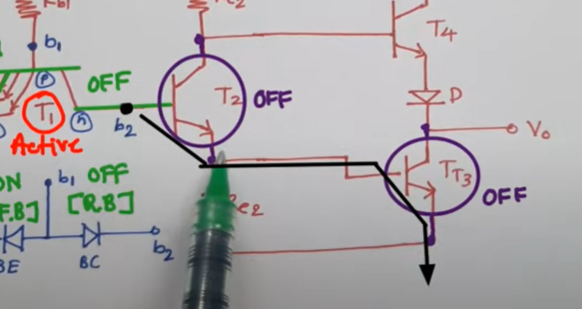
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like before first weve converted the transistor into a circuit in terms of diode

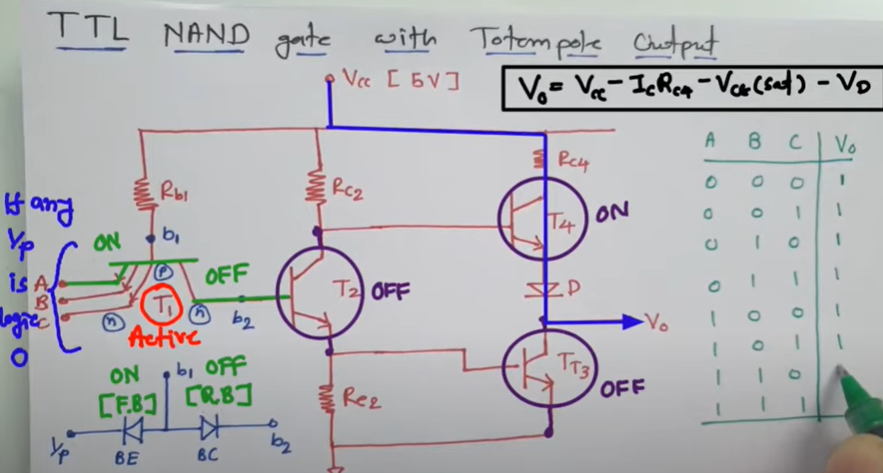
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**Case 1: input 0 0 0**

**If any input is active low(0)** so for that at the input section the base-emitter junction will come in forward bias and this base collector junction will come in reverse bias open circuit will be created between from b1 to b2 and the transistor t1 will come in active region. As b1—b2 is open circuited so the transistor t2 there will be no triggering so this t2 will be off and the transistor 3 needs base triggering t2 is off so this two terminal of T2 is open circuit so that does not allow supply to be given at the base of t3 and as there is no base supply at t3 so that will be off, so the basic condition to have triggering of t2 and t3 is to have a triggering of t2 and t3 at the base terminal of t2 and total voltage that should be b.e(base emitter)

junc of t2 and t3.so at base b2 there should be voltage that should be Vbe2(of T2) and Vbe3(of T3) and that should be 0.7+0.7=1.4 voltage

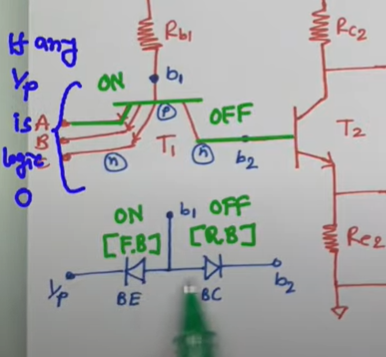
Thats needed at b2 terminal to have triggering of t2 and t3 is off.

**At T4** Vcc voltage now that will give triggering to T4 anf T4 will be on,our output Vo that will driven by Vcc like this -****

**So if we want** to calculate Vo formula is given in the pic above and by applying the formula we will get the output as logic 1 so for any input 0 output will be 1

**Now the case of input 1 1 1:**

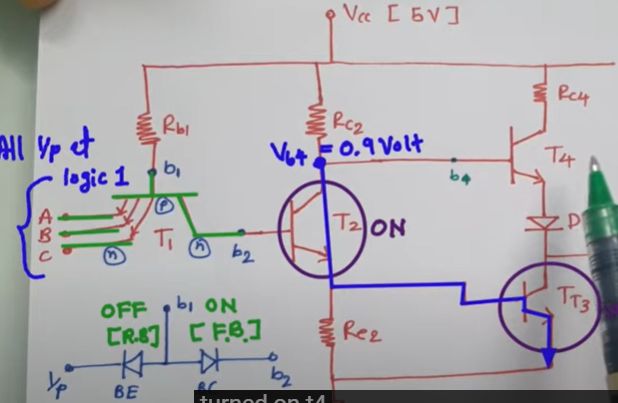
**Here** at T1 b.e junction in rev bias and b.c juntion will be in forward bias so the left part of t1 will be open circuited

****

**Vcc will draw a supply base b2**

**And the tran**sistor will get turned on so this Vcc supply that will draw supply at

**Base of this t3 and t3 will get on for T4**  and tlets say base terminal

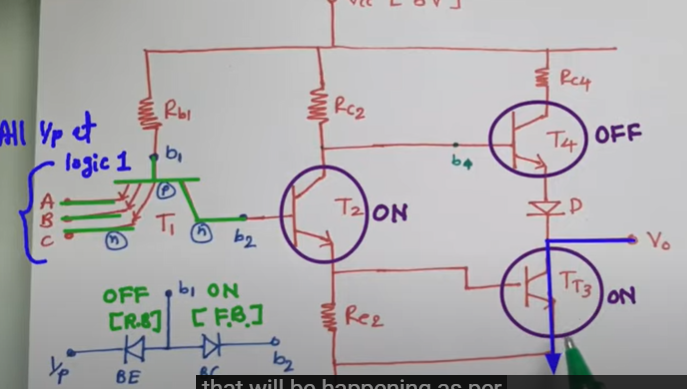
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over here is b4 ,so b4 will justify whether this t4 is on or off so we can observe this base b4 that is having voltage as per as per the loop in blue color shown in the above pic this b4 will have the voltage of Vce2(of T2) →saturation so 0.2 volt and the voltage of Vbe3(of T3) —>0.7 volt so Voltage of b4 will be 0.9 volt. So the condition for T4 to turned on , we need to have at least Vbe4(at T4) + Vd( voltage of the diode connected with t4)

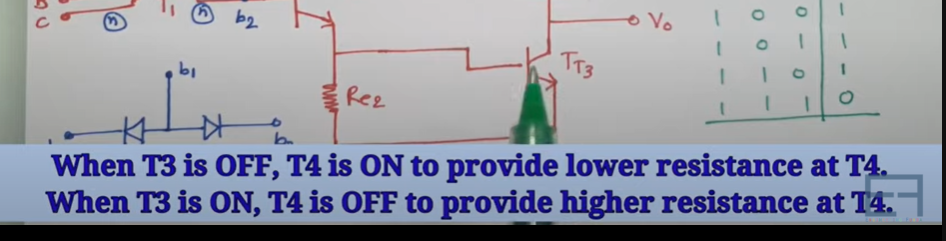
Thats 0.7+0.7=1.4 but here Vb4 that is 0.9 volt is lower

**Than 1.4 that so** t4 will stay in off state so t4 is off and the

Output voltage Vo as per Vce3(of T3) saturation voltage 0.2 volt so we ca say logic 0.

****

**So finally , we** have replaced passive pullup with totempole that is improving fan out

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