MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

MOSFETs are basically of 2 types:

1. Depletion Type MOSFET
2. Enhancement Type MOSFET

MOSFET basically has 4 terminals:

1. Source (S)
2. Drain (D)
3. Gate (G)
4. Body (B)

Depletion type MOSFET:

There is a physical channel between S & D. No separation between S & D

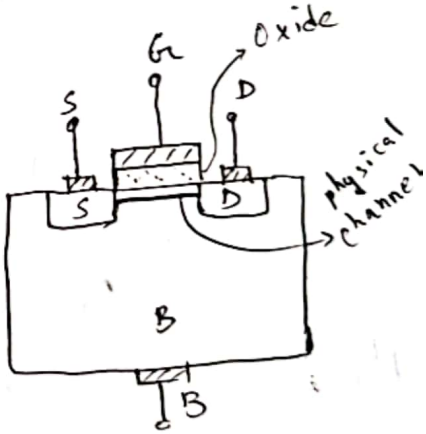


fig: Depletion type MOSFET

Enhancement type MOSFET:

There is no physical channel between S & D. Channel has to be created by applying proper biasing voltage between gate (G) and source (S).

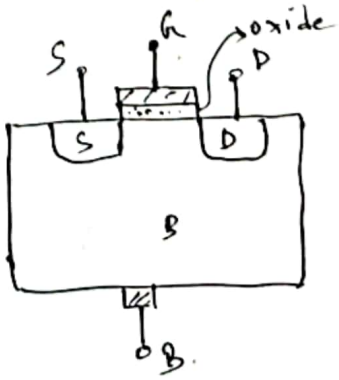


fig: Enhancement type MOSFET

Both Depletion type MOSFET and Enhancement type MOSFET can be categorized either as n-channel MOSFET (nMOS) or p-channel MOSFET (pMOS).

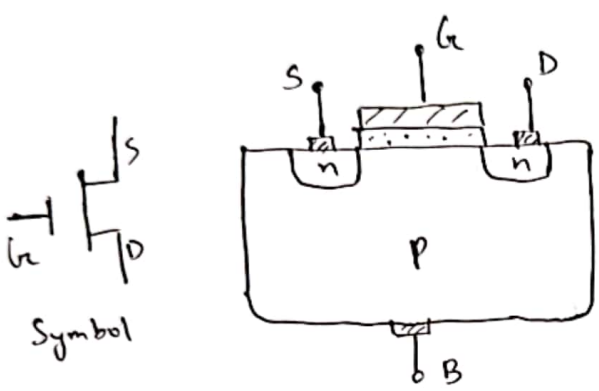


fig: Enhancement Type nMOS

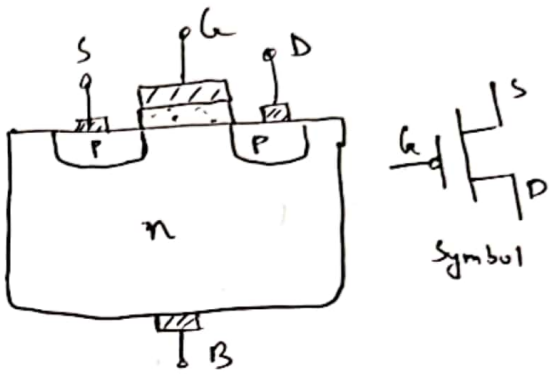


fig: Enhancement Type pMOS

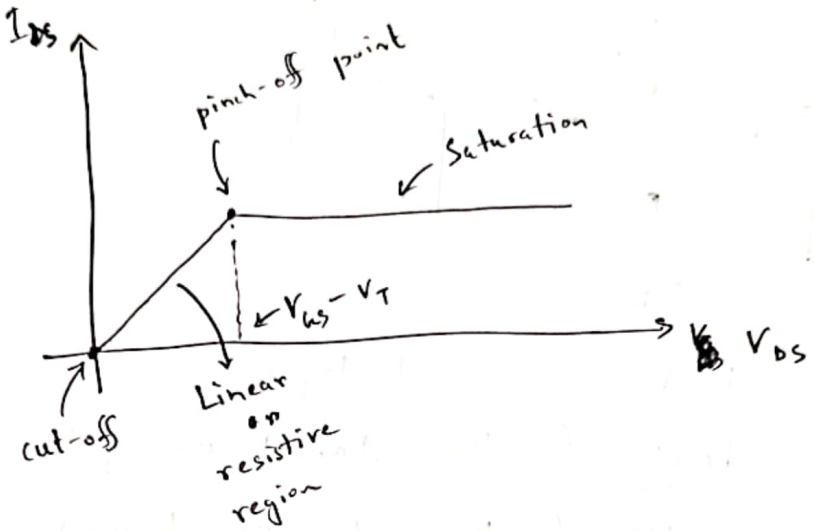
Enhancement type nMOS:

In order to make current flow from D to S channel has to be created between S to D by applying proper voltage (V_{GS}) between G & S. The minimum gate to source voltage (V_{GS}) that is needed to create the channel is called the threshold voltage (V_T).

If $V_{GS} > V_T$ → channel will be created

for nMOS, V_T is (+Ve)

I-V characteristics graph of enhancement type nMOS:



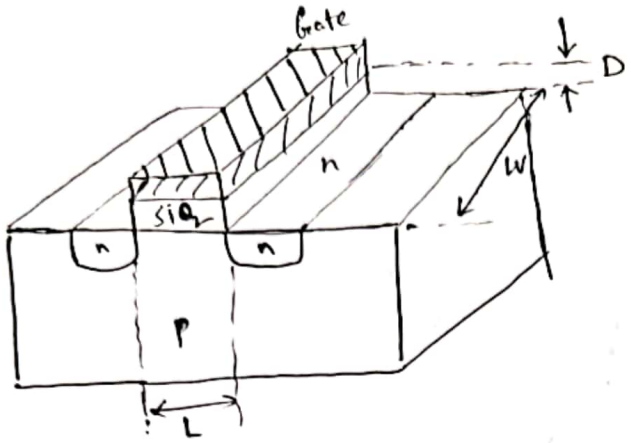
$V_{GS} < V_T \rightarrow$ no channel
$I_{DS} = 0$
} cut-off

$V_{GS} > V_T \rightarrow$ channel will be created
$V_{DS} = 0$
$I_{DS} = 0$
} cut-off (the initial state of Linear region)

$V_{GS} > V_T$
$0 < V_{DS} < (V_{GS} - V_T)$
$I_{DS} > 0$
} Linear or resistive region

$V_{GS} > V_T$
$V_{DS} = (V_{GS} - V_T)$
$I_{DS} > 0$
} pinch-off point (end of linear region & starting point of saturation region)

$V_{GS} > V_T$
$V_{DS} > (V_{GS} - V_T)$
$I_{DS} > 0$
} Saturation region



D → thickness of oxide layer

L → length of the channel or gate

W → width of the gate or channel

In Linear region,

D to S current, $I_{DS} = \frac{\epsilon \mu_n}{D} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$

ϵ → permittivity of oxide layer

μ_n → mobility of electron

$\frac{W}{L}$ → aspect ratio

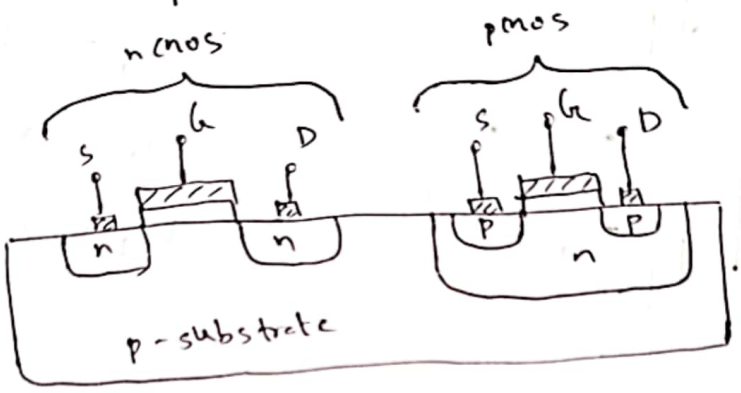
In saturation region,

D to S current, $I_{DS} = \frac{\epsilon \mu_n}{2D} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$

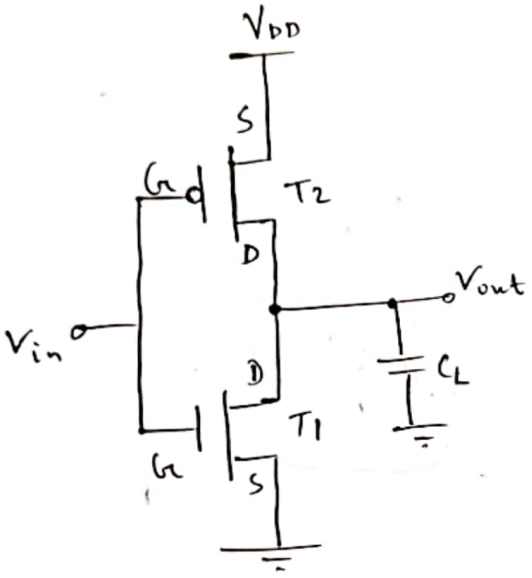
CMOS (Complementary Metal Oxide Semiconductor)

↳ combination of pMOS and nMOS in a single IC

↳ normally a single IC contains symmetrical (complementary) pMOS - nMOS pairs



cMOS Inverter Design (NOT gate)



$T_1 \rightarrow$ nMOS

$T_2 \rightarrow$ pMOS

$V_{Tp} = -1V$

$V_{Tn} = 1V$

$V_{DD} = 2.5V$

$V_{in} \rightarrow$ HIGH (2.5 V)

for T_1,

$V_{in} = V_{GS} = 2.5V$

$V_{GS} > V_{Tn}$

$\therefore T_1$ is ON

for T_2,

$V_{SG} = V_{DD} - V_{in}$

$= (2.5 - 2.5)V$

$= 0V$

$V_{SG} < |V_{Tp}|$

$\therefore T_2$ is OFF

Output capacitor (C_L) will discharge

$V_{out} = 0V$ (LOW)

$V_{in} \rightarrow$ LOW (0V)

for T_1,

$V_{in} = V_{GS} = 0V$

$V_{GS} < V_{Tn}$

$\therefore T_1$ is OFF

for T_2,

$V_{SG} = V_{DD} - V_{in}$

$= (2.5 - 0)V$

$= 2.5V$

$V_{SG} > |V_{Tp}|$

$\therefore T_2$ is ON

Output capacitor will charge through T_2

$V_{out} = V_{DD} = 2.5V$

Important properties of cMOS inverter:

→ The high and Low output levels equal V_{DD} and GND, respectively

→ Ratioless design: which means that logic levels are not dependent on relative device sizes

→ In steady state, a finite resistance path exists between the output and either V_{DD} or GND

→ Input impedance is extremely high. Steady state i/p current is nearly zero. So, a single inverter can theoretically drive an infinite number of gates. (fan-out = infinite). However, increasing fan-out will increase propagation delay

→ No direct path exists between source and ground in steady state operation. Thus, no continuous current flow from V_{DD} to GND. So, static power dissipation is very less.

Input - Output Characteristics of cMOS Inverter

(Voltage - transfer characteristics)

Steps to draw the graph:

→ Sketch the I-V curve of the nMOS and pMOS transformed on a common co-ordinate set for different input voltages

→ Superimpose the two I-V curves of nMOS & pMOS

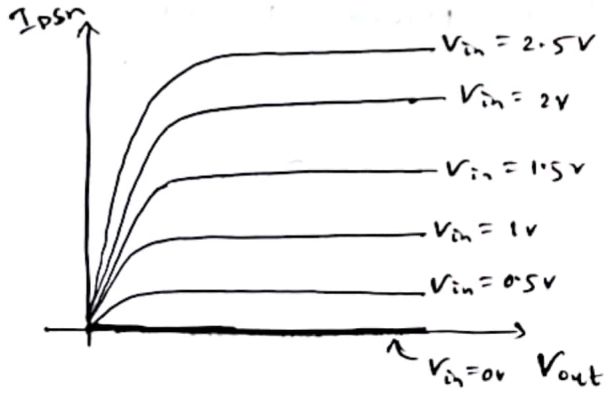
→ Find the operating points of the inverter from the intersecting points between the two curves for each input voltage level

→ Plot the output voltage against the input voltage

Now,

Let, the variables associated with the common cordinate set be: V_{in}, V_{out} & I_{DSn} (Current through nMOS)

→ nMOS IV curve for different values of V_{in}:



$V_{in} = V_{GSn}$

$V_{out} = V_{DSn}$

I_{DSn}

→ pMOS IV curve can be transferred into the same coordinate set variables w.r.t. the following relations

$$I_{DSp} = -I_{DSn}$$

$$V_{GSp} = V_{in} - V_{DD}$$

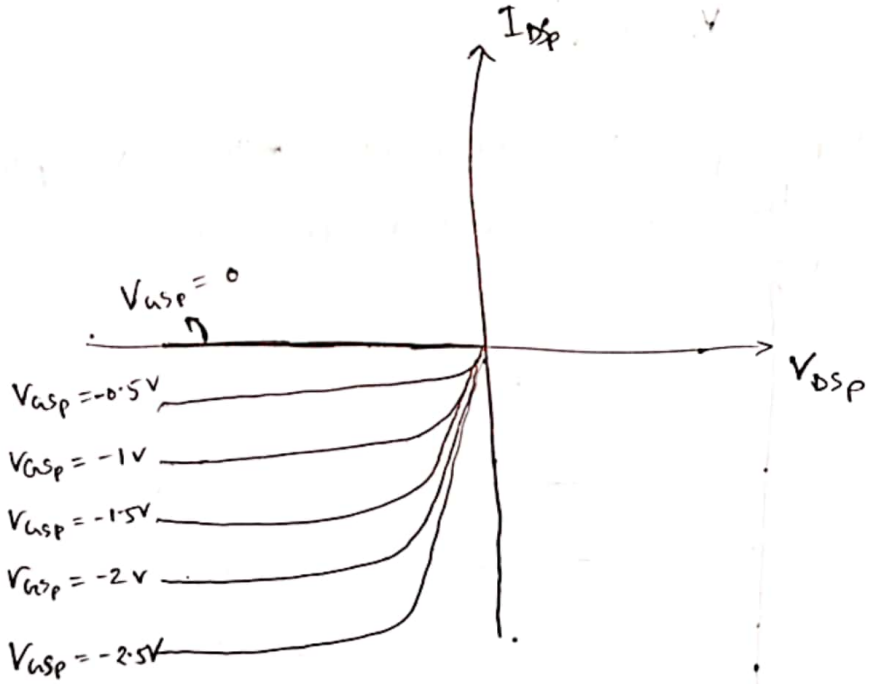
$$V_{DSp} = V_{out} - V_{DD}$$

$$I_{SDp} = I_{DSn}$$

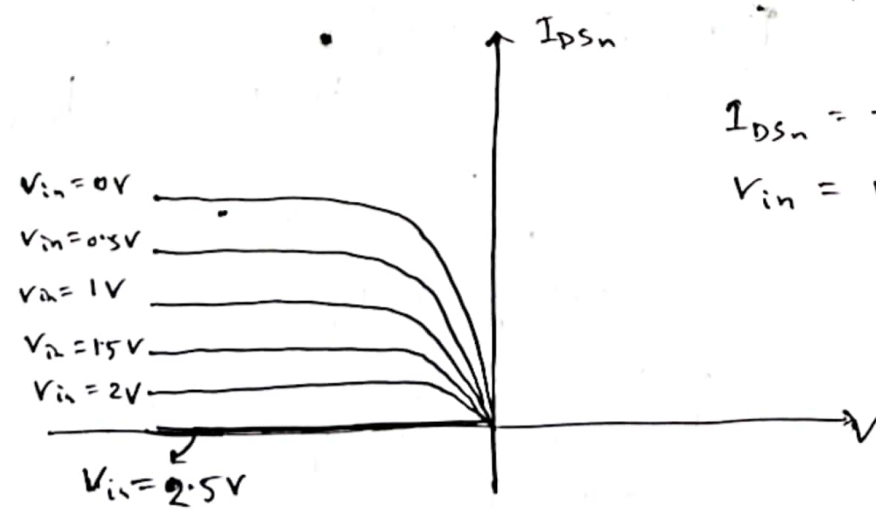
$$V_{SGp} = V_{DD} - V_{in}$$

$$V_{SDp} = V_{DD} - V_{out}$$

pMOS IV curve in terms of I_{DSp}, V_{DSp} & V_{GSp}



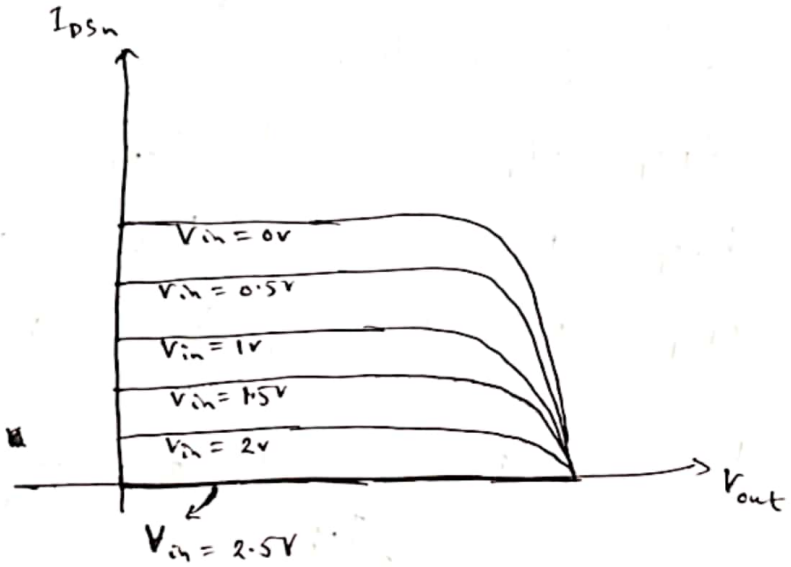
pMOS IV curve in terms of I_{DSn}, V_{DSp}, V_{in}



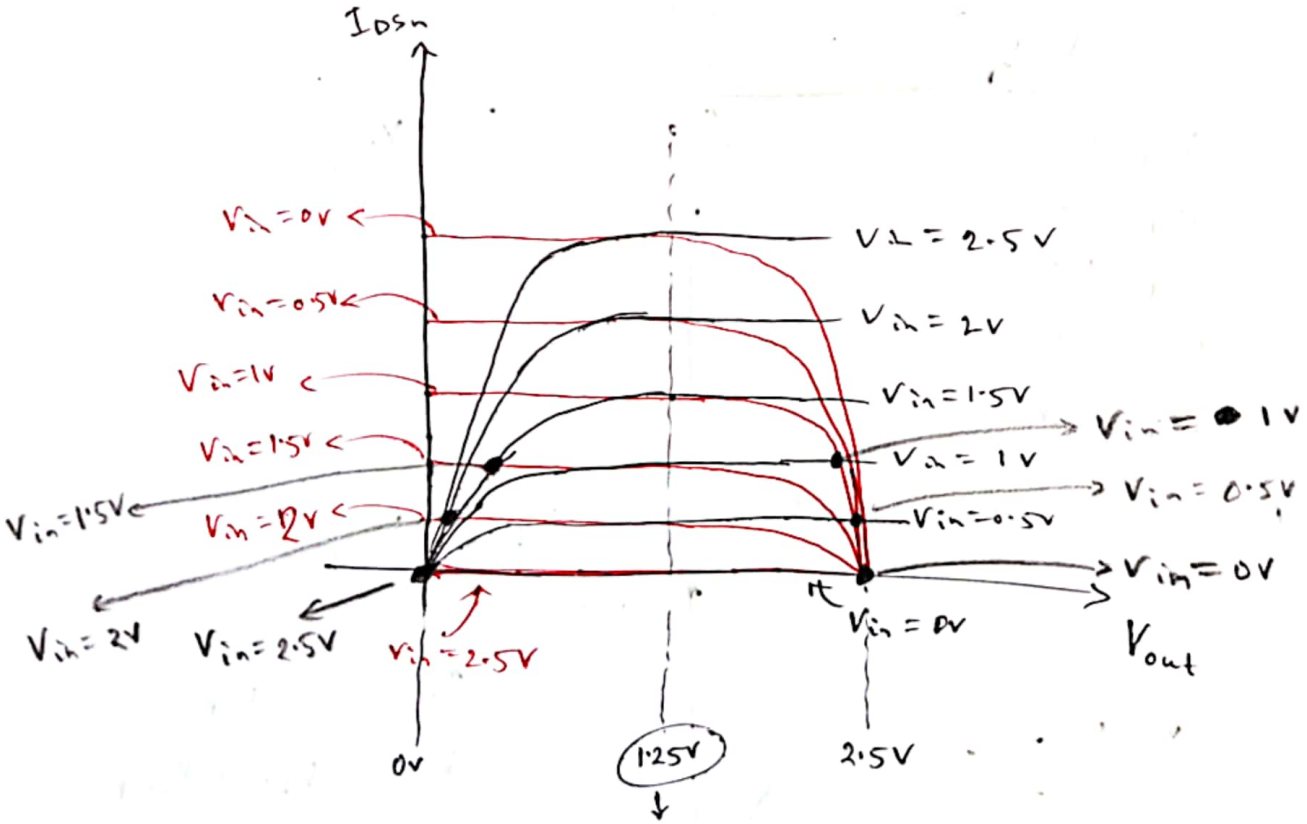
$$I_{DSn} = -I_{DSp}$$

$$V_{in} = V_{DD} + V_{GSp}$$

pMOS IV curve in terms of I_{DSn}, V_{out}, V_{in}



→ Superimposing IV curves of nMOS & pMOS drawn in the same co-ordinate set

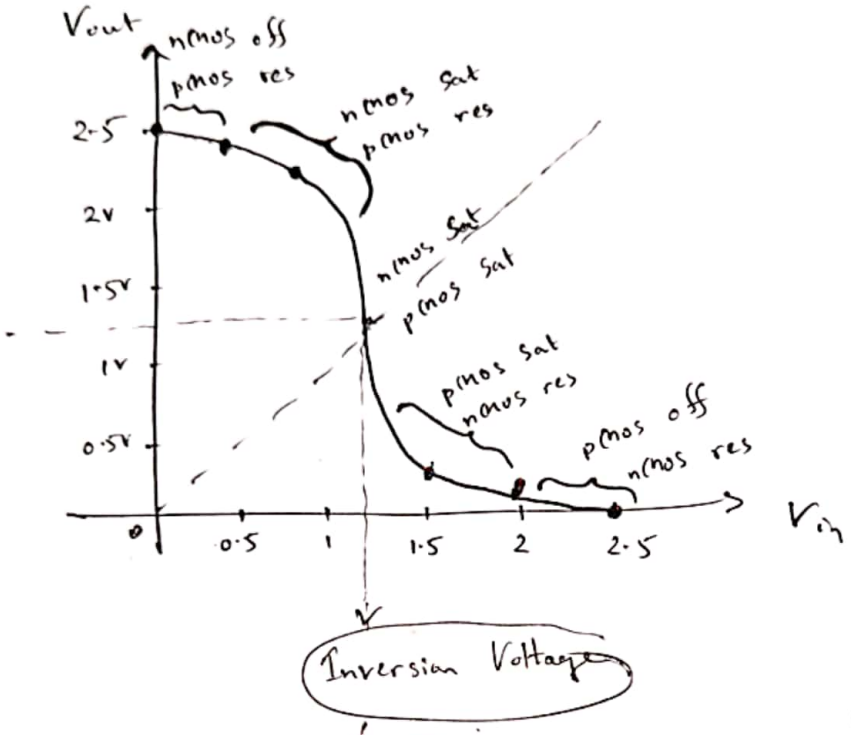


Inversion Voltage

↓

nMOS & pMOS interchange their mode of operation w.r.t this voltage

Input - Output Characteristic graph



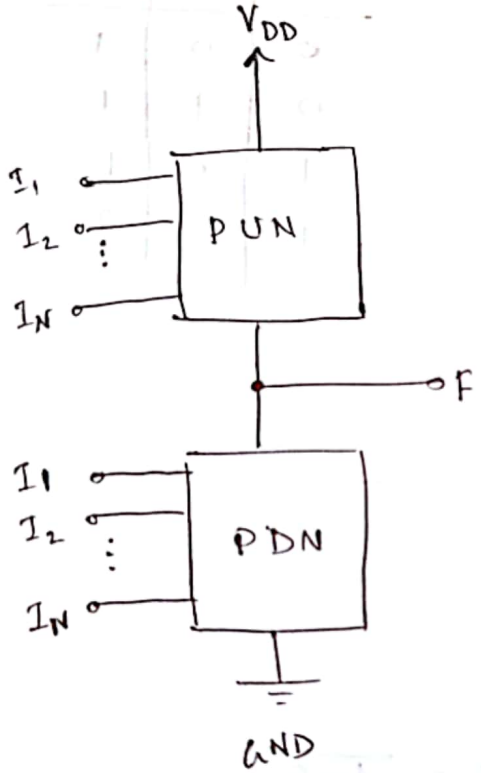
Inversion Voltage

↳ Typically equal to $\frac{V_{DD}}{2}$

Combinational Logic Gates using cMOS

Static cMOS Design

→ Static cMOS gate is a combination of two networks: pull-up network (PUN)
pull-down network (PDN)



PUN → provides a connection between output (F) and V_{DD} when F is supposed to be HIGH

PDN → provides a connection between output (F) and GND when F is supposed to be LOW

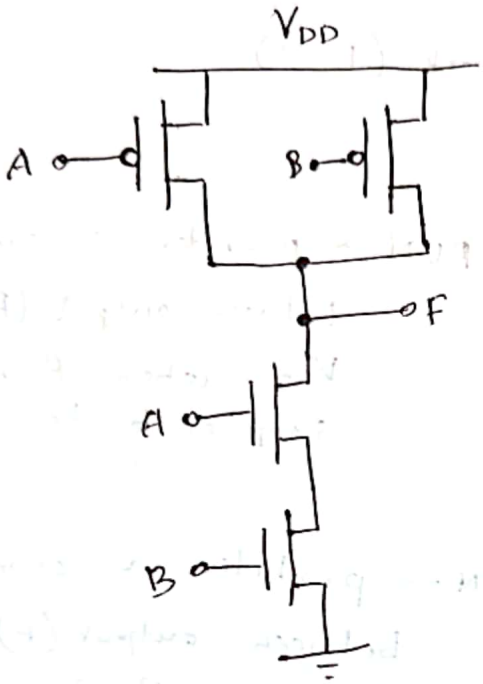
At steady state only one of the networks between PUN & PDN conducts

→ nMOS devices are normally used in the ~~PDN~~ PDN

→ pMOS devices are normally used in the ~~PDN~~ PUN

Two-Input NAND Gate:

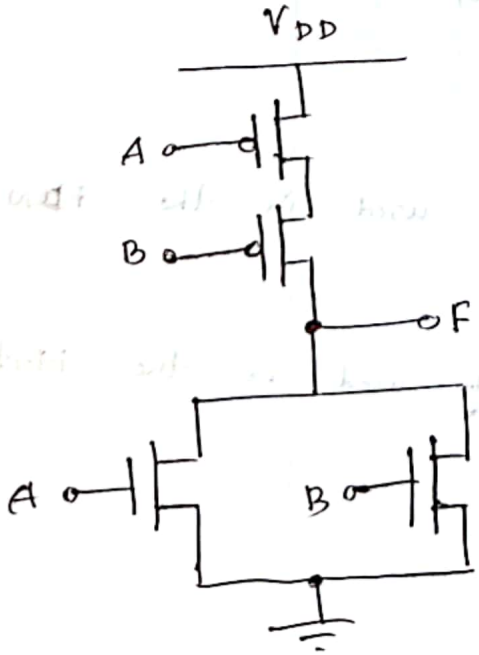
Boolean Expression, $F = \overline{A \cdot B}$



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Two-Input NOR Gate:

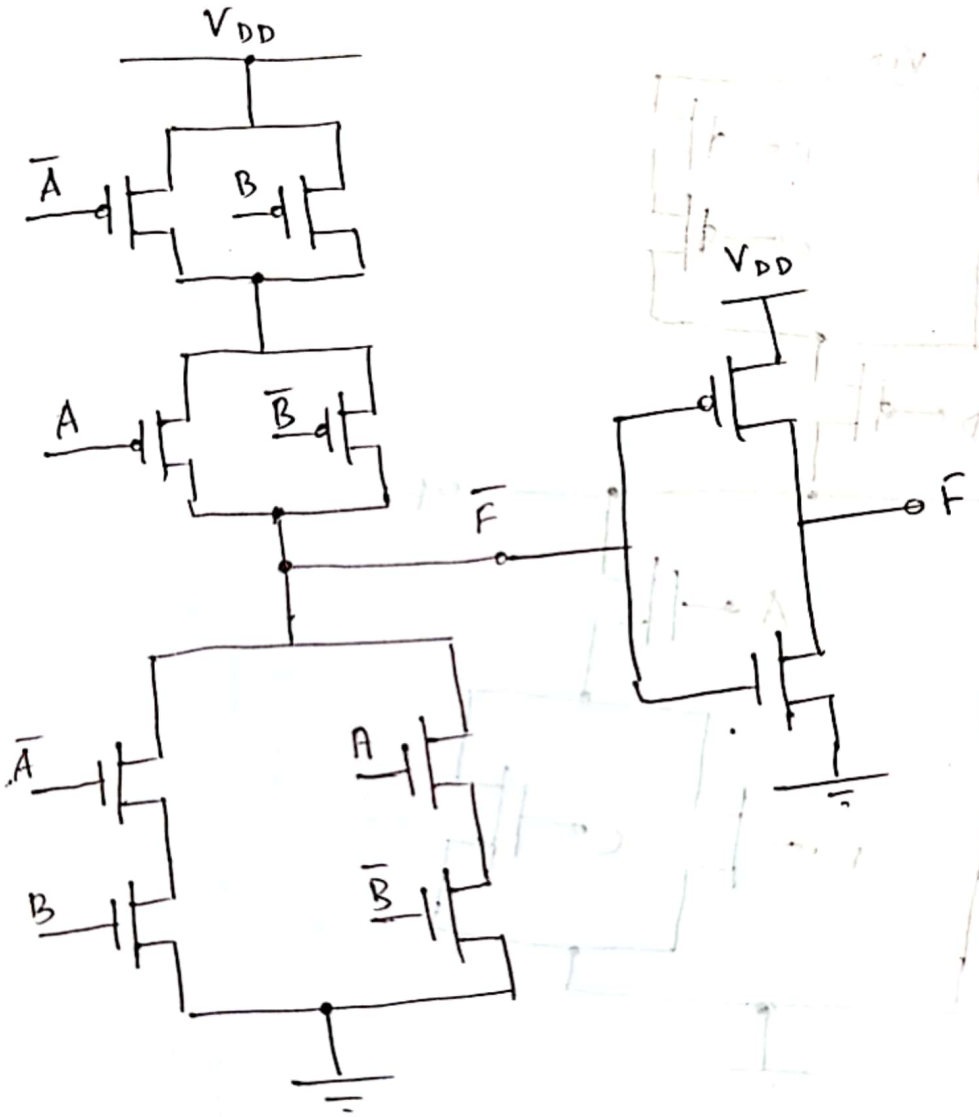
Boolean Expression, $f = \overline{A + B}$



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate

$F = \bar{A}B + A\bar{B}$



XOR Gate :

$$F = \bar{A}B + A\bar{B}$$

$$\bar{F} = \overline{\bar{A}B + A\bar{B}}$$

$$= \overline{(\bar{A}.B)} \cdot \overline{(A\bar{B})}$$

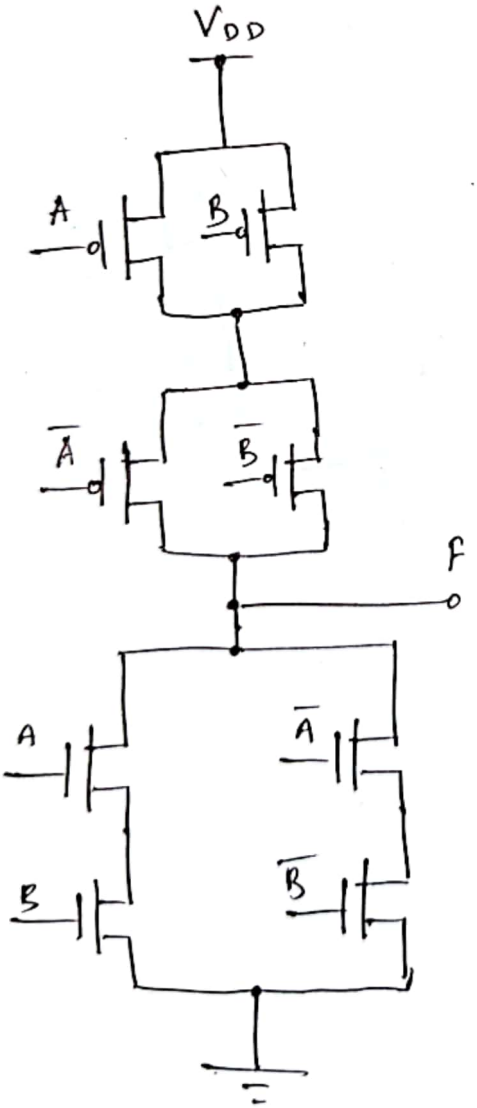
$$= (\bar{\bar{A}} + \bar{B}) \cdot (\bar{A} + \bar{\bar{B}})$$

$$= (A + \bar{B}) \cdot (\bar{A} + B)$$

$$= A \cdot \bar{A} + AB + \bar{A}\bar{B} + \bar{B}B$$

$$= AB + \bar{A}\bar{B}$$

$$\therefore \bar{\bar{F}} = F = \overline{AB + \bar{A}\bar{B}}$$



Example :

$$F = \overline{D + A.(B+C)}$$