Logic family

Logic family means a group of logic ICs which follow similar design architectures, has own set of characteristics, requirements and advantage - disadvantages.

Classification of Logic families

↳ can be classified broadly according to the technologies they are built with:

- → Diode logic (DL)
- → Resistor - Transistor Logic (RTL)
- → Diode - Transistor Logic (DTL)
- → Emitter Coupled Logic (ECL)
- → Transistor - Transistor Logic (TTL)
- → CMOS Logic {

⇒ TTL & CMOS logic family is most widely used IC technologies

Level of Integration

Scheme	Transistors / chip
SSI	< 12
MSI	12 - 99
LSI	1000
VLSI	10K
ULSI	100K
GSI	1 Meg

IC logic gates → SSI

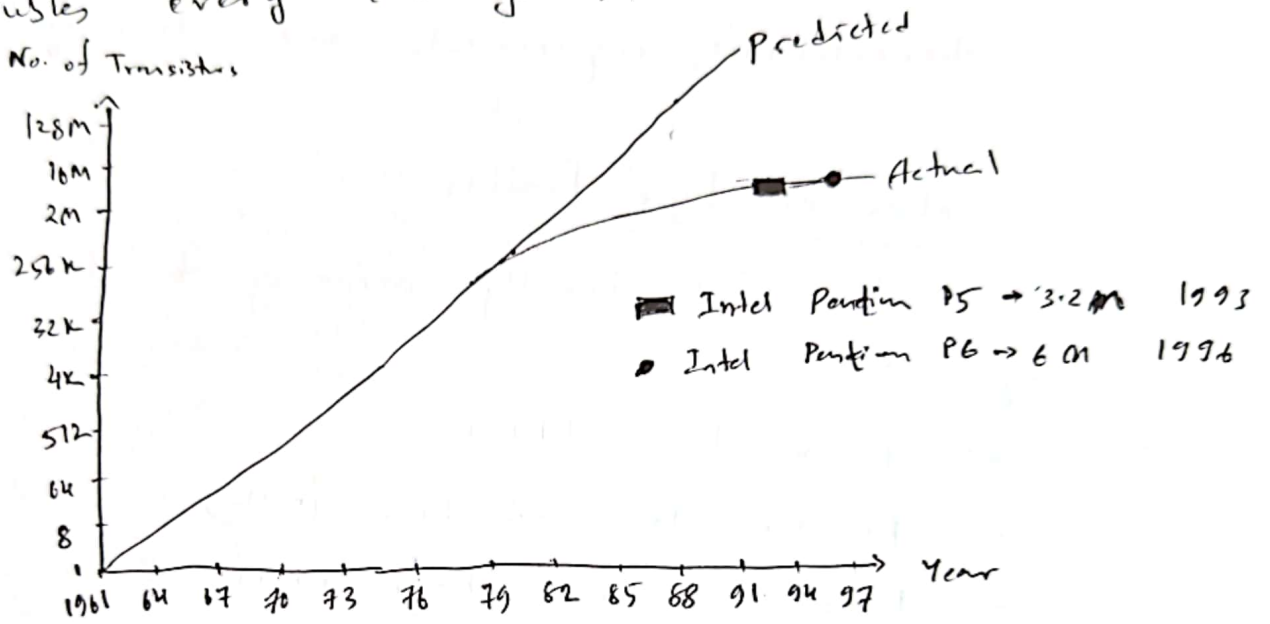
Combinational logic circuits → MSI

Microprocessor → LSI & above

Moore's Law

prediction in 1965

"Number of transistors on a microchip roughly doubles every two years."



Performance Parameters of Logic families

→ Input & Output Current

→ fan-IN , Fan-Out

→ Input & Output Voltage Level.

→ Noise Margin

→ Rise Time, fall Time, Propagation Delay

→ Power Dissipation

Input & Output Currents

I_{OH} → Output current in the logical "1" state under specified load conditions

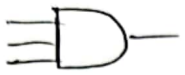
I_{OL} → Output current in the logical "0" state under specified load conditions

I_{IH} → Input current when a specified HIGH level is applied to that input

I_{IL} → Input current when a specified LOW level is applied to that input

Fan In

Fan-in is the number of inputs a logic gate can handle.

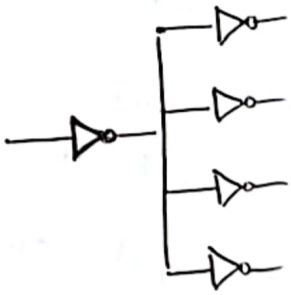


fan-in = 3

Fan Out

In a physical switching system, a particular logic gate is supposed to provide input logic levels to a number of other such gates. The number of gates driven by a single gate is referred to as the fan-out of that driving gate.

→ Fan-out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of the connecting gate



fan-out = 4

$$\text{fan-Out} = \min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$$

for Standard TTL,

$I_{OH} = 400\ \mu A$ $\quad I_{OL} = 16\ mA$

$I_{IH} = 40\ \mu A$ $\quad I_{IL} = 1.6\ mA$

Fan-out = 10

Input & Output Voltage Levels

→ There is a limit on voltage until it is considered High.

→ There is a limit on voltage below which it is considered Low.

V_{OH} (min) : Minimum output voltage in High State (Logic 1)

V_{OL} (max): Maximum output voltage in Low State (Logic 0)

V_{IH} (min): Minimum input voltage guaranteed to be recognized as Logic 1 (High).

V_{IL} (max): Maximum input voltage guaranteed to be recognized as Logic 0 (Low).

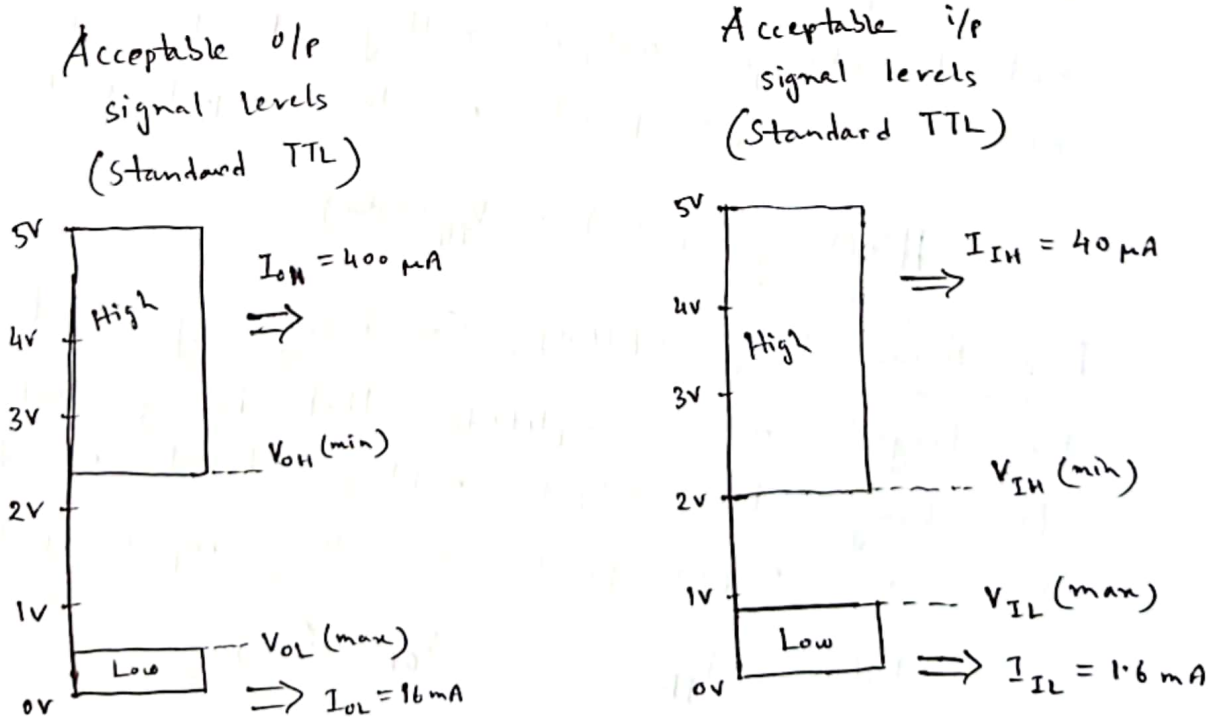


Fig: Standard TTL voltage & current profiles

for Standard TTL,

$V_{OH}(min) = 2.4\ V$

$V_{OL}(max) = 0.4\ V$

$V_{IH}(min) = 2\ V$

$V_{IL}(max) = 0.8\ V$

Noise Margin

→ measures how much external electrical noise a gate can withstand before producing an incorrect outcome

High Noise Margin (HNM): Considering logic level is High, the largest noise amplitude that is guaranteed not to change output voltage level if that noise is superimposed on the input voltage.

$$HNM = V_{OH}(min) - V_{IH}(min)$$

Low Noise Margin (LNM): Considering logic level is Low, the largest noise amplitude that is guaranteed not to change the output voltage level if that noise is superimposed on the input voltage.

$$LNM = V_{IL}(max) - V_{OL}(max)$$

for Standard TTL,

$HNM = 2.4 - 2.0 = 0.4\ V$

$LNM = 0.8 - 0.4 = 0.4\ V$

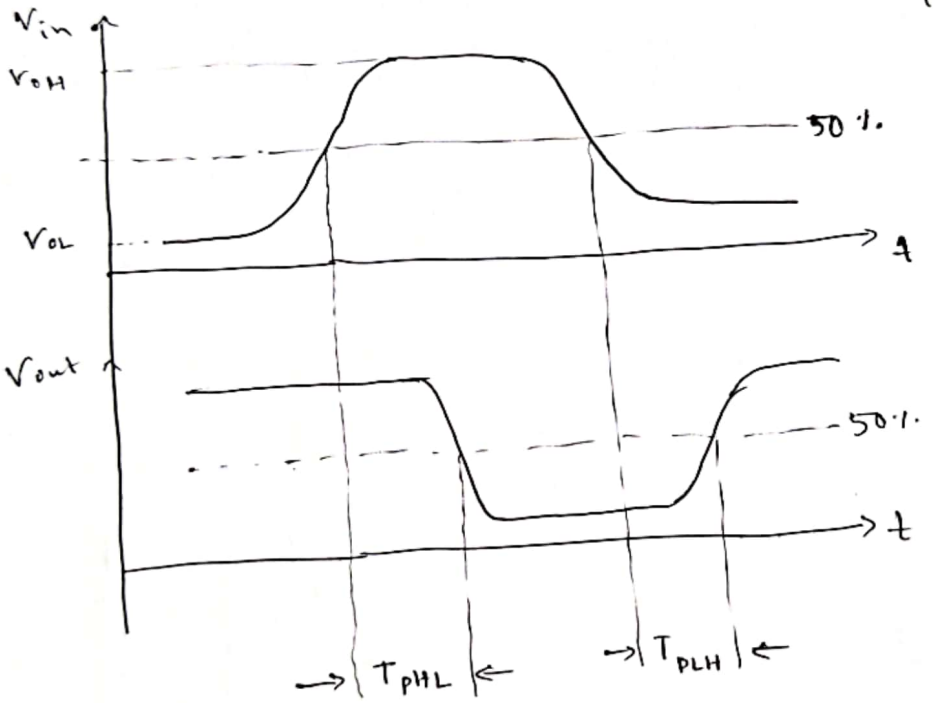
Rise Time, fall Time, Propagation Delay:

Rise Time (T_R)

↳ the duration it takes for a pulse to rise from its 10% point upto its 90% point

fall Time (T_F)

↳ the duration it takes for a pulse to fall from its 90% point to its 10% point



Propagation Delay

↳ measure of how long it takes for a gate to change its state

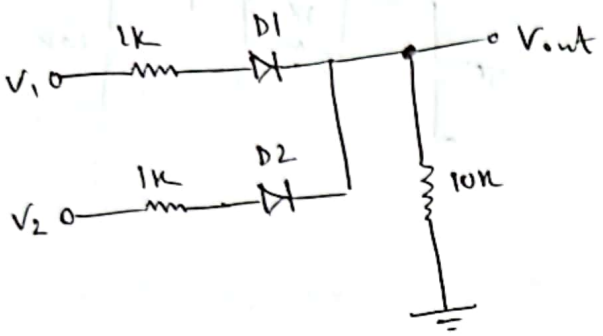
Propagation delay time, $T_P = \frac{T_{PHL} + T_{PLH}}{2}$

T_{PHL} → High to Low propagation delay

T_{PLH} → Low to High propagation delay

Diode Logic Gates (logic implemented using diode & resistors)

OR Gate:



Truth Table

V_1	V_2	V_{out}
0	0	0
0	1	1
1	0	1
1	1	1

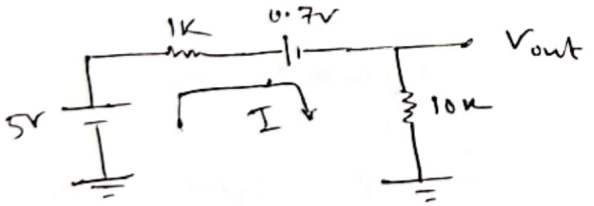
Case 1: $V_1 = 0V$ $V_2 = 0V$

D1 → RB D2 → RB

$V_{out} = 0V$

Case 2: $V_1 = 0V$ $V_2 = 5V$

D1 → RB D2 → FB



$-5 + (1K)I + 0.7 + (10K)I = 0$

$\Rightarrow (11K)I = 4.3$

$\therefore I = \frac{4.3}{11K} = 0.4 mA$

$\therefore V_{out} = (10K) * (0.4 mA) = 4V$

Case 3:

$V_1 = 5V$ $V_2 = 0V$

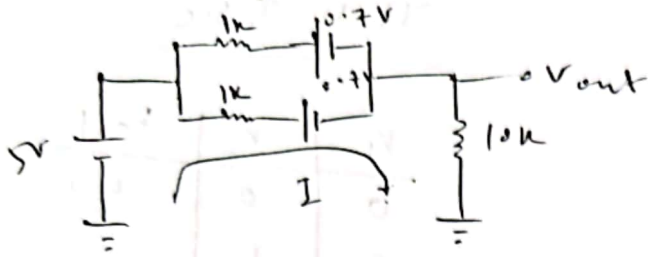
D1 → FB D2 → RB

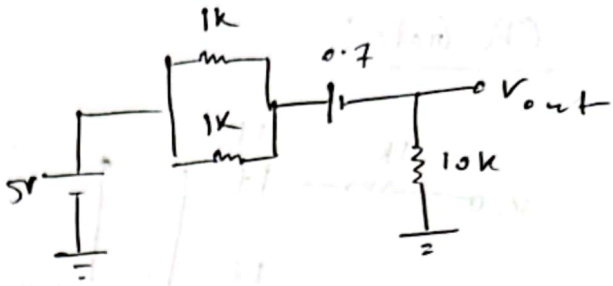
Same as case 2

$V_{out} = 4V$

Case 4: $V_1 = 5V$ $V_2 = 5V$

D1 → FB D2 → FB





$(1K) \parallel (1K) = 500\,\Omega$

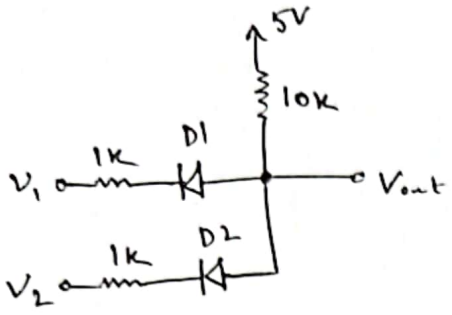
$-5V + (500)I + 0.7 + (10K)I = 0$

$\Rightarrow \quad I \cdot 10500 = 4.3$

$\therefore \quad I = 0.41\ mA$

$\therefore V_{out} = 10K \times (0.41\ mA) = 4.1\ V$

AND Gate:

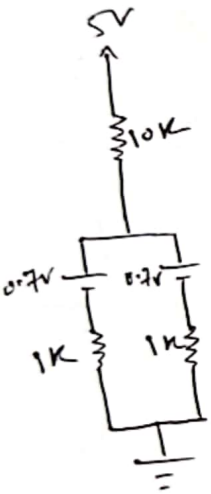


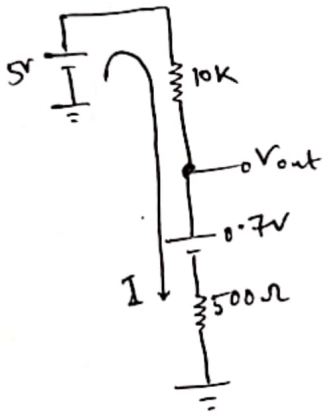
Truth Table

V_1	V_2	V_{out}
0	0	0
0	1	0
1	0	0
1	1	1

Case 1: $V_1 = 0V$, $V_2 = 0V$

D1 → FB D2 → FB





$-5 + (10K)I + 0.7 + (500)I = 0$

$\Rightarrow (10500)I = 4.3$

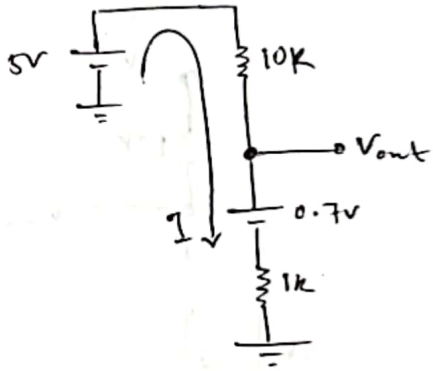
$\therefore I = 0.41\,mA$

$V_{out} = 0.7 + (0.41m) * 500$

$= 0.905\,V$

Case 2: $V_1 = 0V$, $V_2 = 5V$

D1 → FB D2 → RB



$-5 + (10K)I + 0.7 + (1K)I = 0$

$\Rightarrow (11K)I = 4.3$

$\therefore I = 0.4\,mA$

$V_{out} = 0.7 + (0.4m) * 1K$

$= 1.1\,V$

Case 3: $V_1 = 5V$, $V_2 = 0V$

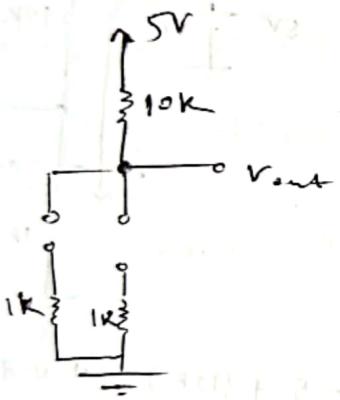
D1 → RB D2 → FB

Analysis same as case 2

$V_{out} = 1.1V$

Case 4: $V_1 = 5V$, $V_2 = 5V$

D1 → RB D2 → RB



$\therefore V_{out} = 5\ V$

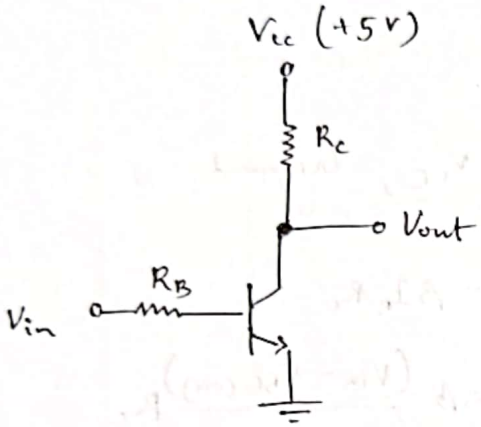
→ Using DL, it is not possible to implement NOT gate

→ Not used in integrated circuits.

Resistor - Transistor Logic (RTL)

↳ logic gates are implemented using combination of resistors & transistors

NOT gate (inverter):



Let,

$R_B = 10\,k\Omega$

$R_c = 1\,k\Omega$

$\beta = 50$

$V_{BE(ON)} = V_{BE(sat)} = 0.7V$

$V_{CE(sat)} = 0.2V$

Cut-off region

When, $V_{in} = 0V$ (Low)

Transistor is off

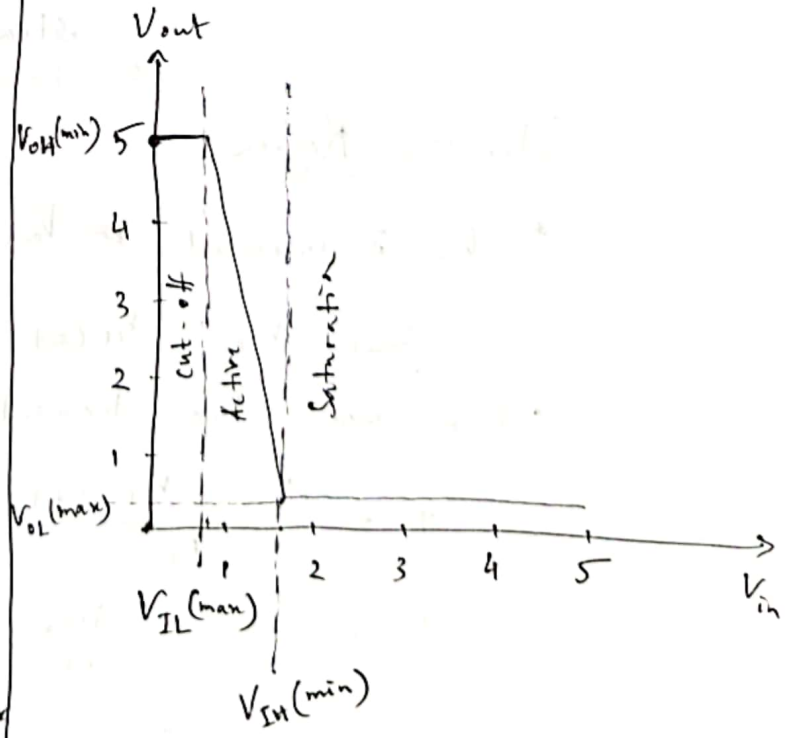
$I_c = 0$

$V_{out} = V_{cc} - I_c R_c$

$= V_{cc} = 5V$ (High)

V_{out} remains High until the BE junction becomes sufficiently forward biased. Which is $V_{BE} < 0.7V$

Input - Output Characteristics



Active Region (when V_{in} is increased beyond 0.7 V, I_B starts to flow, Transistor goes to active region)

Applying KVL along V_{in}, R_B, V_{BE}, Ground

$$I_B = \frac{(V_{in} - V_{BE(on)})}{R_B}$$

In active region, $I_c = \beta I_B$

Applying KVL along V_{cc}, R_c, V_{CE}, Ground

$$V_{CE} = V_{out} = V_{cc} - I_c R_c = V_{cc} - \beta I_B R_c$$

$$= V_{cc} - \beta \frac{(V_{in} - V_{BE(on)})}{R_B} R_c$$

$$= V_{cc} - \frac{\beta R_c}{R_B}(V_{in} - V_{BE(on)})$$

↓

straight line with negative slope

Saturation Region

As V_{in} is increased ~~V_{out} starts~~ continues, V_{out} to decrease until

$$V_{out} = V_{CE} = V_{CE(sat)}$$

which means the transistor enters saturation region

$$I_c = \frac{V_{cc} - V_{CE(sat)}}{R_c} = \frac{(5 - 0.2)}{1k} = 4.8\ mA$$

$$I_B = \frac{I_c}{\beta} = \frac{4.8m}{50} = 0.096\ mA$$

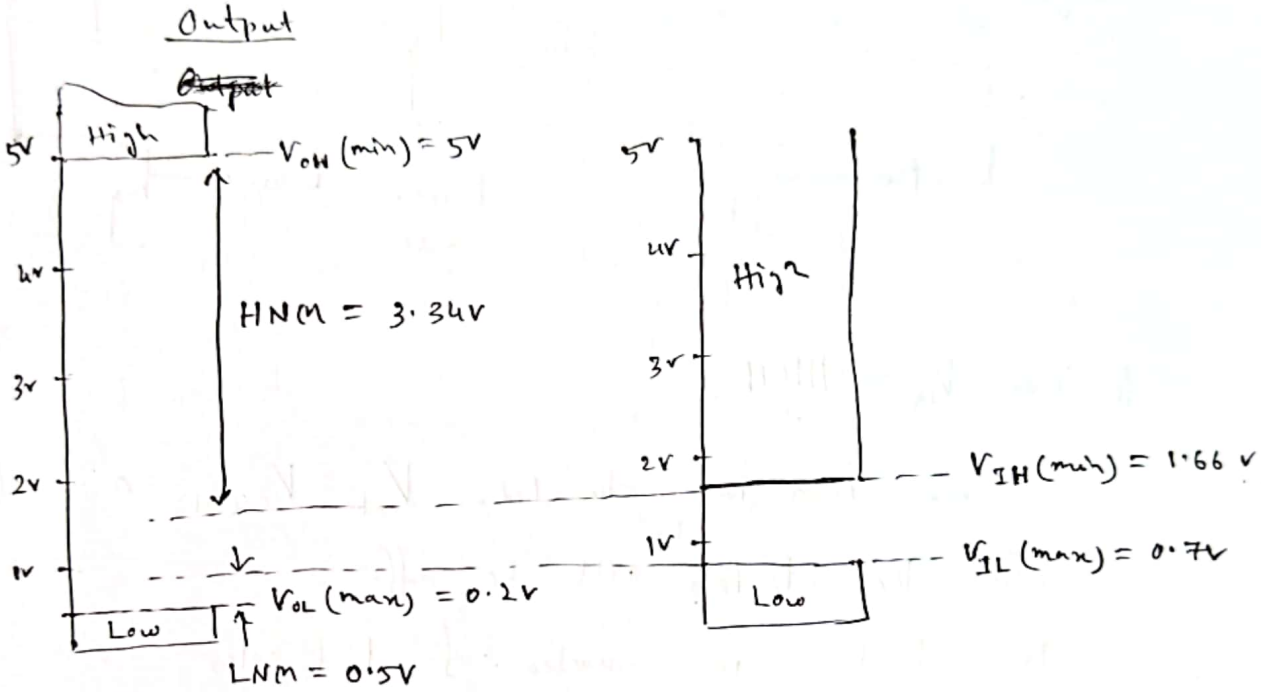
$$V_{in} = V_{BE(on)} + I_B R_B = 0.7 + (0.096m)(10k) = 1.66\ V$$

Thus, when, $V_{in} \geq 1.66\ V$ → Transistor saturates

Noise Margin

$V_{IL}(max) = 0.7V$ $V_{IH}(min) = 1.66V$

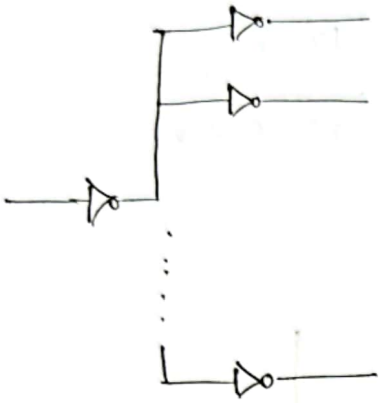
$V_{OH}(min) = 5V$ $V_{OL}(max) = 0.2V$

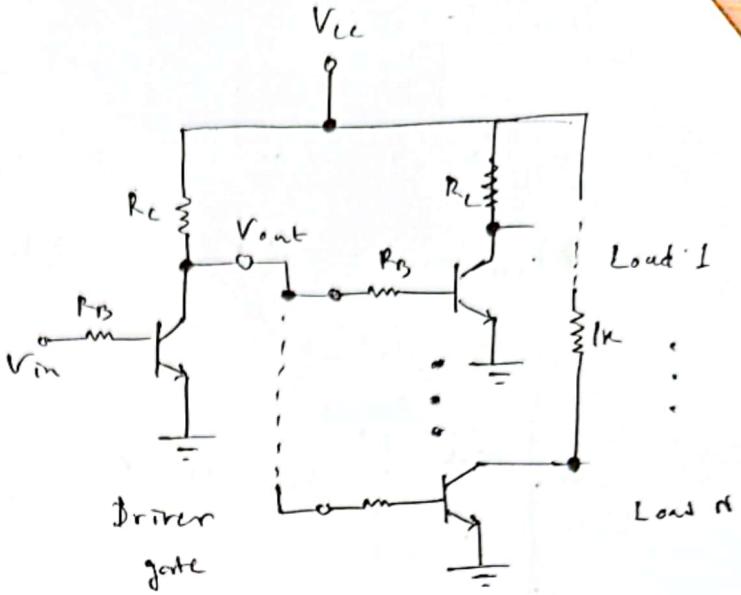


$HNM = V_{OH}(min) - V_{IH}(min) = 5 - 1.66 = 3.34\ V$

$LNM = V_{IL}(max) - V_{OL}(max) = 0.7 - 0.2 = 0.5\ V$

Fanout





* When V_{in} → HIGH

Driver Transistor Saturated. $V_{out} = V_{CE(sat)} = 0.2V$ (Low)

All the load gates will be off

No restriction in number of load gates

\# When, V_{in} → LOW

Driver Transistor Cut-off.

V_{out} → high

↳ will serve as input to the load gates

Now, $V_{IH}(min) = 1.66\,V$ → minimum input voltage in the load gates to recognize a logic HIGH state

for Driver,

$$I_{C(driver)} = \frac{(V_{cc} - V_{out})}{R_c} = \frac{5 - 1.66}{1K}$$

$$= 3.34\,mA$$

for load,

$$I_{B(load)} = \frac{V_{out} - V_{BE(sat)}}{R_B}$$

$$= \frac{1.66 - 0.7}{10k} = 0.096\ mA$$

$$N = \frac{I_{C(driver)}}{I_{B(load)}} = 34.79 \approx 34$$

Effect of noise margin

for a 0.5V noise margin

Minimum HIGH Level voltage at V_{out}

$$V_{OH(min)} = V_{IH(min)} + NM$$

$$= 1.66 + 0.5 = 2.16\ V$$

Critical $V_{out} = 2.16\ V$,

$$I_{C(driver)} = \frac{V_{CC} - V_{out}}{R_C} = \frac{5 - 2.16}{1k} = 2.84\ mA$$

$$I_{B(load)} = \frac{V_{out} - V_{BE(sat)}}{R_B} = \frac{2.16 - 0.7}{10k} = 0.15\ mA$$

$$N = \frac{I_{C(driver)}}{I_{B(load)}} = 19.4 \approx 19$$