# Transistor – Transistor Logic (TTL)

→ Usefulness of DTL gates are limited by their speed of operation. This limitation is overcome in TTL gates.

## Limitation associated with DTL gates:

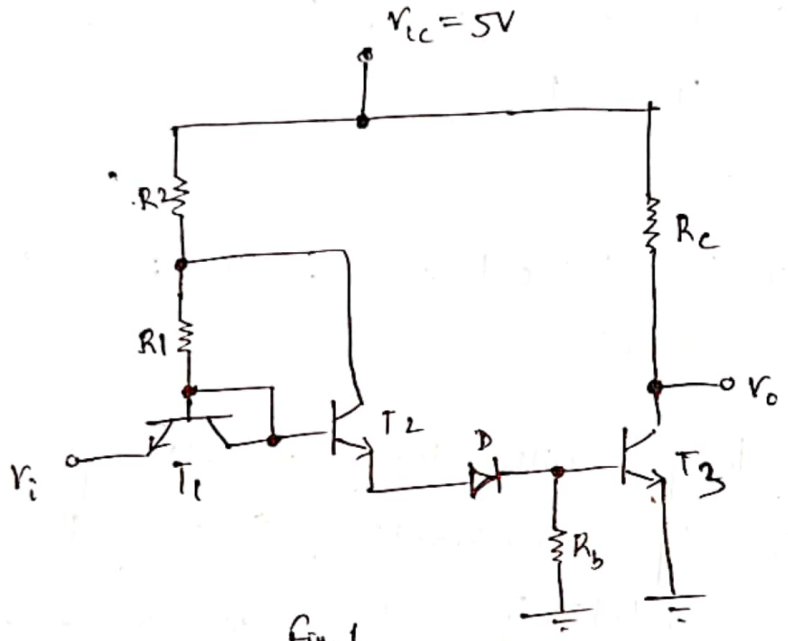



fig. 1

$T_1$ → input transistor which works as a diode in this circuit as collector & base are shorted. Input diode is replaced by a "diode connected transistor"

$T_3$ → output transistor

When, $V_i = 1$

→ B to E junction of $T_1$ reverse biased

→ Current flows through $T_2$, D to the base of $T_3$

→ $T_3$ saturated. Thus, $V_o = V_{CE(sat, T_3)} = 0.2\,V$ (Low)
At saturation, $V_{BE(sat, T_3)} = 0.75\,V$

When, $V_i = 0$

→ B to E junction of $T_1$ forward biased. Current from $V_{cc}$ mainly flows through $T_1$

→ $T_2$, D are cut-off

→ Thus, $T_3$ should be cut-off. So, $T_3$ will have a transition from saturation to cut-off

$T_3$ will not reach cut-off until it's base charge is removed

This base charge will leak off through $R_b$ or dissipate by recombination. This discharging process is relatively slow which gives rise to the speed limitation of DTL gates

→ After discharging, when $T_3$ is cut-off;

$V_o = V_{cc} = 5V$ (High)

# Basic TTL gate:

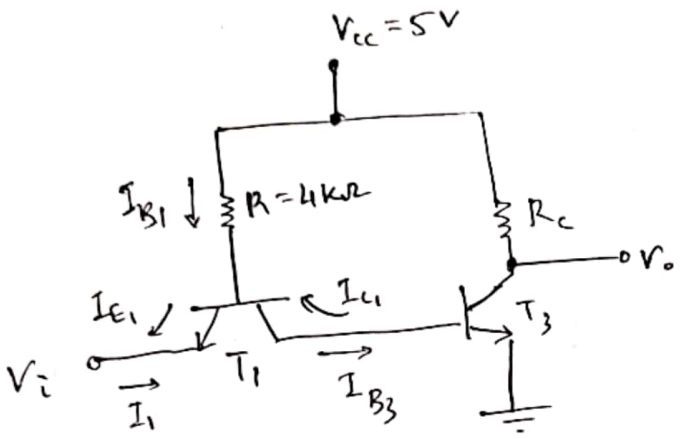



fig.2

Here,
$T_1$ is connected as a transistor as connection between B & C is not there like the previous DTL circuit

When, $V_i \rightarrow$ HIGH

→ B-E junction of $T_1$ is reverse biased
B-C junction of $T_1$ is forward biased.

Thus, $T_1$ will operate in inverse mode or reverse active mode

→ Current will flow from $V_{cc} \rightarrow R \rightarrow$ (BC junction of $T_1$) → (base of $T_3$)

$T_3$ will be saturated

$$V_{o} = V_{CE(sat, T_3)} = 0.2\,V \quad \text{(LOW)}$$

$$V_{BE(sat, T_3)} = 0.75\,V$$

When, $V_i \rightarrow$ LOW

→ B-E junction will be forward biased

B-C junction will momentarily be reverse biased

$T_1$ will operate in active mode

→ Base of $T_3$ will discharge through $T_1$

→ After discharging $T_3$ will cut-off.

Thus,

$$V_o = V_{cc} = 5V \quad (HIGH)$$

→ Discharging process through a transistor takes place much faster compared to discharging through resistor

Thus, TTL gates operate faster compared to DTL gates

# A Comparison between TTL & DTL :

→ In fig. 1, when $T_3$ is saturated,

$$V_{BE(sat, T_3)} = 0.75V$$

When, $V_i$ is Low and $T_2$ & D is cut-off, base of $T_3$ will discharge through $R_b$

While discharging, initial current out of the base of $T_3$ = $\frac{V_{BE(sat, T_3)}}{R_3} = \frac{0.75}{2K}$

$\approx 0.38$ mA

→ In fig. 2, when $V_i$ is High, $T_3$ will be Saturated

$$V_{BE(Sat, T_3)} = 0.75V$$

$$\therefore V_{CE(T_1)} = 0.75V$$

~~$T_1$ operates in active mode~~

when, $V_i$ is grounded,

B-E junction of $T_1$ will be forward biased

As base of $T_3$ will not discharge instantaneously, $T_1$ will initially operate in active mode as $V_{CE(T_1)} = 0.75V$

Base current of $T_1$, $I_{B_1} = \dfrac{V_{cc} - V_{BE}(T_1)}{R}$

$= \dfrac{5 - 0.75}{4k}$

$\simeq 1.1\ mA$

When $T_3$ starts discharging, the initial collector current of $T_1$, $I_{C_1} = \beta I_{B_1}$

$= 20 * (1.1m)$ [if $\beta = 20$]

$= 22\ mA$

As collector of $T_1$ is connected with base of $T_3$, during the discharge of stored charge at base of $T_3$, $I_{C_1}$ amount of current can be drawn from the base of $T_3$.

→ As the amount of current that can be drawn from base of $T_3$ is much higher then DTL, the TTL gates can result in faster removal of ~~stored~~ stored charge

# Input transistor

In fig. 2, when $V_i$ is HIGH

$T_1 \rightarrow$ operates in inverse active region

$T_3 \rightarrow$ operates in saturation

Let,

the common-base current gain in the inverse active mode of $T_1$ is $\alpha_I$

From fig.2, Input current, $I_1 = \alpha_I I_{B3}$

$$I_{B3} = I_{B1} + I_1 = I_{B1} + \alpha_I I_{B3}$$

$$\Rightarrow I_{B1} = (1 - \alpha_I) I_{B3}$$

In TTL gate, if input transistor is designed to have a very low $\alpha_I$ (i.e: $\alpha_I = 0.02$); then majority of the base current of $T_3$ need to be supplied through R from $V_{cc}$

for $\alpha_I = 0.02$ $\longrightarrow$ 2% current comes from input source

$\hookrightarrow$ 98% " " " $V_{cc}$ through R

Thus, low value of $\alpha_I$ provide the advantage of minimizing the loading on a driving source.

→ To construct multi-input TTL gate, multiple transistors can be connected in parallel at the input side with Collector & Base terminal of each transistor shorted and providing input signals through the emitter

Instead of connecting multiple transistors in parallel, "Multi-emitter Transistor" is used with a single common collector & single common base.

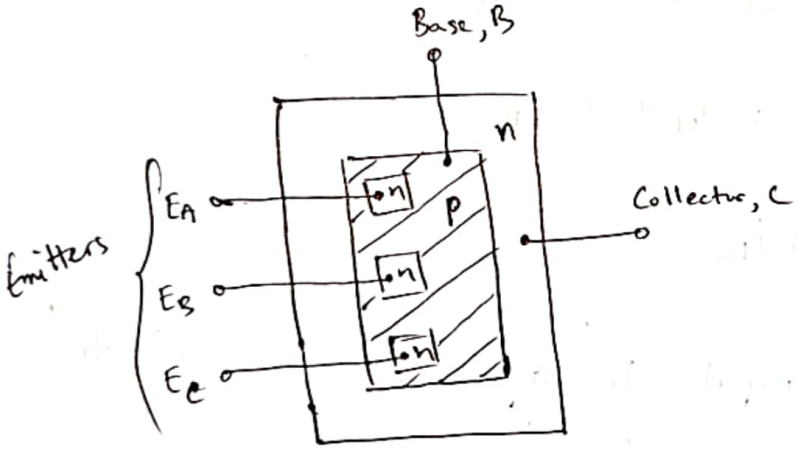



fig3: Physical structure of multi-emitter transistor

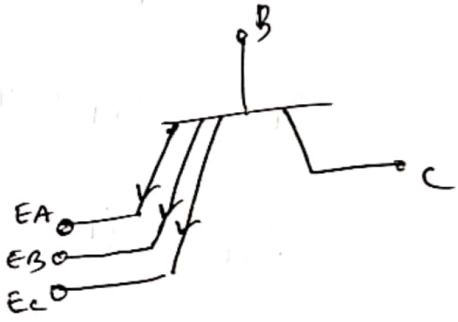



fig4: Circuit symbol of multi-emitter transistor

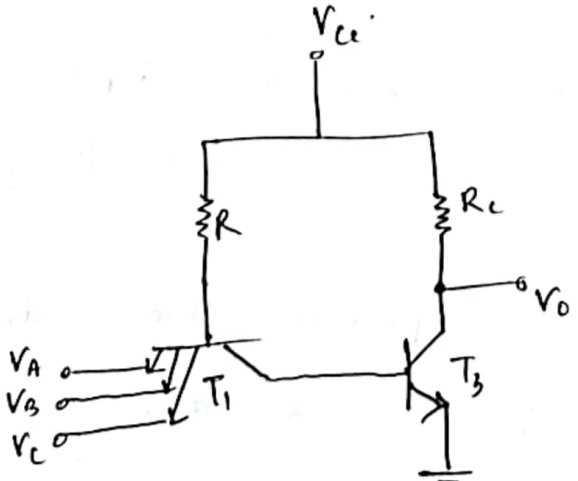


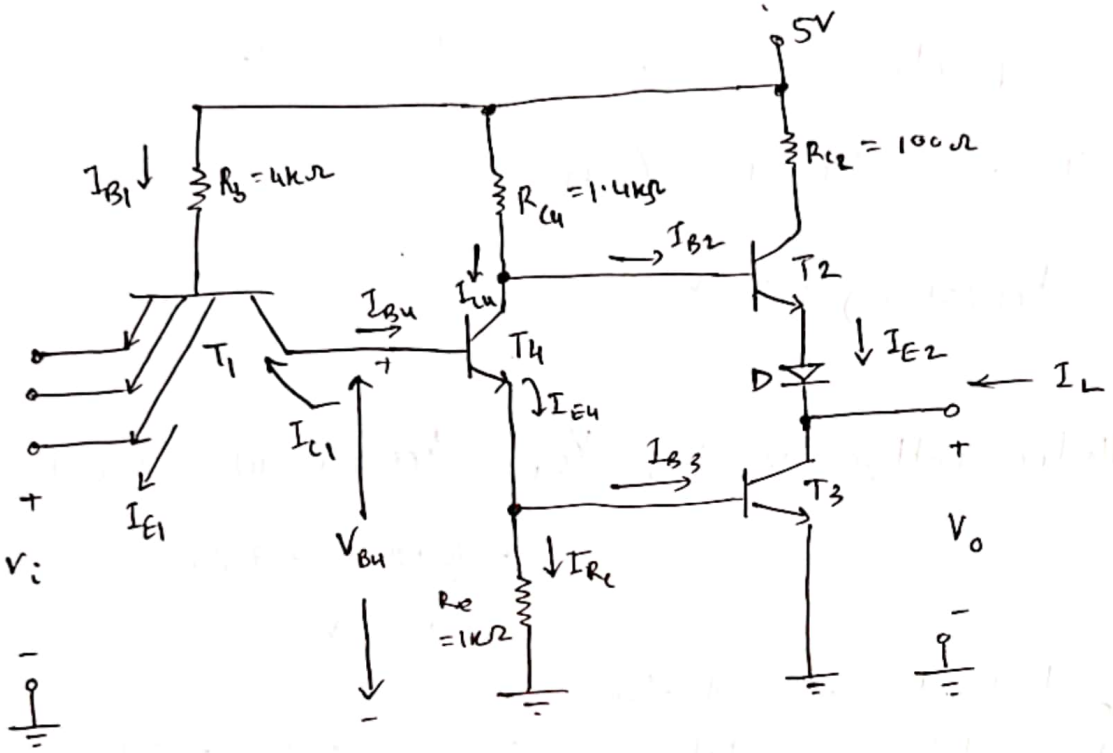

fig5: 3-input basic TTL NAND Gate

In Fig. 5;

→ If any one i/p is '0'
- $T_1$ → saturated
- $T_3$ → cut-off
- $V_0$ → HIGH '1'

→ If all inputs are at '1'
- $T_1$ → reverse active
- $T_3$ → saturated
- $V_0$ → Low '0'

# TTL NAND Gate with Active Pull-up




$V_o \rightarrow$ Low

$T_3 \rightarrow$ saturated

$T_2 \rightarrow$ cut-off

$V_o \rightarrow$ High

$T_3 \rightarrow$ cut-off

$T_2 \rightarrow$ saturated

$T_2 - T_3 \rightarrow$ Totem-pole pair

↳ When one transistor is ON, the other transistor will be OFF

$T_4 \rightarrow$ phase splitter

↳ Alternate switching of $T_2$ & $T_3$ is done through $T_4$

When, all i/p of $T_1$ is HIGH

$T_1 \rightarrow$ operates in reverse active mode

$T_4, T_3 \rightarrow$ Saturation (ON)

$V_o = V_{CE(Sat, T_3)} \approx 0.2V$

Collector voltage of $T_4$, $V_{C4} = V_{CE(Sat, T_4)} + V_{BE(Sat, T_3)}$

$= (0.2 + 0.75)V$

$= 0.95V$

If diode D is not there,
Voltage difference between base and emitter of $T_2$, $V_{BE}(T_2) = V_{C4} - V_{C3}$

$= (0.95 - 0.2)V$

$= 0.75V$

As $V_{BE}(T_2) > V_{BE(cut-in)} = 0.65V$

$T_2$ will start conducting if diode D is not present

If diode D is present, the voltage difference of $V_{C4}$ & $V_{C3}$ will not be sufficient to make the B-E junction of $T_2$ and diode D forward biased.

# Input - Output Characteristics

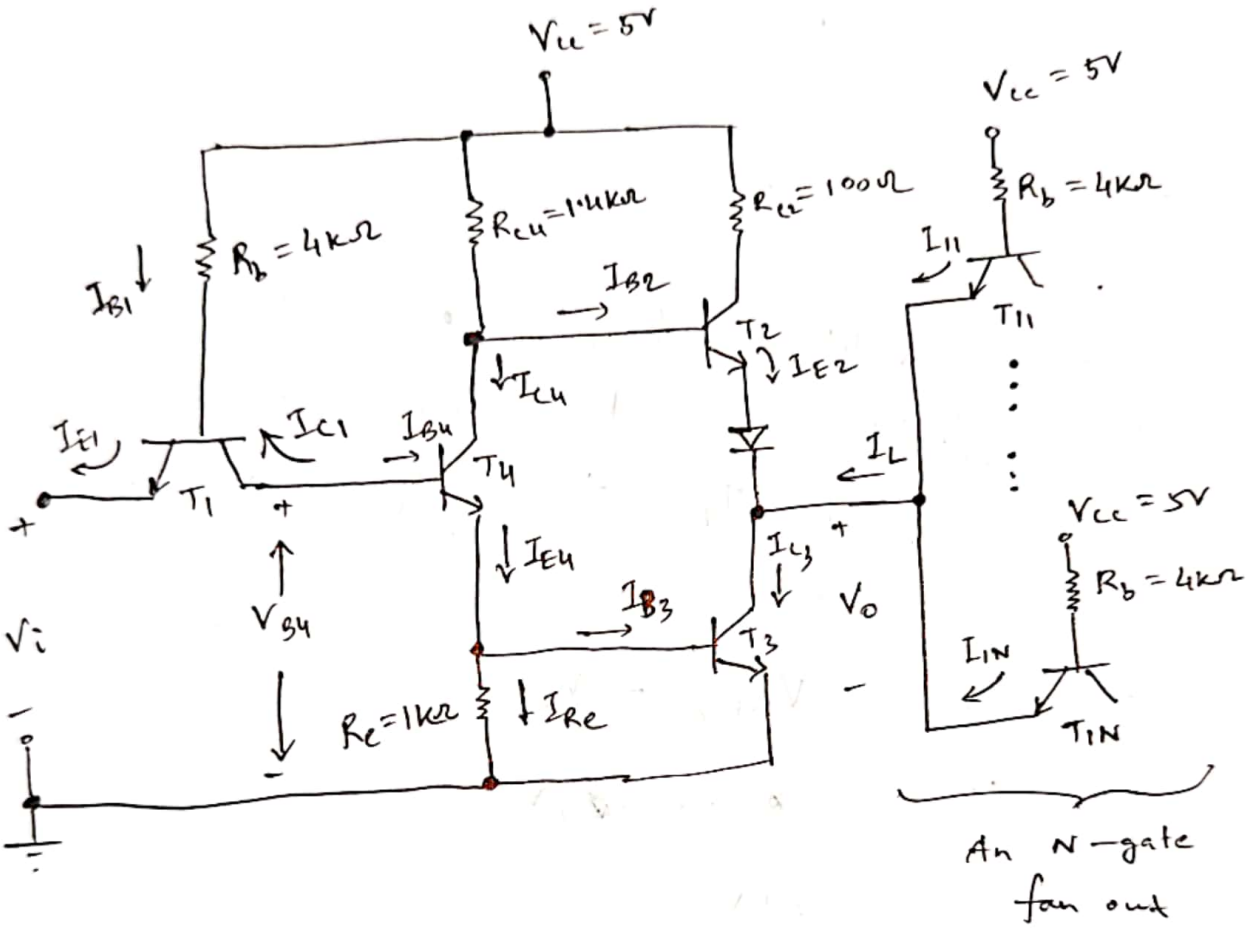



fig: A loaded TTL gate

$V_i \rightarrow$ Low (0 V)

$T_1 \rightarrow$ in saturation

Let, $V_{CE(sat, T_1)} = 0.1\ V$

$V_{B4} = V_i + V_{CE(sat, T_1)}$

$= 0 + 0.1\ V$

$= 0.1\ V$

$T_4, T_3 \rightarrow$ Cut-off

$T_2 \rightarrow$ Active mode

$I_{E2} \rightarrow$ Emitter current of $T_2$

↳ will provide current supply to N other similar gates

$I_{E2} = -I_L$

$$V_0 = V_{CC} - I_{B2} R_{C4} - V_{BE2} - V_D$$

$$= V_{CC} - \frac{I_{E2}}{(\beta+1)} R_{C4} - V_{BE2} - V_D$$

$$= V_{CC} + \frac{R_{C4} I_L}{(\beta+1)} - V_{BE2} - V_D$$

Considering voltage drop across $R_{C4}$ to be negligible due to small amount of load current $I_L$ the output voltage will be,

$$V_o = V_{CC} - V_{BE2} - V_D$$

$$= (5 - 0.7 - 0.7)\,V$$

$$= 3.6\,V$$

As $V_i$ is gradually increased at some point $V_{B4}$ will be equal to the cut-in voltage of $T_4$ $\left[V_{BE(cut-in)} = 0.65\,V\right]$

When, $V_{B4} = 0.65\,V$

$$V_i = V_{B4} - V_{CE(Sat, T_1)}$$

$$= (0.65 - 0.1)\,V = 0.55\,V$$

When, $V_i \geq 0.55\,V$

$T_4 \rightarrow$ will enter the active region

$T_3 \rightarrow$ will remain cut-off

→ As $V_i$ is increased further,

In active mode of operation $V_{BE4} = 0.7V$

$T_3$ will enter ~~saturation~~ active region when $V_{BE3} \geq 0.65V$

When, $T_3$ just enters active mode,

$$V_{B4} = V_{BE4} + V_{BE3}$$

$$= (0.7 + 0.65)V$$

$$= 1.35V$$

$$V_i = V_{B4} - V_{CE(sat),T_1} = (1.35 - 0.1)V$$

$$= 1.25V$$

As $T_4$ & $T_3$ both are in active mode, voltage drop across $R_{C4}$ will not be negligible

$$I_{Re} = \frac{0.65}{1K} = 0.65mA$$

$$I_{Re} \approx I_{E4} \approx I_{C4}$$

Voltage drop across $R_{C4} = (1.4K) * (0.65m)$

$$= 0.9V$$

$$V_o = (3.6V - 0.9V) = 2.7V$$

→ As $V_i$ increased further,

$T_3$, $T_4$ → Saturation

$T_2$ → Cut-off

$$V_{B4} = V_{BE(Sat, T_4)} + V_{BE(Sat, T_3)}$$

$$= (0.75 + 0.75)V$$

$$= 1.5V$$

$$V_i = V_{B4} - V_{CE(Sat, T_1)}$$

$$= (1.5 - 0.1)V$$

$$= 1.4\ V$$

$$V_o = V_{CE(Sat, T_3)}$$

$$= 0.1\ V$$