NOR gate using Resistor – Transistor Logic (RTL)

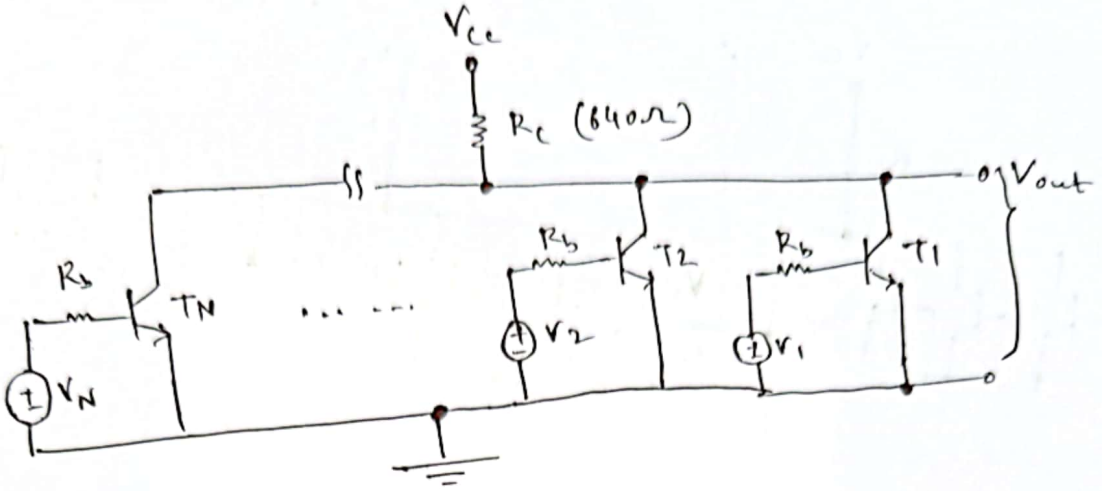

Fig: An N-input RTL NOR gate

→ For N input NOR gate N number of transistors ($T_1, T_2, \ldots T_N$) are required

→ Emitters of ~~each~~ all transistors are connected to a common ground

→ Collectors are connected to supply voltage (V_{cc}) through a common collector resistor (R_c).

→ V_i ($i = 1, 2, \ldots N$) represent the input logic level applied to the bases of the transistors through resistors R_b.

$$V_i = \begin{cases} V_L ; & \text{Logic Low} \\ V_H ; & \text{Logic High} \end{cases}$$

V_L → should be low enough for the corresponding transistor to be in cut-off

V_H → should be high enough to ~~make~~ drive the corresponding transistor to saturation

NOR gate using RTL

Let, $R_c = 640\,\Omega$

$R_b = 450\,\Omega$

$V_{cc} = 3V$

$V_{BE(cut-in)} = 0.65V$

$V_{BE(sat)} = 0.75V$

$V_{CE(sat)} = 0.2V$

$\beta = 50$

$\sigma = 0.85$

$\sigma = \frac{I_c}{\beta I_B}$

Apart from input to T_1, all other input signals are at voltages which ensure that the corresponding transistor is cut-off

Input - output characteristics will be drawn w.r.t. V_o & input to T_1 (V_i)

→ V_i → Low

$V_i < 0.65V$

∴ T_1 cut-off

∴ $V_o = V_{cc} = 3V$ (HIGH)

→ When, $V_i > 0.65V$ → T_1 will enter active region

→ As V_i is increased further at some point V_i will be sufficient to take T_1 to saturation.

→ After attaining saturation,

$V_o = V_{CE(sat)} = 0.2V$

$\therefore I_c = \frac{V_{cc} - V_{CE(sat)}}{R_c} = \frac{3 - 0.2}{640} = 4.4mA$

$\therefore I_B = \frac{I_c}{\beta\sigma} = \frac{4.4m}{(50)(0.85)} \approx 0.1mA$

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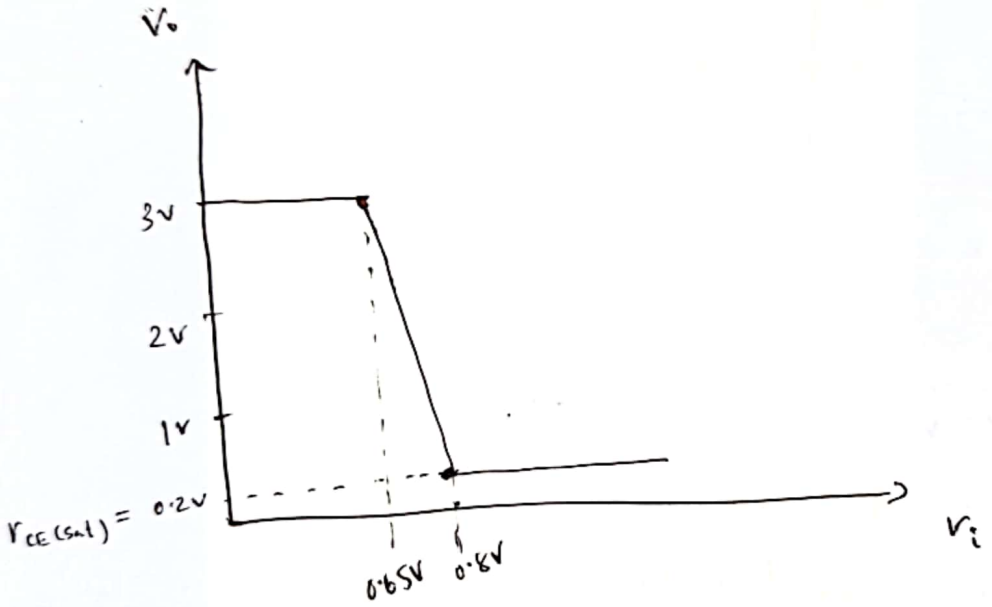
Applying KVL at the i/p side of T_1,

$$V_i = I_B R_b + V_{BE(sat)}$$
$$= (0.1m)(450) + 0.75$$
$$\approx 0.8\ V$$

Thus, when $V_i \geq 0.8V$, T_1 will saturate



$V_{IL}(max) = 0.65\ V$ $\quad$ $V_{IH}(min) = 0.8\ V$

$V_{OL}(max) = 0.2\ V$ $\quad$ $V_{OH}(min) = 3\ V$

The Direct Coupled Transistor - Logic (DCTL) gate

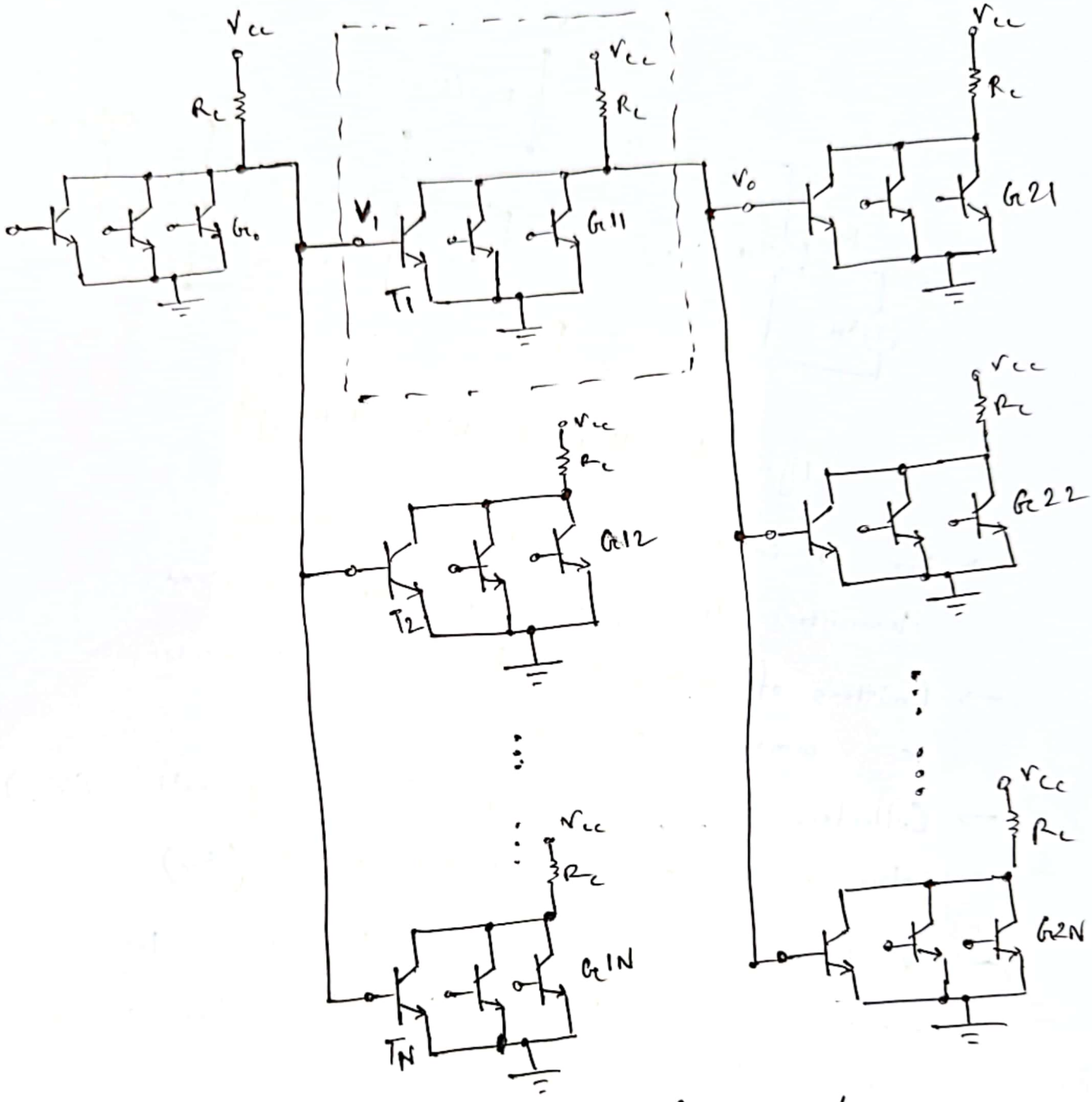


fig: DCTL NOR gate with fan-out of N

→ economically constructed by omitting the base resistors R_b used in RTL gates

→ NOR, NAND referred to as universal gates

In a sophisticated switching system, each of the inputs to the NOR gate can be derived from the outputs of other similar NOR gates

→ Let us assume,
fan-out of G0 is N.
So, output of gate G0 will be providing a signal to one input of N other gates G11, G12, ... G1N

→ Similarly, fan-out of gate G11 is N
So, output of gate G11 will provide a signal to one input of N other gates G21, G22, ... G2N

→ Other input terminal will get signal from other sources

→ If all inputs to gate G0 is LOW, then the output of G0 is supposed to be HIGH that is supposed to drive $T_1, T_2, \ldots \ldots T_N$ to saturation

Let, $V_{BE(sat)} = V_0 = 0.75\,V$

$\therefore V_i = 0.75\,V$ [As output voltage at G0 is 0.75V]

→ Current through $R_c = \dfrac{V_{cc} - V_0}{R_c} = \dfrac{V_{cc} - 0.75}{R_c}$

↳ This is the total current supplied from V_{cc} to drive $T_1, T_2, \ldots \ldots T_N$ to saturation

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→ Each base current at $T_1, T_2, \ldots \ldots T_N$:

$$I_B = \frac{(V_{cc} - 0.75)}{N R_c}$$

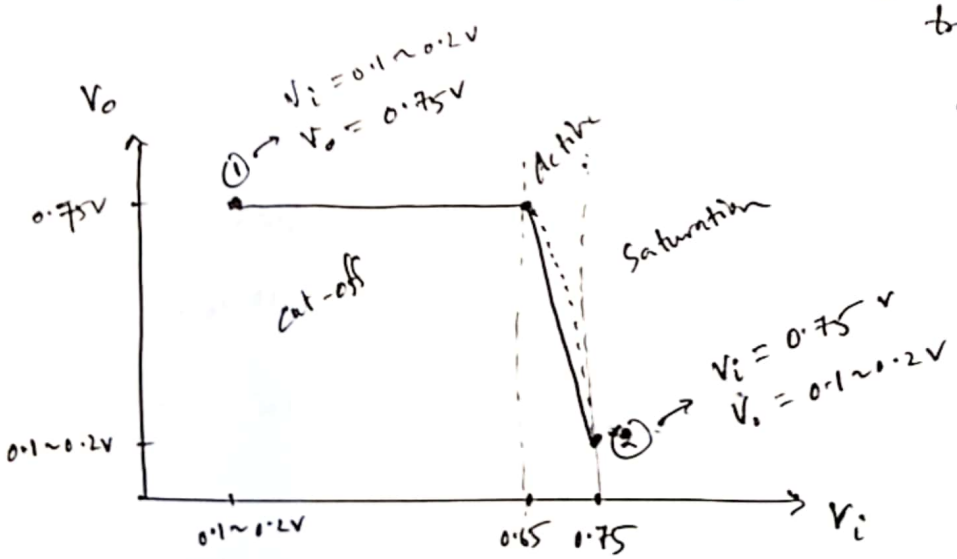
→ for G11,

$V_i = 0.75\ V$ (HIGH)

$V_o = V_{CE} = V_{CE}(sat) = 0.1 \sim 0.2\ V$ (LOW)

Input - Output Characteristics of DCTL

Plotting V_o of gate G11 as a function of input voltage V_i applied to one of the transistors in the gate. [assuming other transistors in the gate are cut-off]



Cut-in voltage = 0.65 V

$0.65\ V < V_i < 0.75\ V$ → Transistor in Active mode

In active region, $I_c \approx I_E$

I_E related to base-emitter voltage by diode eqn

$$I_c \approx I_E \approx I_{E_0} e^{V_{BE}/V_T}$$

$$\approx I_{E_0} e^{V_i/V_T}$$

$$\boxed{V_T = \frac{KT}{q}}$$

$$V_o = V_{cc} - R_c I_c = V_{cc} - R_c I_{E_0} e^{V_i/V_T}$$

Current Hogging in DCTL gates

→ Transistors of similar manufacture are generally quite similar in performance, but not precisely identical

→ When output of G_{10} is at logic '1', $T_1, T_2, \ldots \ldots T_N$ are supposed to be driven to saturation

Let,

at saturation V_{BE} of T_1 is 0.74 V ;

V_{BE} of T_2 is 0.76 V

V_{BE} of T_N is 0.75 V

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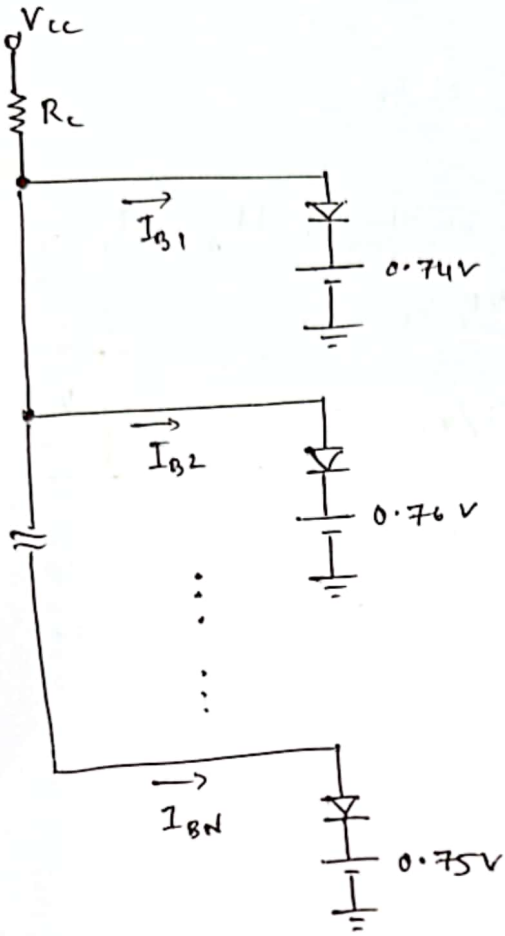

Base - emitter equivalent circuit of T1

$$I_{B1} = \frac{V_{cc} - 0.74}{R_c}$$

Base - emitter equivalent circuit of T2

$$I_{B2} = \frac{V_{cc} - 0.76}{R_c} \qquad I_{B2} << I_{B1}$$

Base - emitter equivalent circuit of T_N

$$I_{BN} = \frac{V_{cc} - 0.75}{R_c} \qquad I_{BN} << I_{B1}$$

Fig: Equivalent Circuit to illustrate current hogging in DCTL

→ According to this figure, T_1 will draw (hog) more current from V_{cc} through R_c as its required V_{SE} (0.74V) ~~is less than~~ to reach saturation is less than other transistors.

→ Thus, other transistors might starve for sufficient base current to attain saturation. This phonomenon is known as current hogging

→ Due to current hogging, DCTL gates are not commonly used

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Diode Transistor Logic (DTL) Gate

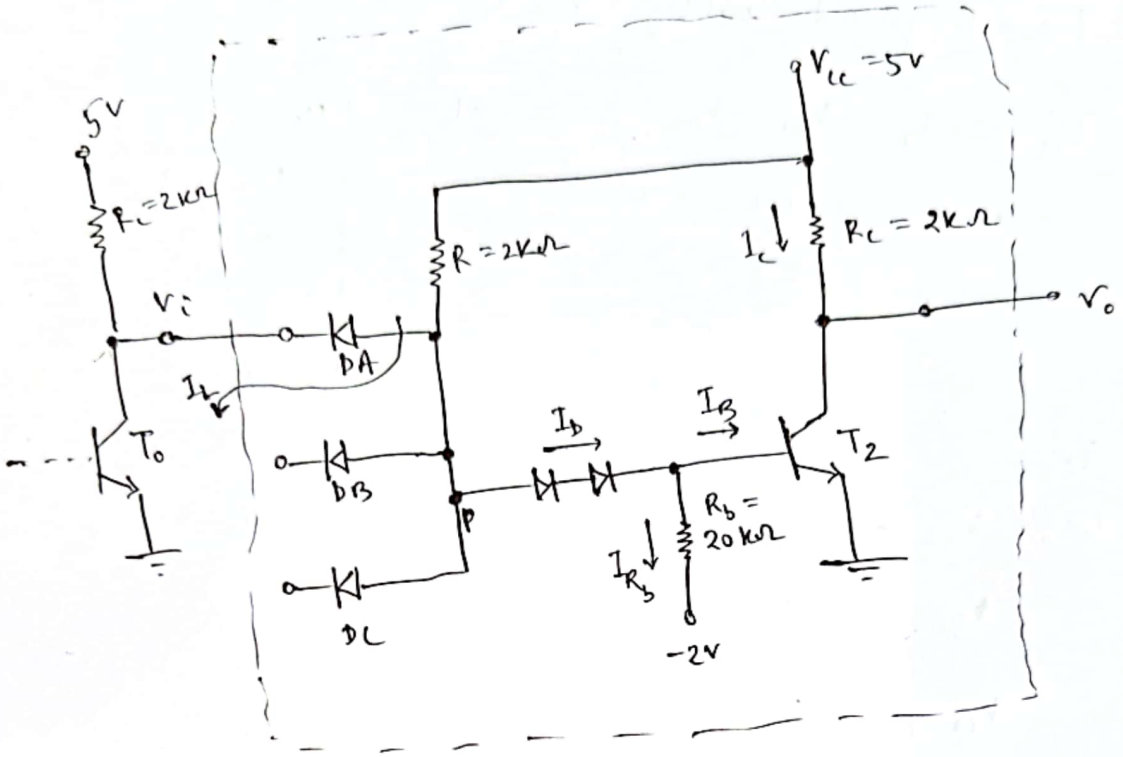

Fig: NAND Gate using DTL

Here;

T_0 → output transistor of driving gate

→ output from T_0 is serving as input along D_A

Case 1:

Let,

T_0 is at logic level '0'

T_0 is in saturation

Thus, $V_i = V_{CE(sat)T_0} = 0.2\,V$ [LOW]

Voltage at point P,

$V_p = V_{CE(sat, T_0)} + V_{DA}$

$= 0.2 + 0.75$

$= 0.95\,V$

It is considered that current in DA is sufficient to produce a voltage drop of 0.75 V

The base-to-ground voltage of T_2 is;

$$V_{BE} = V_p - V_{D1} - V_{D2}$$
$$= 0.95 - 0.65 - 0.65$$
$$= -0.35\ V$$

Here,
$V_{D1} = V_{D2} = 0.65\ V$
↳ it is assumed that current in D1 & D2 is very small

for T_2,

let, $V_{BE(cut-in)} = 0.65V$

$V_{BE(sat)} = 0.75V$

$V_{CE(sat)} = 0.2V$

$\because V_{BE} < V_{BE(cut-in)} = 0.65V$

$\therefore T_2$ is cut-off

Diode current I_D flows through R_b only.

$$I_{R_b} = I_D = \frac{V_{BE} + 2}{R_b} = \frac{-0.35 + 2}{20K} = 0.08\ mA$$

At this stage,

~~$V_0 = V_{CE(sat), T_2}$~~

$$V_0 = V_{cc} = 5\ V \quad (HIGH)$$

Similarly, when all inputs are at logic level '0', V_0 remains at logic level '1'.

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Case 2:

Let,

all inputs are at logic level '1' ($V_{High} = 5V$)

→ DA, DB, DC will be disconnected from circuit

→ Current will flow from V_{cc} through R, then through D_1, D_2 and into the base of T_2

→ Here, T_2 will be saturated &

$$V_{BE} = V_{BE(Sat, T_2)} = 0.75V$$

→ Current through R_3

$$I_{R_3} \approx \frac{V_{BE} + 2}{20K} \approx \frac{0.75 + 2}{20k} \approx 0.14\,mA$$

→ Voltage at point P;

$$V_p = V_{D1} + V_{D2} + V_{BE}$$
$$= 0.75 + 0.75 + 0.75$$
$$= 2.25\,V$$

It is assumed that current in D_1 & D_2 is sufficiently large to result in a voltage drop of 0.75V accross the diodes

→ Diode current I_D,

$$I_D = I_R = \frac{V_{cc} - V_p}{R} = \frac{5 - 2.25}{2K}$$

$$\approx 1.4\,mA$$

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→ Base current of T_2,

$$I_B = I_b - I_{R_b} = 1.4\,mA - 0.14\,mA$$

$$\simeq 1.26\,mA$$

→ The collector current of T_2,

$$I_c = \frac{V_{cc} - V_{CE(sat,T_2)}}{R_c} = \frac{5 - 0.2}{2K}$$

$$= 2.4\,mA$$

Choice of R_b & V_{BB}

↳ Value of R_b & V_{BB} needs to be chosen keeping a trade-off into consideration

Let, all inputs of the gate are HIGH &

T_2 is saturated.

If any one of the i/p to the gate becomes LOW, then V_p will fall to 0.95V. However, $V_{BE(sat,T_2)}$ will not drop from 0.75V instantly.

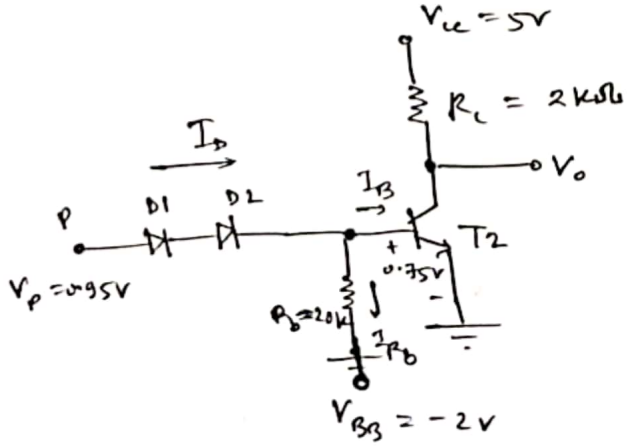

Fig: Equivalent Circuit of the DTL NAND gate at the instant that V_p is decreased to 0.95 V

→ Voltage drop across D1 & D2 is (0.95 − 0.75) = 0.2V which is not sufficient to forward bias D1 & D2

Thus, $I_D = 0 \rightarrow I_B = 0$

→ $V_{BE(Sat, T_2)} = 0.75V$ doesn't drop to '0' instantly as there is charge storage mechanism in the transistor

This stored charge leaves through R_b

Thus, V_{BB} is set to −2V to increase the rate of discharge

A trade-off need to be considered between these two points while choosing the values of R_b & V_{BB}

→ To quickly cut-off T_2, R_b should be small & V_{BB} should be very negative

→ When it is necessary to turn on T_2 again, it is required that majority of the current flows through base of T_2. Thus, R_b should be large & V_{BB} should be positive so that less current flows through R_b and majority of the current flows through base of T_2.

→ Typical values of R_b → 5 to 30 kΩ

V_{BB} → 0 to −5V

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Fan-Out

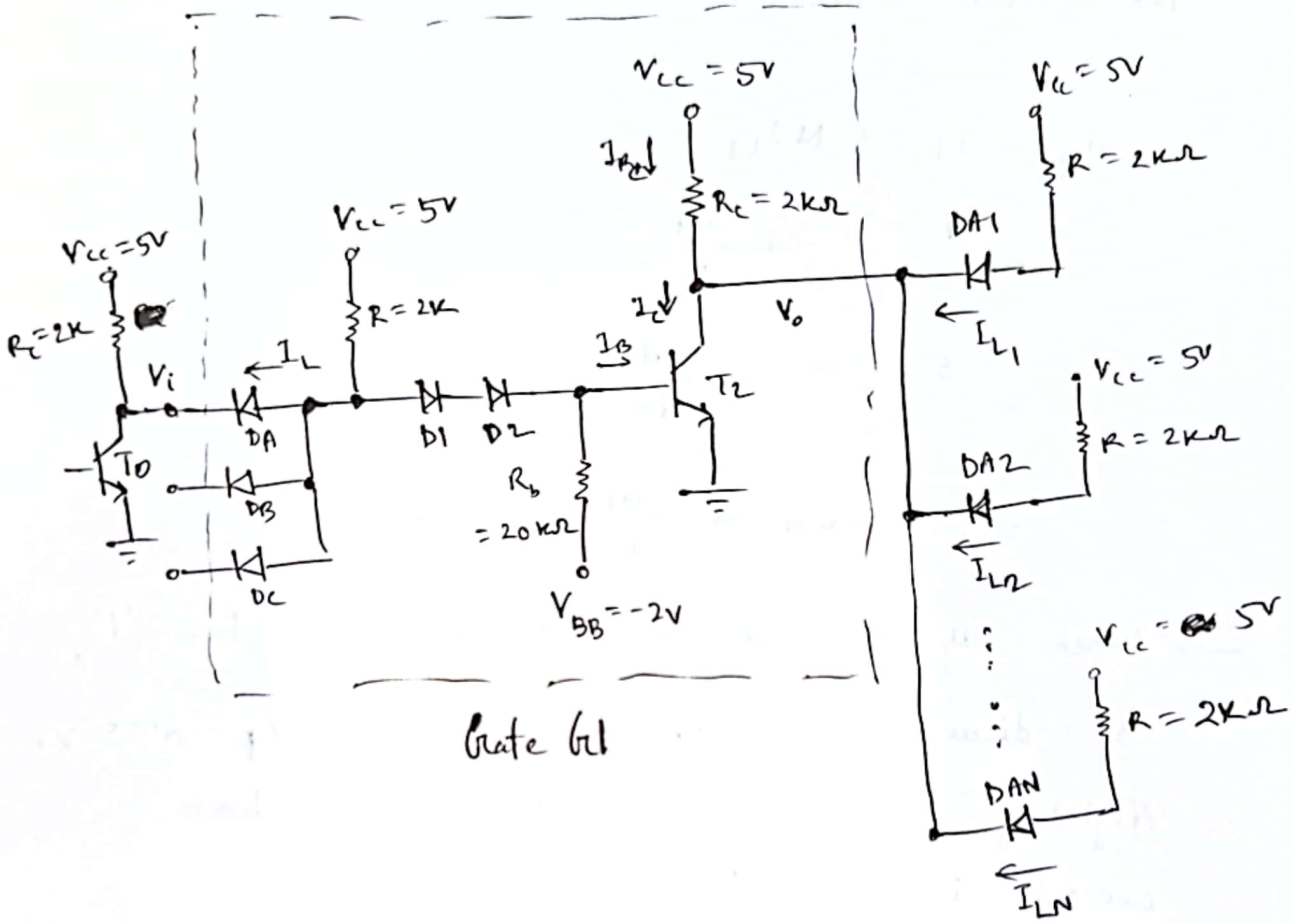

fig: A DTL Gate with Fan-Out

→ Gate G1 is doiving N other similar gates

→ Let, all inputs of gate G1 are at logic '1' (High)

Thus, T_2 is saturated

$$V_o = V_{CE(Sat, T_2)} = 0.2V$$

→ Current through each of the N loading gates

$$I_{L_1} = I_{L_2} = \dots\dots = I_{LN} \approx \frac{V_{cc} - V_{DA1} - V_D}{R} \approx \frac{5 - 0.75 - 0.2}{R}$$

$$\approx \frac{4}{R}$$

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→ The total collector current in T2 is

$$I_C = I_{R_c} + N I_{L1}$$

$$= \frac{V_{cc} - V_o}{R_c} + \frac{4N}{R}$$

$$= \frac{5 - 0.2}{2k} + \frac{4N}{R}$$

$$= 2.4\,mA + \frac{4N}{R} \quad \text{---} (1)$$

→ When all 8 inputs of G1 are at logic '1', as discussed in previous section $V_p = 2.25\,V$. Neglecting the current in R_b, the base current in T2 is

$$I_B \approx I_D = \frac{V_{cc} - V_p}{R} = \frac{5 - 2.25}{R} = \frac{2.75}{R} \quad \text{---} (2)$$

→ Since, T_2 is in saturation,

$$I_C = \sigma\beta I_B \quad \text{---} (3)$$

→ from (1), (2), (3);

$$\sigma\beta I_B = 2.4\,mA + \frac{4N}{R}$$

$$\Rightarrow \sigma\beta \frac{2.75}{R} = 2.4\,mA + \frac{4N}{R}$$

$$\therefore N \approx 0.7\sigma\beta - (0.6\,m) * R$$

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If, $\beta = 50$, $\sigma = 0.85$ & $R = 2K\Omega$

$$N = (0.7) * 50 * 0.85 - (0.6m) * (2K)$$

$$= 28.55$$

$$\approx 28$$

Note:

The scenario considered in this example is the heaviest loading condition of gate G1. Here, o/p of G1 is LOW. So, T_2 is saturated. T_2 sinks the current flowing through the i/p terminals of the ~~succe~~ succeeding gates. Maximum current is sinked by T_2 when only one input of the succeeding gates are at logic '0' and rest of the inputs are either at logic '1' or 'Floating'.

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