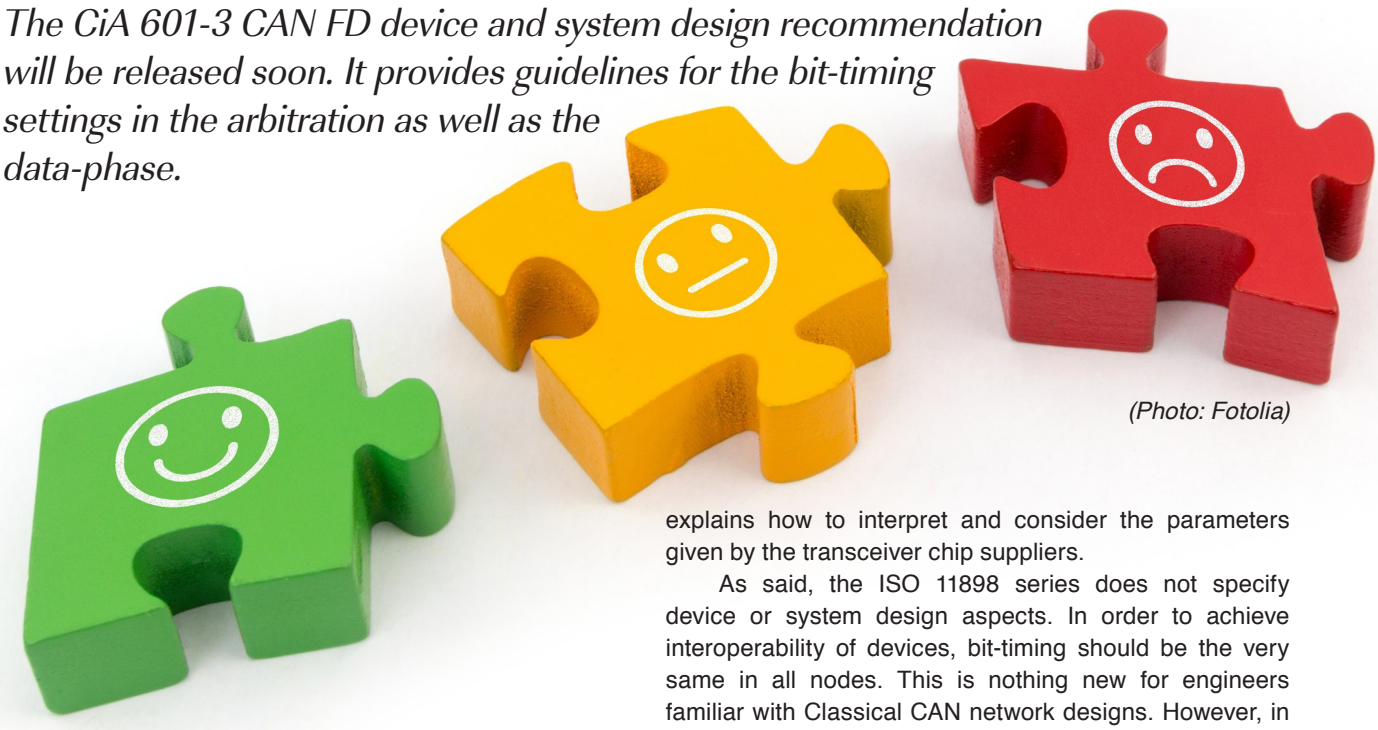
Recommendation for the CAN FD bit-timing

The CiA 601-3 CAN FD device and system design recommendation will be released soon. It provides guidelines for the bit-timing settings in the arbitration as well as the data-phase.



(Photo: Fotolia)

The CAN FD standards, ISO 11898-1 and ISO 11898-2, do not include device and system design specifications. The new editions of ISO 11898-1 and ISO 11898-2 address only semiconductor manufacturers. Device and system designers need additional guidelines and recommendations for the CAN FD device interface. Normally, the device designer needs to fulfill the device design requirements given by the OEM.

The ISO 11898-1:2015 document does not specify the interface to the host controller in detail. It just gives some basic information, which is not sufficient for interoperability and system design aspects. For example, the oscillator frequency is not specified, because this is a device design issue. The CiA 601-2 CAN controller interface specification recommends using 20 MHz, 40 MHz, or 80 MHz. Other frequencies should not be used. Another recommendation in this document is the number of bit-timing registers to be implemented. The ISO standard just requires a small register, which is sufficient for some bit-rate combinations. The CAN FD protocol may use two bit-rates: one for the arbitration phase and another one or the same for the data-phase. In case of using a large ratio between arbitration and data-phase bit-times, the standardized size of the bit-timing registers is not appropriate. Therefore the CiA 601-2 document recommends for the arbitration phase a register programmability of 5 time-quanta (*tq*) to 385 *tq*. The configurability for the data-phase register should be in the range from 4 *tq* to 49 *tq*. Additionally, the CiA 601-2 specification contains some recommendations regarding interrupt sources and message buffer behaviors.

In order to understand the ISO 11898-2:2016 standard from a device designer's point-of-view, the CiA 601-1 specification provides some useful information about the transceiver loop delay symmetry, the bit-timing symmetry, the transmitter delay compensation (TDC). This document explains how to interpret and consider the parameters given by the transceiver chip suppliers.

As said, the ISO 11898 series does not specify device or system design aspects. In order to achieve interoperability of devices, bit-timing should be the very same in all nodes. This is nothing new for engineers familiar with Classical CAN network designs. However, in Classical CAN networks there are some tolerances allowed regarding the bit-timing settings. They are necessary, when nodes with different oscillator frequencies are in the same network. Typically, the sample-point (SP) is given as a range such as 85 % to 90 % with nominal value of 87,5 % (CANopen). The SP is between the phase segment 1 and the phase segment 2 of a bit-time. The bit-time comprises the synchronization segment (always one time-quantum), the propagation segment, the phase segments 1 and 2.

In CAN FD networks, the rules and recommendations needs to be more strict, because higher bit-rates bring the network closer to the physical limits. Of course, when not using the bit-rate switch function, the bit-timing is like in Classical CAN. But when using two bit-rates, the system designer should take care that all nodes apply the very same bit-timing settings.

The nonprofit SAE (Society of Automotive Engineers) International association developed two recommended practices for CAN FD node and system designers. The SAE J2284-4 document specifies a bus-line network running at 2 Mbit/s with all necessary device and system parameters including the bit-timing settings. The SAE J2284-5 document does the same for a point-to-point CAN FD communication running at 5 Mbit/s. The given parameter values are mainly deriving from General Motors CAN FD first system designs. If you read between the lines, you can adapt the specification also for other topologies and bit-rates.

The Japan Automotive Software Platform and Architecture (Jaspar) association develops also guidelines for CAN FD device and system design. The Japanese nonprofit group cooperates with CAN in Automation (CiA). Both associations exchange documents and comment them each other. Recently, there was a joint meeting to discuss the ringing suppression, in order to achieve higher ▷

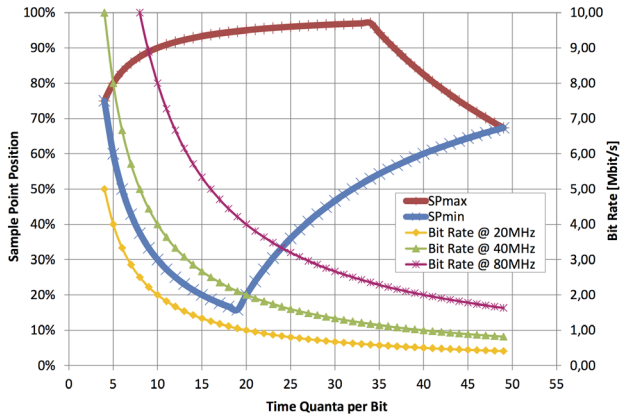


Figure 1: Possible data bit rates and SP positions (min/max); this is a graphical representation of values given in CiA 601-3 (Photo: CiA)

bit-rates or to support hybrid topologies such as multi-star networks.

Recently, CiA has released its CiA 601-3 document. Besides the oscillator frequency (see above), it recommends the bit-timing configuration and some optimization hints for the phase margin. This includes recommendations for the topology, the device design (especially limiting parasitic capacitance).

The bit-timing configuration has two aspects: Setting the nominal time-quantum for the arbitration phase and the data time-quantum for the data-phase as well as setting of the related sample-points including the secondary sample-point (SSP) in the data-phase, when the TDC is used.

Six recommendations

The recommendations given below consider that with each resynchronization, a receiving node can correct a phase error of sjw_D in the data-phase and sjw_A in the arbitration phase. The larger the ratio $sjw_D:BT_D$, the larger the resulting CAN clock tolerance in the data-phase. The same holds for the arbitration phase with $sjw_A:BT_A$. The absolute number of resynchronizations per unit of time increases towards higher bit-rates. However, the absolute value of sjw_D or sjw_A decreases proportionally with the bit-time. In other words, a higher bit-rate leads to more, but smaller resynchronizations. A CAN FD node performs the bit-rate switching at the SP of the BRS (bit-rate switch) bit and the CRC (cyclic redundancy check) delimiter bit. All three available SPs are independent of each other: arbitration phase SP, data phase SP, and data phase SSP. They can be chosen independently.

In the arbitration phase, the nodes are synchronized and need the propagation segment as a waiting time for the round-trip of the bit-signal. In the data-phase, the nodes are not synchronized. Therefore, no delays need to be considered. Nevertheless, the phase-segment 1 should be large enough, to guarantee a stable signal.

For the data-phase bit-timing settings all the following recommendations should be considered. For the arbitration phase just recommendation 3 and 5 apply.

- Recommendation 1: *Choose the highest available CAN clock frequency*

This allows shorter values for the *tq*. Use only recommended CAN clock frequencies (see above).

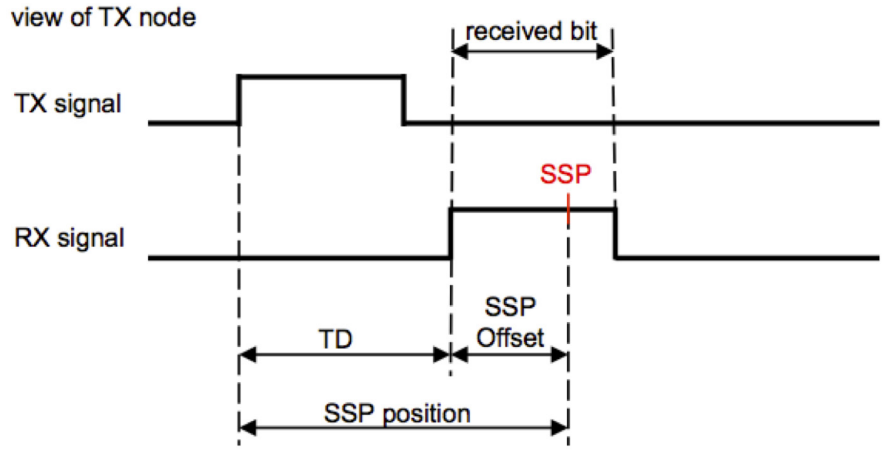


Figure 2: Definition of the SSP (secondary sample-point) position (Photo: CiA)

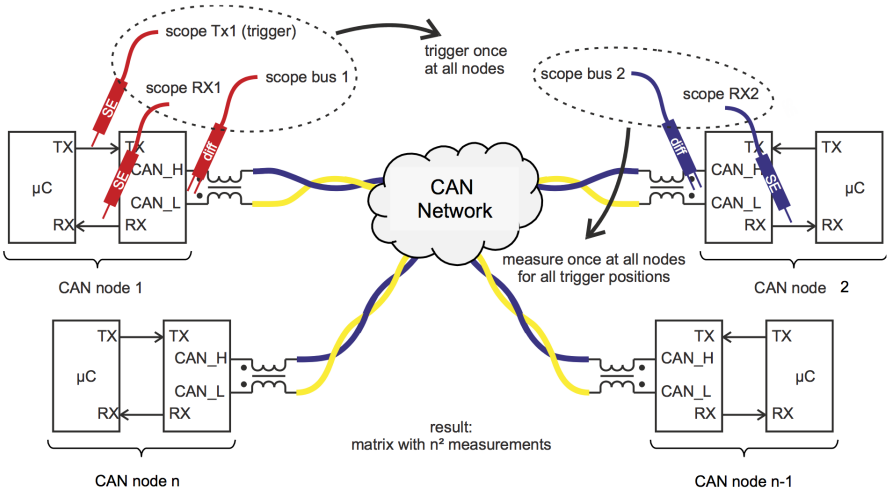


Figure 3: Measurement setup for the evaluation of the asymmetry introduced by the topology (Photo: CiA)

- Recommendation 2: *Set the BRP_A bit-rate prescaler equal BRP_B*

This leads to identical *tq* values in both phases. This prevents that during bit-rate switching inside the CAN FD data frame an existing quantization error can transform into a phase error.

- Recommendation 3: *Choose BRP_A and BRP_D as low as possible*

Lower BRPs lead to shorter *tq*, which allows a higher resolution of the bit-time. This has the advantage that the SP can be placed more accurately to the optimal position. The size of the synchronization segment is shorter and reduces the quantization error. Additionally, the receiving node can synchronize more accurately to the transmitting node, which increases the available robustness.

- Recommendation 4: *Configure all CAN FD nodes to have the same arbitration phase SP and the same data phase SP*

The simplest way to achieve this is to use the identical bit-timing configuration in all CAN nodes. This is not always possible, when different CAN clock frequencies are used. The arbitration phase SP and the data phase SP can be different, without any impact on robustness. Different SPs in the CAN FD nodes reduce robustness, because this leads to different lengths' of the BRS bits and CRC delimiter bits in the different nodes and a phase error introduced by the bit-rate switching. The SSP can be different in the CAN nodes, without influencing robustness.

- Recommendation 5: *Chose sjw_D and sjw_A as large as possible*

The maximal possible values are min ($ps1_{A/D}$, $ps2_{A/D}$). A large sjw_A value allows the CAN node to resynchronize quickly to the transmitting node. A large sjw_D value maximizes the CAN clock tolerance.

- Recommendation 6: *Enable TDC for data bit-rates higher than 1 Mbit/s*

In this case, the BRP_D shall be set to 1 or 2 (see ISO 11898-1:2015). It is not recommended to configure the TDC with a fixed value, because the large transmitter delay variations.

Location of sample-points

The SP locations of the arbitration phase and the data-phase may be different. If in the arbitration phase the SP is at the very far end of the bit-time, the maximum possible network length can be achieved. Sampling earlier reduces the achievable network length, but increases robustness. A value of higher than 80 % is not recommended for automotive applications due to robustness reasons

The SP location in the data-phase depends on the maximum possible bit asymmetries. There are two asymmetries, one for the worst lengthening of dominant bits (A1) and another for the worst shortening of dominant bits (A2) in a given network set-up. Both values are given normally in ns. Both values are the sum of asymmetries

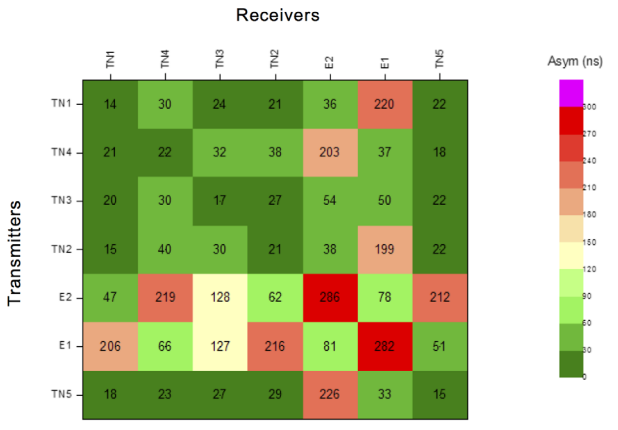


Figure 4: Example of worst-case A1 values for all communciation relationships (Photo: CiA)

caused by the physical network elements including transceiver, cabling, connectors, and optional circuitry (e.g. galvanic isolation). In order to avoid compensations, absolute values are added. ISO 11898-2:2016 specifies the asymmetry values for 2 Mbit/s and for 5 Mbit/s qualified transceivers. The asymmetries caused by the other physical network components are given by datasheets or needs to be estimated or measured. The system designer selects the worst-case connections in network and calculates or measures the both asymmetry values. Another option is to simulate it. There are providers offering such simulation services.

$A1_{topology}$ and $A2_{topology}$ values are different for every communication relationship. This means in a setup with n CAN nodes there are n^2 values for $A1_{topology}$ and n^2 values for $A2_{topology}$. To represent the worst-case, the maximal $A1_{topology}$ and the maximal $A2_{topology}$ values are used to calculate A1 respectively A2. CiA provides with the CiA 601-3 specification a spreadsheet to prove the robustness of the chosen bit-timing settings and the sample-points.

The PM is the allowed shift of a bit edge towards the SP of the bit, at a given tolerance of the CAN clock frequency (d_{fused}). In other words, this is the edge shift caused by physical layer effects that is still tolerated by the CAN protocol.

The worst-case bit sequence, i.e. that leads to the lowest PMs, is when the transmitting node sends five dominant bits followed by one recessive stuff bit (for details see /CiA601-1/). This is the longest possible sequence of dominant bits followed by a recessive bit inside a frame. Current transceiver designs cause the largest bit asymmetry at this bit sequence, i.e. the recessive bit is typically shorter than its nominal value. Further effects additionally raise the asymmetry: e.g. asymmetric rise and fall times, bus topology, EMC jitter, etc.

The PM1 and PM2 values for the RX direction given in s (aecond) can be calculated by the following equations:

$$PM1 < \frac{6 \cdot BT_D - PS2_D - tq_D}{(1+df_{used})} - \frac{5 \cdot BT_D}{(1-df_{used})} \quad (1)$$

$$PM2 < \frac{5 \cdot BT_D}{(1+df_{used})} - \frac{5 \cdot BT_D - PS2_D}{(1-df_{used})} \quad (2)$$

with *PM1* = phase margin 1, *PM2* = phase margin 2, BT_D = data-phase bit-time, $PS2_D$ = data-phase phase segment 2.

Additionally, *PM1* and *PM2* for the TX direction needs to be calculated and considered.

Optimizing the system design

The transceiver chips or the SBCs cause a significant part of the overall asymmetry. Therefore it is recommended, to use always components qualified for higher bit-rates. Even if for 2-Mbit/s CAN FD networks, 5-Mbit/s qualified chips should be chosen.

The “badly” designed wiring harness can add many asymmetries. The following recommendations should be considered:

- Use a linear topology, terminated at both ends.
- Reduce the total bus length.
- Limit the number of CAN nodes.

- Avoid long, not terminated stubs, which are branches from the well-terminated CAN lines; use stubs of "cm-range" instead of "m-range". Consider a high-ohmic termination of not terminated stubs.
- Optimize the low-ohmic termination (resistor position and resistor value). Another option is to increase the low-ohmic termination resistance (e.g. 124 Ω instead of 120 Ω) to compensate for the high-ohmic terminations in systems with many nodes.
- Reduce the number of stubs per star point. The more stubs are connected to one star point, the higher the reflection factor gets.
- In case, a star point with many branches is required due to mechanical constraints, avoid identical stub lengths per star point.
- In case, multiple star points are required, keep a significant distance between the two star points.
- Cable cross section: increase it to approximately 2 x 0,35 mm of the CAN_H and CAN_L wire.

Besides these system design recommendations, the device designer should consider the following hints:

- Limit the parasitic capacitance of the device. The parasitic capacitance of the device includes the following parameters: additional ESD protection elements; parasitic capacitance of the connector; parasitic capacitance of the CAN_H or CAN_L wire; parasitic capacitance of the CMC; the parasitic capacitance of the transceiver input pins. All this parasitic capacitance should be below 80 pF per channel.
- CAN_H and CAN_L PCB tracks from connector to transceiver should be of equal distance and parallel.
- Keep the TXD and RXD PCB tracks between host controller and transceiver short.
- Configure the host controller TXD output pin with strong push-pull behavior: a pull-up or pull-down resistor behavior can cause additional asymmetries and propagation delays.
- Avoid any serial components like logical gates or resistors within the TXD and RXD connection lines between host controller and transceiver. In case galvanic isolation is required, take care of the potential additional asymmetry and select components accordingly.
- Use a CAN clock source with lower clock jitter.
- Avoid galvanic isolation, or use a galvanic isolation solution that adds only a small asymmetry.
- In order to optimize the PM, the following hints should be considered:
- Optimize the bit-timing configuration by reducing the *tq* length. This increases PM1 by reducing the quantization error.
- Use a CAN clock with lower tolerance (dfused). This improves PM1 and PM2.

Further recommendations under development

Besides galvanic isolation, there are some other options, which system and device designers may consider. European carmakers often use common-mode chokes, for example. Further add-on circuitry includes a split-termination (two 60-Ω resistors) with a capacitor to ground.

References

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[2] Florian Hartwich: "The configuration of the CAN bit-timing", 6th international CAN Conference (iCC 1999), Turin, Italy, 1999

[3] Marc Schreiner: "CAN FD system design", 15th international CAN Conference (iCC 2015), Vienna, Austria, 2015

[4] Y. Horii, "Ringing suppression technology to achieve higher data rates using CAN FD," 15th international CAN Conference (iCC 2015), Vienna, Austria, 2015

[5] CAN Newsletter magazine 2012 to 2017 (several articles), Nuremberg, Germany.

[6] CiA 601 series, Nuremberg, Germany

The CiA community discusses a ringing suppression option, which will be specified in the CiA 601-4 document. It is still under development. In general, such ringing suppression circuitry changes dynamically the network impedance to reduce the ringing in the beginning of the bit-time. Before the SP, the impedance is dynamically switched back to the nominal value. There are two approaches discussed:

- Ringing suppression circuitry on the critical receiving nodes (CiA 601-4 version 1.0)
- Ringing suppression circuitry on the transmitting nodes

The updated CiA 601-4 will just specify the requirements and not the implementations. The automotive industry is highly interested in ringing suppression. It would allow achieving higher bit-rates (desired is 8 Mbit/s) or to allow higher asymmetries caused by the network topology.

The common-mode choke specification for CAN FD networks will be given in CiA 601-6. Also this document is under development. It will mainly contain recommendations and how to measure the values to be provided in datasheets. It is the goal, to make datasheet values more comparable than today.

CiA members are also working on a cable specification (CiA 110). It is intended to define parameters and how to measure them, in order to make datasheets comparable. ◀

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