Communication between PS (CPU) and PL (FPGA)

PS (Processing System)

The Processing System (PS) corresponds to the processor part of the Xilinx Zynq UltraScale+ MPSoC integrated into the KV260 Vision AI Starter Kit. It includes the elements required to run software and manage the general functions of an embedded system.

- Main Components
  - ARM processors:
    - 4 Cortex-A53 cores (64-bit) for running operating systems such as Linux and complex applications.
    - 2 Cortex-R5F cores for real-time tasks.
      - Mali-400MP2 GPU for graphics processing and display.
      - Memory controller compatible with DDR4/LPDDR4, ensuring fast data access.
      - Communication interfaces: Ethernet, USB, UART, SPI, I^2C, CAN, GPIO, etc.
      - Internal buses and exchange mechanisms (AXI-GP, AXI-HP, AXI-ACP, DMA, IRQ) enabling communication with the programmable logic part of the SoC.
- **Role**

The PS handles:

- running the operating system and software applications,
- managing memory and integrated peripherals
- coordinating with the programmable logic to delegate hardware-accelerated processing,
- providing network and user interfaces for the entire embedded system.

- **In the KV260**

On the KV260, the PS acts as the “software core” of the module: it runs Linux (Ubuntu or PetaLinux), controls integrated peripherals, manages memory, and supervises communication with hardware accelerators implemented in the programmable logic.

PL (Programmable Logic)

The Programmable Logic (PL) is the reconfigurable logic part of the Xilinx Zynq UltraScale+ MPSoC. It is an integrated FPGA that allows implementing hardware architectures tailored to the specific needs of the application.

- **Main Components and Resources**
  - Configurable logic blocks to create custom digital circuits.
  - **DSPs (Digital Signal Processing)** for fast mathematical and signal-processing operations.
  - **BRAM (Block RAM)** and embedded memories for temporary data storage.
  - **Programmable I/Os** to interface with sensors, cameras, or other peripherals.
  - **AXI interfaces (GP, HP, ACP)** along with DMA and IRQ for efficient exchange with the PS.

- **Role**

The PL enables:

- executing parallel and hardware-accelerated processing (vision, AI, signal processing),
- offloading heavy, repetitive tasks from the processor,
- adapting the system by dynamically reconfiguring hardware blocks,
- integrating specific or proprietary interfaces for particular needs.

- **In the KV260**

On the KV260, the PL is used to host optimized hardware accelerators (e.g., for AI, video processing, or computer vision). It acts as the module's "reconfigurable hardware core," working alongside the PS to deliver high performance and maximum flexibility.

Communication between PS and PL

Communication between the Processing System (PS) and the Programmable Logic (PL) in a Xilinx Zynq UltraScale+ MPSoC relies on a set of integrated buses and mechanisms. It enables the processor to efficiently exchange data and commands with the programmable logic.

- **Main Communication Methods**

  - **AXI (Advanced eXtensible Interface):**
    - AXI-GP (General Purpose) for configuration and control exchanges.
    - AXI-HP (High Performance) for large-volume data transfers between memory and logic.
    - AXI-ACP (Accelerator Coherency Port) for direct, cache-coherent access to the processor.
      - **DMA (Direct Memory Access):** fast data transfers without CPU involvement.
      - **Interrupts (IRQ):** notifications from the logic to the processor when an event occurs.
      - **GPIO:** simple communication through logic signals.
      - **Shared memory (DDR or BRAM):** space accessible by both the processor and the programmable logic.

- **Role of this Communication**

  - Configuring and controlling hardware logic.
  - High-speed data transfers (video, AI, signals).
  - Synchronization via interrupts.
  - Seamless integration between software processing and hardware acceleration.

PS ↔ PL Communication in the KV260

On the KV260 Vision AI Starter Kit, based on the Zynq UltraScale+ MPSoC, PS–PL communication is optimized for computer vision and artificial intelligence applications.

- **Specifically Used Methods**
  - **AXI-GP:** for configuring and controlling hardware accelerators implemented in the PL.
  - **AXI-HP + DMA:** for transferring large volumes of data (e.g., video streams from a camera) directly between memory and the PL without overloading the processor.
  - **AXI-ACP:** used when the PL must share data with ARM A53 cores while maintaining cache coherency.
  - **Interrupts (IRQ):** to signal completion of an AI task or video pipeline processing.
  - **Shared DDR memory:** used as a buffer to exchange images or intermediate results between PS and PL.

- **Role in the KV260**
  - Allows the processor to run Linux and orchestrate the system.
  - Offloads heavy vision and AI tasks to the reconfigurable FPGA.
  - Ensures a continuous, high-performance flow between cameras, hardware processing, and display or network transmission.

In summary, on the KV260, PS ↔ PL communication is designed to provide a seamless pipeline between acquisition (camera), accelerated processing (FPGA), and software exploitation (CPU/Linux).