# Mostafa Elsanousi

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## EDUCATION

**Virginia Tech Polytechnic Institute and State University** **Blacksburg, VA**

- **Degree:** Bachelor of Science in Computer Engineering *August 2024 – December 2027*
- **Cumulative GPA:** 3.83 / 4.0
- **Technical Summary:** Computer Engineering student focused on embedded/firmware development, low-level hardware bring-up/debug, and FPGA-based digital systems. Hands-on with C/C++ and Verilog (Vivado/Quartus), including an Artix-7 FIR DSP project validated in simulation + hardware.
- **Target Roles:** Firmware/Embedded • Device Drivers/Embedded Linux • FPGA/RTL • Design Verification (Simulation)

## SKILLS

- **Programming**: C, C++, Python, R, Verilog (Structural and Dataflow), MATLAB
- **Tools & Software:** Visual Studio Code, Jupyter Notebook, LTspice, Intel Quartus Prime, Vivado, KiCad, Magic VLSI, Ngspice
- **Hardware:** Arduino, MSP432, STM32, Digilent Basys 3 FPGA

## EXPERIENCE

**Securis, Inc.,** **Chantilly, VA**

*ITAD Technician Intern* *June 2025 – August 2025*

- Performed NIST-compliant secure data sanitization on HDD/SSD inventory using Blancco Drive Eraser.
- Diagnosed and refurbished desktops/laptops/servers; executed RAM/SSD upgrades and BIOS resets for redeployment/resale.
- Tracked assets via barcode inventory systems and routed equipment for reuse, recycling, or disassembly.

**Magdi Algabani Group** **Dubai, UAE**

*Cybersecurity & Embedded Systems Research Intern* *May 2021 – August 2021 & May 2022 – August 2022*

**Hybrid Electric Vehicles Team (HEVT) | Virginia Tech** **Blacksburg, VA**

*Incoming CAV Subteam Member* *Spring 2026 – Present*

- Incoming member of HEVT CAV subteam supporting embedded development and system integration.

## PROJECTS

**FPGA-Based Digital Signal Processing System | Personal Project**

*Independent Developer* *May 2025 – August 2025*

- Designed and implemented 8-tap FIR low-pass filter on Xilinx Artix-7 FPGA (Basys 3) using Verilog HDL for real-time digital signal filtering with 200 kHz passband frequency
- Developed pipelined filter architecture utilizing DSP slices for coefficient multiplication and accumulation, optimizing hardware resource utilization through symmetric tap pair addition
- Implemented user interface featuring LCD display for sorting information and color-coded LED indicators
- Integrated user control interface with board switches for filter parameter adjustment and 7-segment display for real-time output visualization, validating functionality through simulation and hardware testing
- Achieved real-time signal processing with sub-millisecond latency, demonstrating reliable filter performance in hardware testing

**Zynq-7000 PS–PL Ethernet Bring-Up | BRICC Lab**

*Undergraduate Researcher* *October 2025 – Present*

- Built a Vivado block design integrating the Zynq-7000 PS with clocks/resets and an AXI interconnect; memory-mapped custom PL peripherals (e.g., AXI GPIO/logic) into the ARM address space via AXI4-Lite and exported the XSA/bitstream hardware platform.
- Wrote Vitis standalone C app to validate PS↔PL MMIO register R/W over AXI; extending the same PS-controlled workflow to Zynq PS Ethernet pin/config bring-up and Ethernet driver verification using UART serial debug and board programming.
- Used Linux + GNU toolchain workflows for embedded development (build/run/debug from terminal; basic bash automation for repeatable builds/log capture).