Technology: Level 1
T103 Computer architecture,
logic and information processing
Licensed for use by the Arab Open University

T103

Tutor-marked Assignment 1

Contents Cut-off date Apr 19, 2010
T103 TMA Spring- 2010

Part I

Problem 1: [10 Marks]

1. Convert the following decimal numbers: + 36 and -30 to binary then add them using:
    a) signed-magnitude representation
    b) signed-1's complement
    c) signed-2's complement. Indicate if we have overflow.

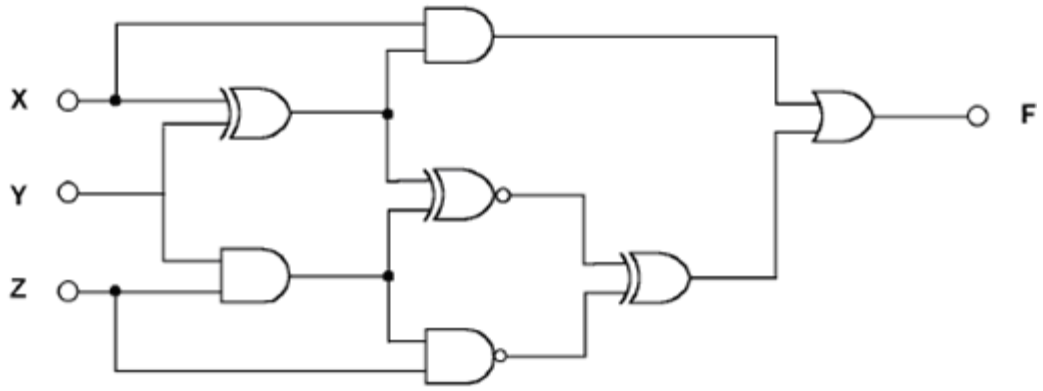
2. Express -0.75 in the revised 14-bit floating-point model with bias = 16.

Problem 2: [10 Marks]

1. Show that $xz = (x + y)(x+y')(x' + z)$ using 2 different methods:

Problem 3: [10 Marks]

1. Find the truth table that describes the following circuit:



2. Describe the JK flip-flop by its characteristic table and draw the related Moore and Mealy machine.

Part II:

Problem 4: [40 Marks]

1. Consider the following assembly program:

```
        ORG     100
        Load    One
        Store   X
Loop,   Load    X
        Subt    Ten
        SkipCond 000
Jump    Endloop
        Add     X
        Store   Sum
        Load    X
        Add     One
        Store   X
        Jump    Loop
Endloop,Load    Sum
        Output
        Halt
Sum,    Dec     0
X,      Dec     0
One,    Dec     1
Ten,    Dec     10
        END
```

a) Present the register transfer notation (RTN) for each of the following instructions:
   - Load X
   - Store X
   - Add X
   - Subt X

b) Describe the output of the above program.

c) Use the MARIE Simulator to run the above program (MarieDP1 or MarieSim)

- Show the changes in the registers (AC, IR, MAR, MBR, PC); Take snapshots showing these registers during the execution of the first Load instruction.

d) Give a description for these changes in (AC, IR, MBR, MAR, PC)

Part III:

Problem 5: [30 Marks]

1. Suppose a computer using fully associative cache has 216 words of main memory and a cache of 64 blocks, where each cache block contains 32 words.

   a. How many blocks of main memory are there?
   b. What is the format of a memory address as seen by the cache, i.e., what are the sizes of the tag and word fields?
   c. To which cache block will the memory reference F8C9 map?

2. Do a research to find the newest technologies used for the cache memory inside the new i7 Intel CPU's, and the maximum sizes used.