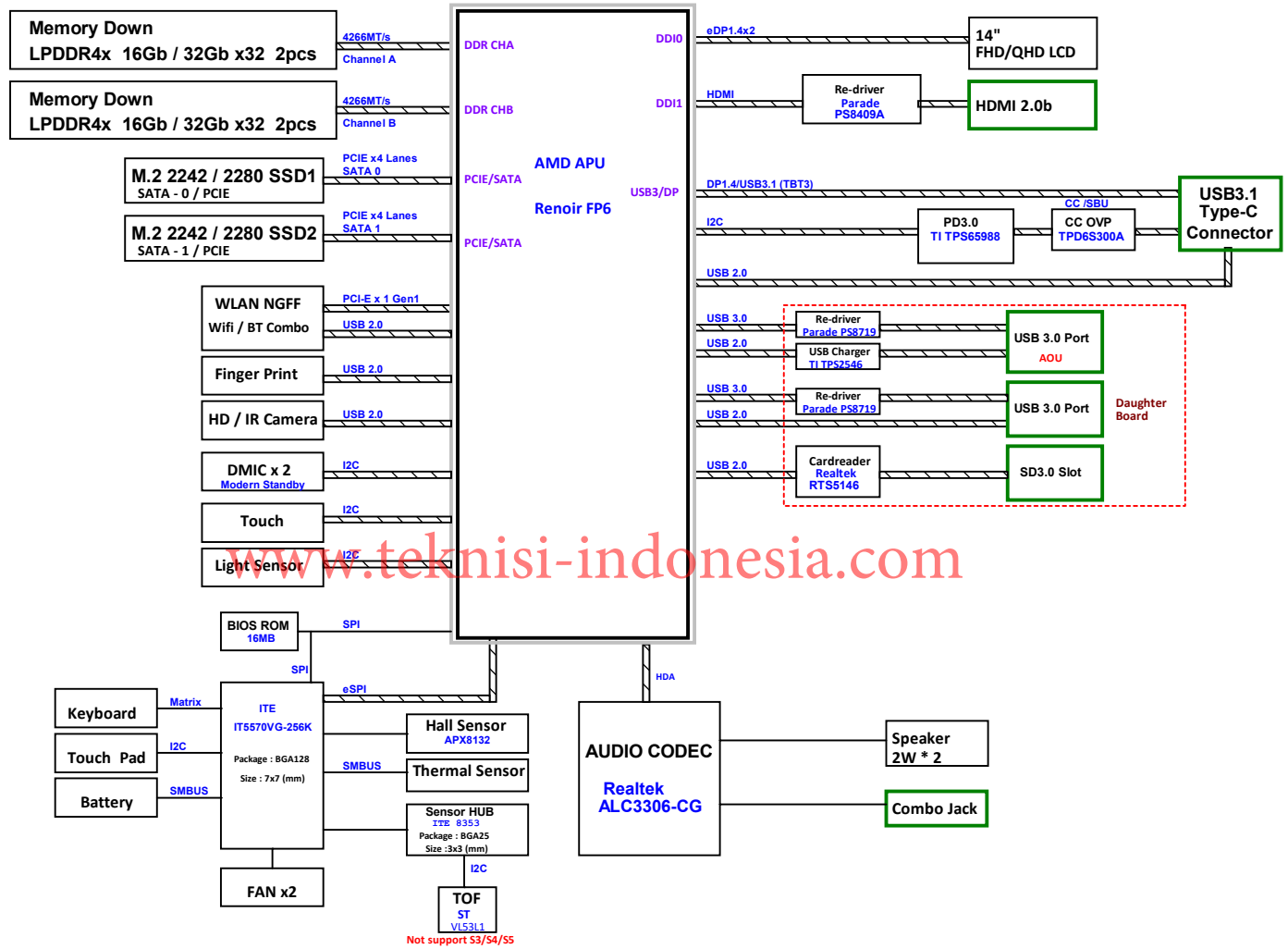
Aries 4B AMD Renoir FP6 Block Diagram



PCB 8L STACK UP

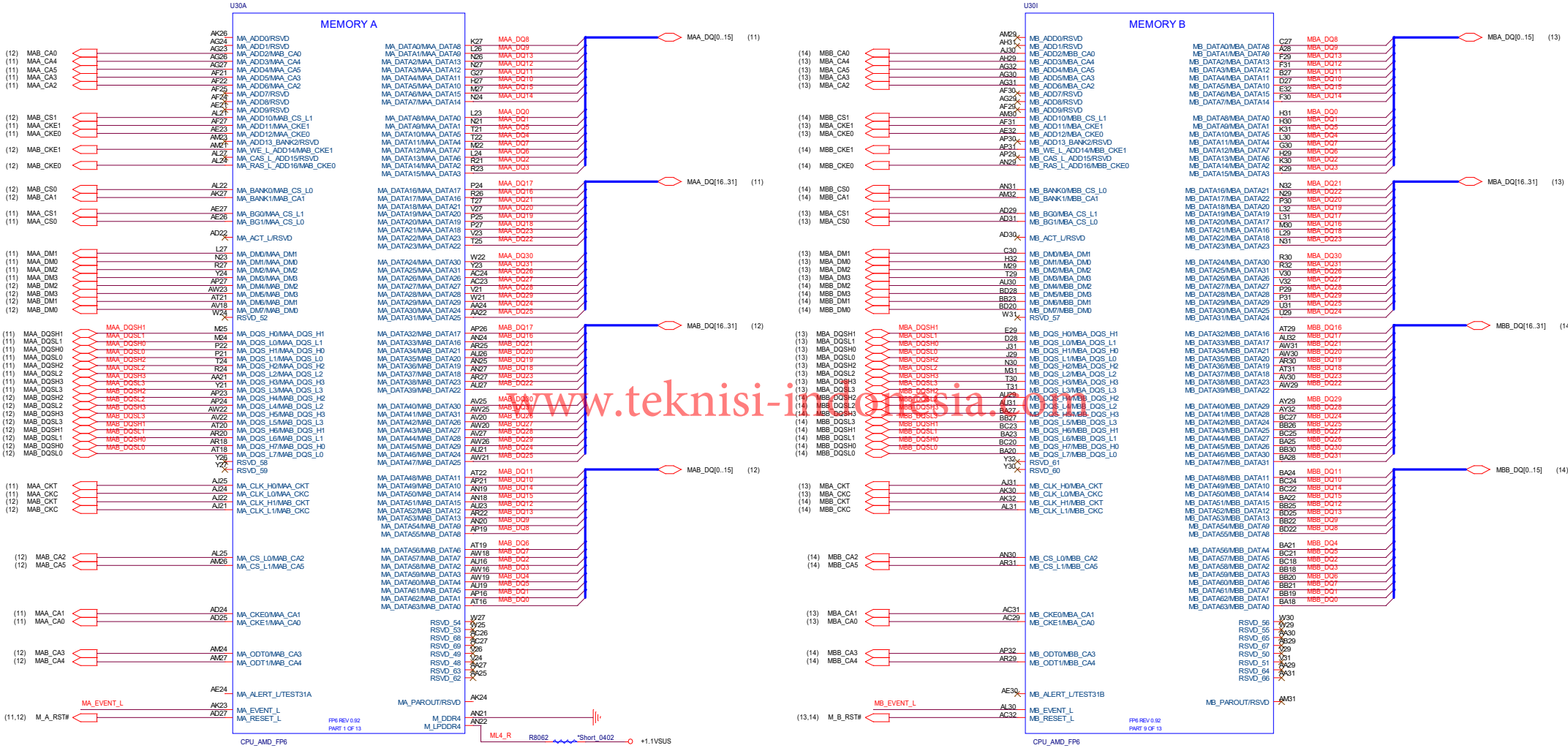
LAYER 1 : TOP
LAYER 2 : SVCC
LAYER 3 : IN1
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT

PROJECT :LS3
Quanta Computer Inc.
BU2

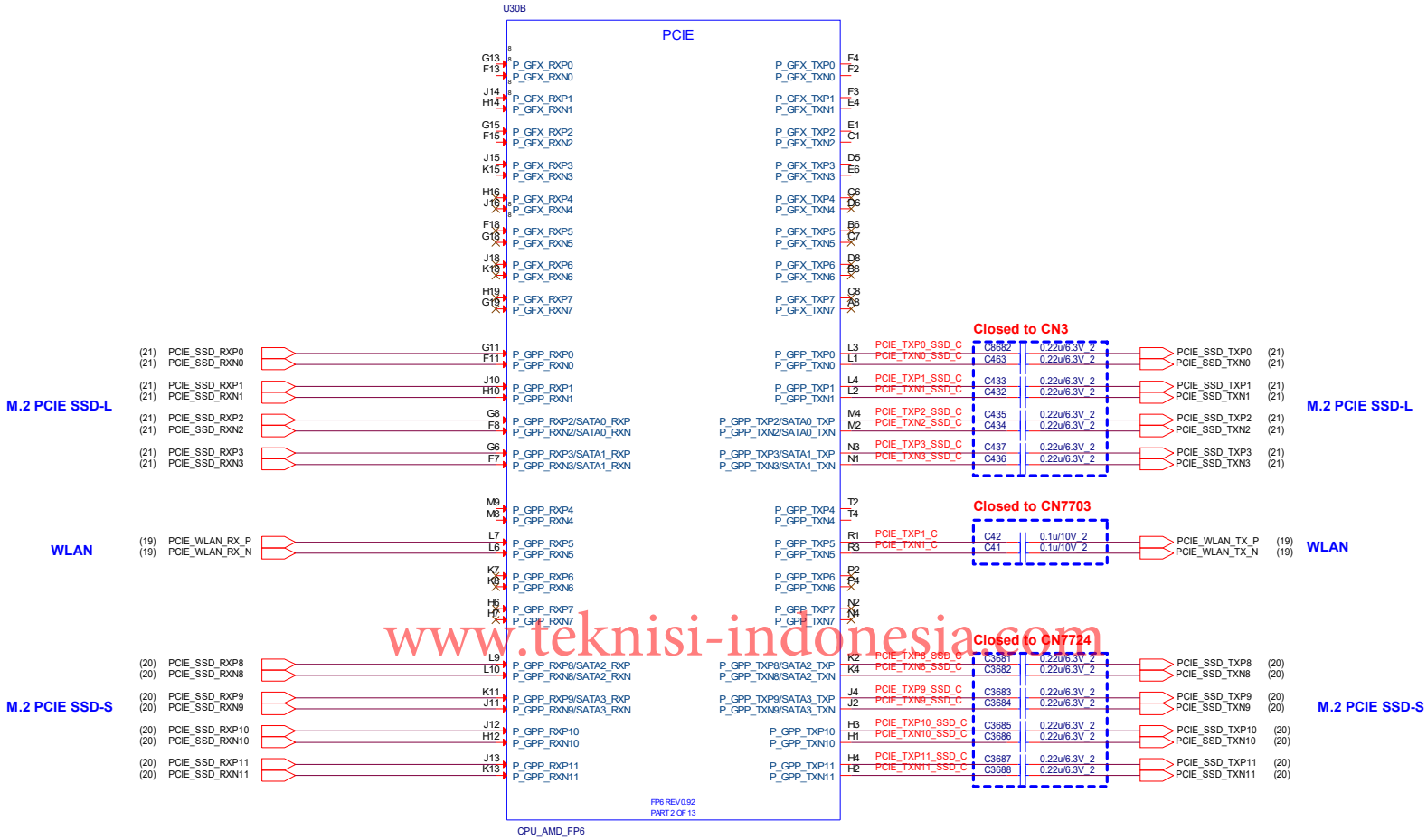
Power Diagram

02

Custom	PROJECT : LS3 Quanta Computer Inc.		
BU2	Size	Document Number Power Map	Rev 1A
Friday, January 17, 2020	Date:	Sheet	of



PROJECT : LS3		
Quanta Computer Inc.		
BU2	Size	Document Number: PIC 1/8(PCIE) — Rev: A1A
	Date: Friday, January 17, 2020	Sheet 3 of 54



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BU2

PROJECT : LS3

Quanta Computer Inc.

Size	Document Number	Rev
	eDP/DDI/MISC	1A

Date: Friday, January 17, 2020 | Sheet 4 of 54

APU DISPLAY and MISC

05

DDI0 output to FHD Panel

DDI1 output to HDMI conn

EC-EVT-E14

Connect to EC SMBUS

eDP

HDMI

TYPE C DP

EMI/ESD reserve

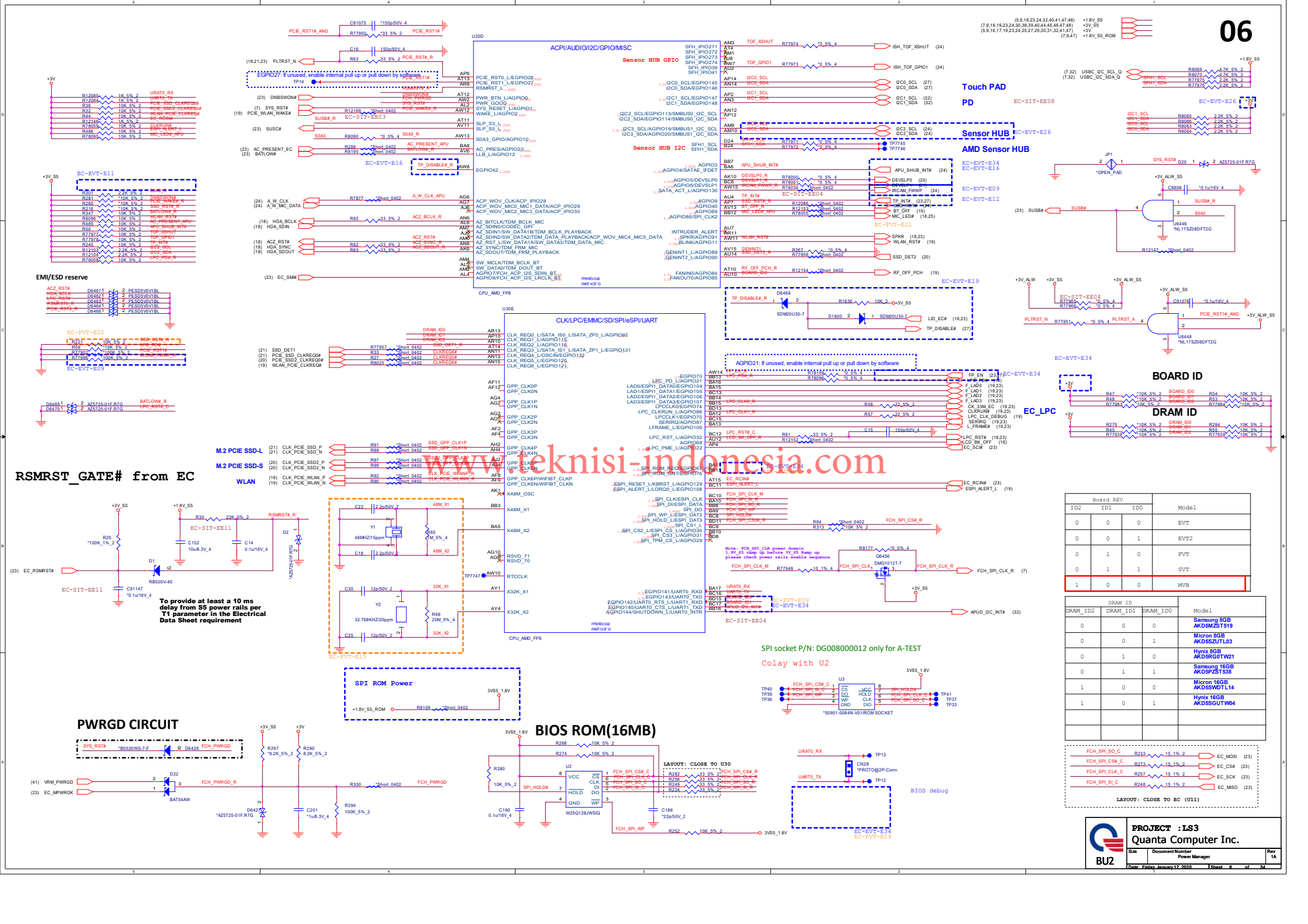
APU Serial VID

Place near APU within 500mil
CRB: SVC & SVD 22 ohm follow check list 0 ohm.

VSS_sense_A for VDDCR and VDDCR_SOC

HDT+ Connector for Debug only

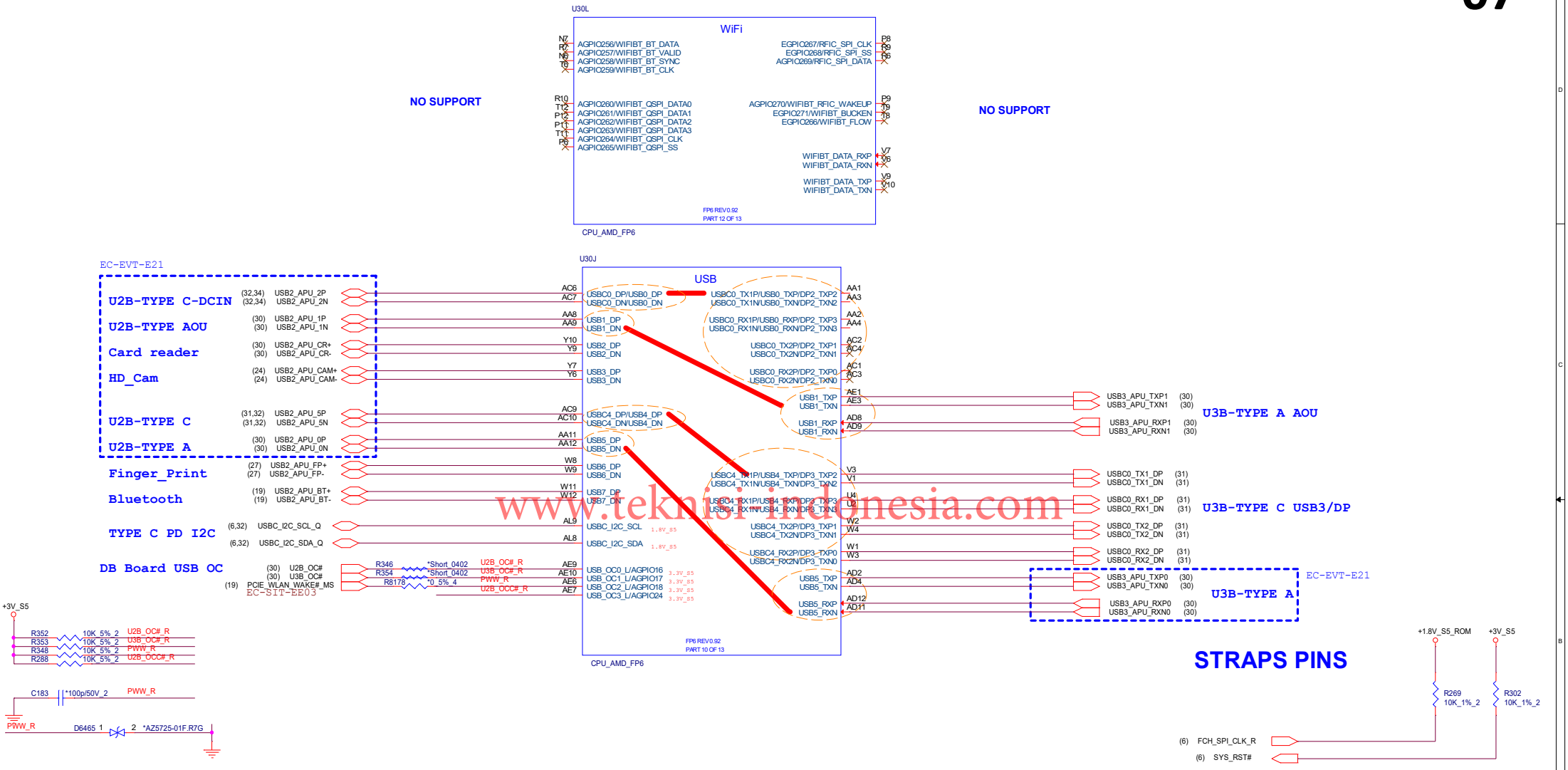
PROJECT	:LS3
	Quanta Computer Inc.
BU2	
Size	Document Number: APU Display Interface
Rev	1A
Date:	Monday, March 23, 2020
Sheet	5 of 54



Board REV			
ID2	ID1	ID0	Model
0	0	0	EVT
0	0	1	EVT2
0	1	0	FVT
0	1	1	SVT
1	0	0	MVB

DRAM_ID			
DRAM_ID2	DRAM_ID1	DRAM_ID0	Model
0	0	0	Samsung 8GB AKD5MZS1519
0	0	1	Micron 8GB AKD5SZUTL03
0	1	0	Hynix 8GB AKD5RG0TW21
0	1	1	Samsung 16GB AKD5PZST538
1	0	0	Micron 16GB AKD5SWDTL14
1	0	1	Hynix 16GB AKD5SGUTW04

PROJECT :LS3
Quanta Computer Inc.
BU2
Size | Document Number: Power Manager | Rev 1A
Date: Friday, January 17, 2020 | Sheet 6 of 54



REQUIRED STRAPS

	FCH_SPI_CLK_R	SYS_RST#
PULL HIGH	Use 48Mhz crystal clock and generate both internal and external clocks (pulled up VDD_18_S5) DEFAULT	normal reset mode (pulled up VDD_33_S5) DEFAULT

USB20_P0	USB20_P1	USB20_P2	USB20_P3	USB20_P4	USB20_P5	USB20_P6	USB20_P7
USB2.0 TYPEC DCIN	USB3.0 TYPEA	Card Reader	HD_CAM	USB2.0 TYPEC	USB3.0 TYPEA	FP	BT

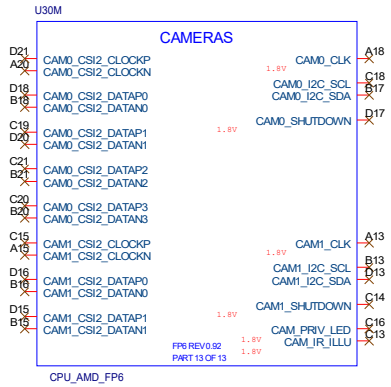
USB30_P1	USB30_P4	USB30_P5
USB3.0 TYPEA	USB3.0 TYPEC	USB3.0 TYPEA

BU2

PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
	CPU Decoupling 1	1A

Date: Friday, January 17, 2020 Sheet 7 of 54



BU2

PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
	CPU Decoupling 2	1A

Date: Friday, January 17, 2020 Sheet 8 of 54

APU POWER

09

BOTTOM SIDE OUTSIDE OF APU

BOTTOM SIDE UNDER APU

BOTTOM SIDE DECOUPLING UNDER APU

If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

Background: VDDIO_VPH is a power supply pin on FP6 package used by certain phys within RN. The purpose of separating these phys is to allow better power efficiency and battery life in certain configurations. However AMD cannot guarantee the phys will meet compliance when 1.1V nominal source is used for VDDIO_VPH. This case is typically only for LPDDR4(x) based systems using the VDDIO_MEM_S3 1.1V source for VDDIO_VPH as previously recommended. A 1.2V or 1.8V nominal source will meet the phy requirements and is recommended. 1.2V is preferred for power savings if DPO is implemented for eDP.

Fix: Use either 1.2V or 1.8V nominal source for VDDIO_VPH. Ensure the source meets the tolerance and ripple requirements defined in the FP6 IRM (PID# 56328)

BOTTOM SIDE OUTSIDE OF APU

BOTTOM SIDE DECOUPLING UNDER APU

BOTTOM SIDE DECOUPLING UNDER APU

BOTTOM SIDE DECOUPLING UNDER APU

BOTTOM SIDE DECOUPLING UNDER APU

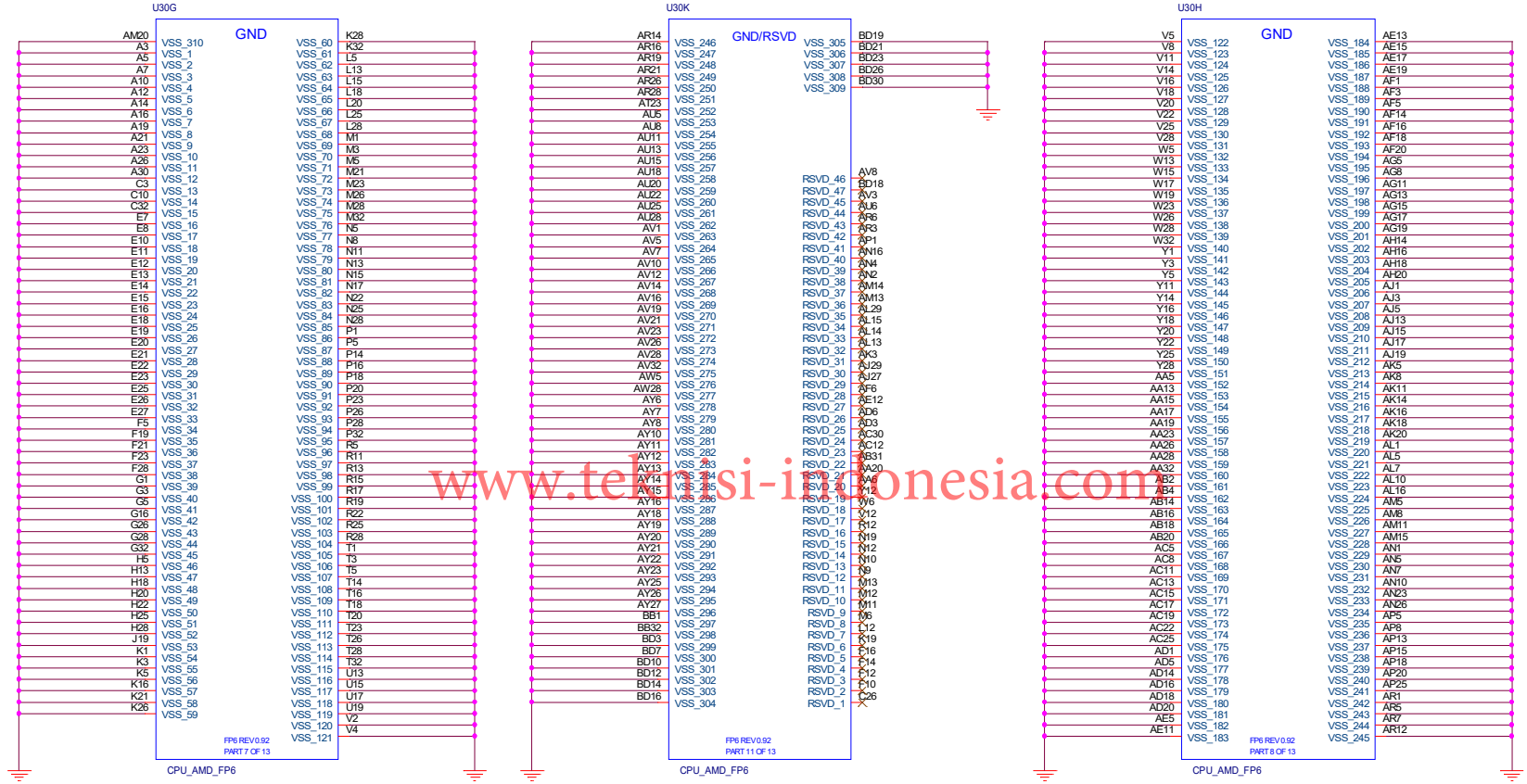
BOTTOM SIDE DECOUPLING UNDER APU

BOTTOM SIDE DECOUPLING UNDER APU

BOTTOM SIDE DECOUPLING UNDER APU

BOTTOM SIDE DECOUPLING UNDER APU

PROJECT : LS3	
Quanta Computer Inc.	
BU2	Size: Document Number: CPU Decoupling 3 — Rev: 1A
Date: Friday, March 13, 2020	Sheet 9 of 54



BU2

PROJECT : LS3

Quanta Computer Inc.

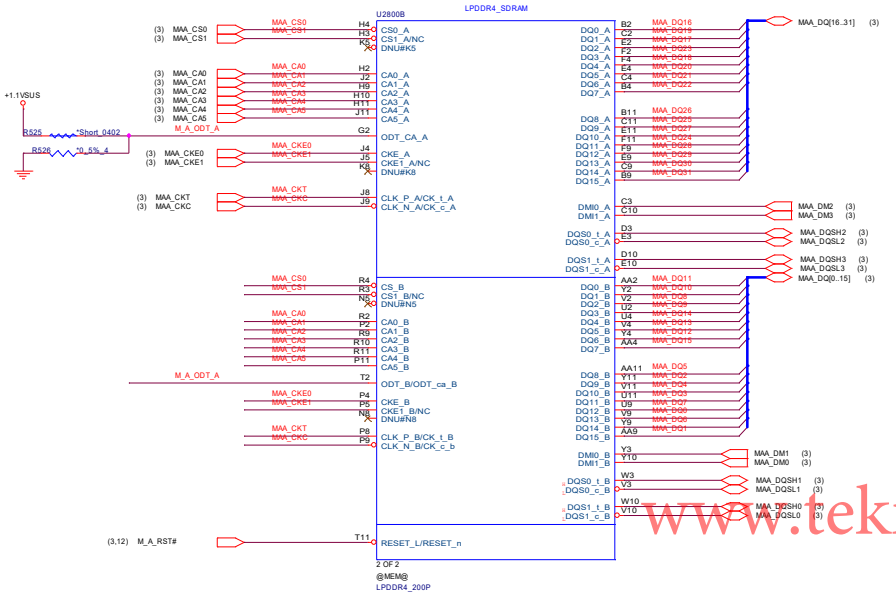
Size	Document Number	Rev
	GND	1A

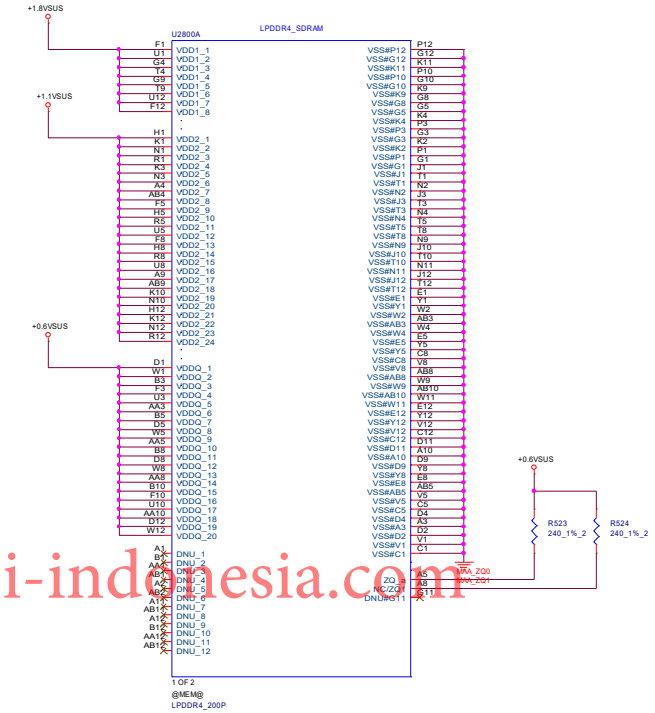
Date: Friday, January 17, 2020 Sheet 10 of 54

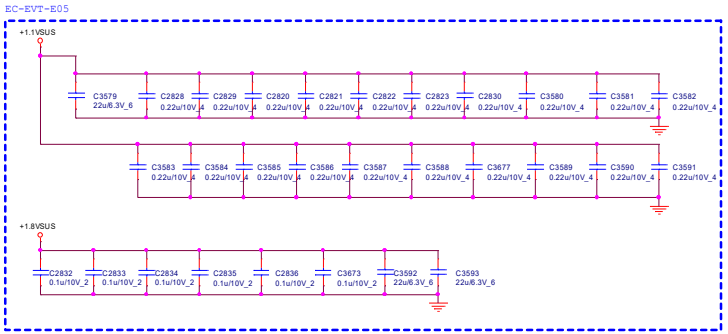
(3,9,12,13,14,39,48) +1.1VSUS
(5,6,9,16,17,19,23,24,25,27,29,30,31,32,41,47) +3V

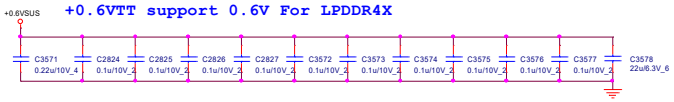
Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-MAA









BU2

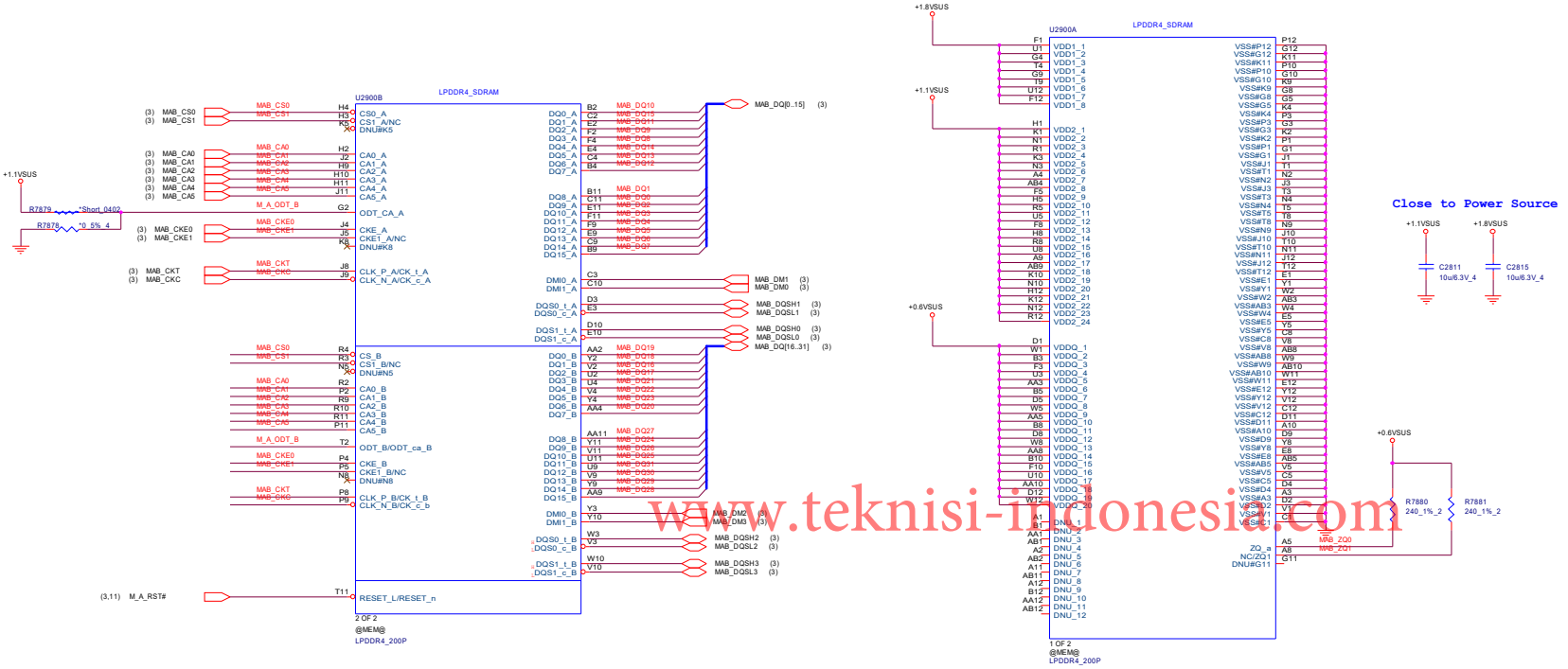
PROJECT : LS3
Quanta Computer Inc.

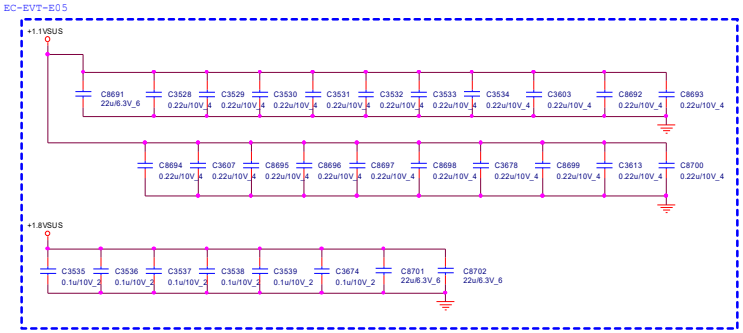
Size	Document Number	Rev
	LPDDR4_A Channel_Memory Down	1A

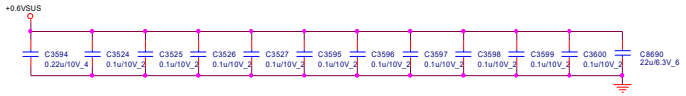
Date: Friday, January 17, 2020 Sheet 11 of 54

Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-MAB



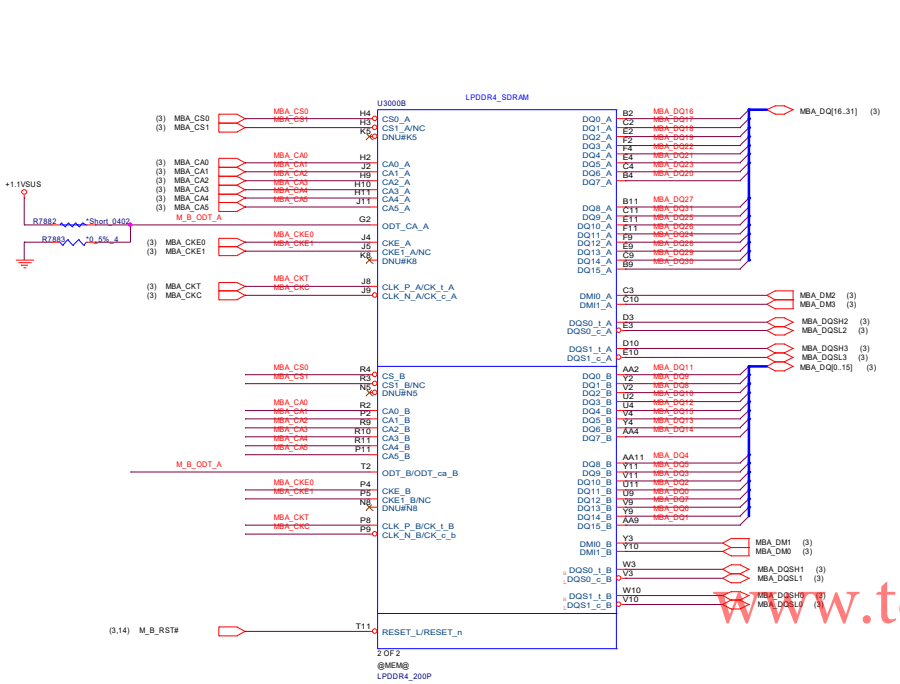


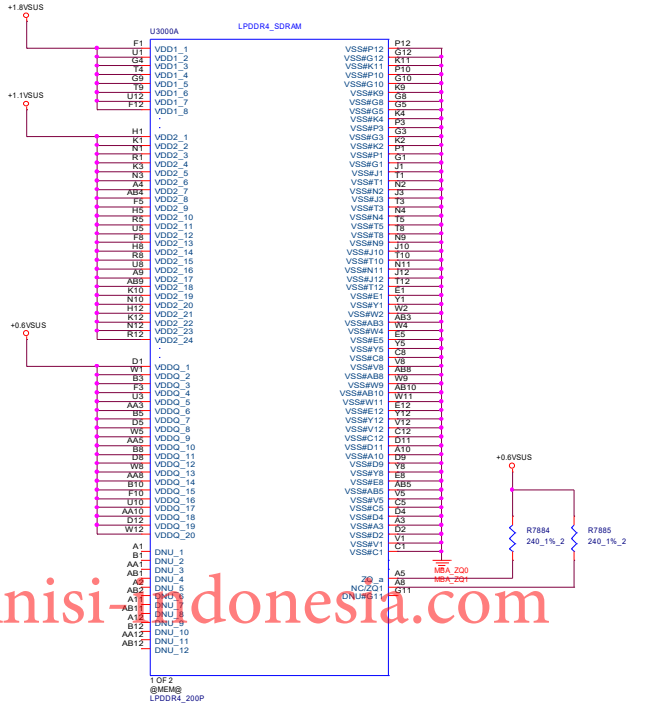


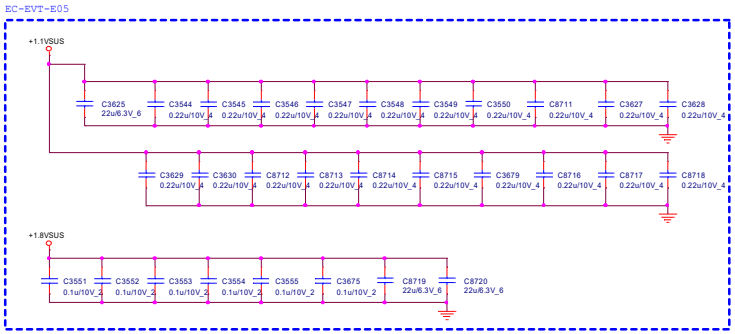
BU2	PROJECT : LS3 Quanta Computer Inc.		
	Size	Document Number LPDDR4_A Channel_Memory Down	Rev 1A
	Date: Friday, January 17, 2020	Sheet 12 of 54	

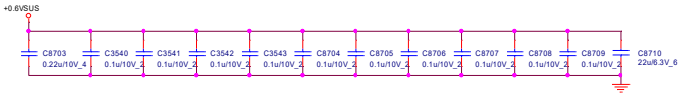
Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-MBA







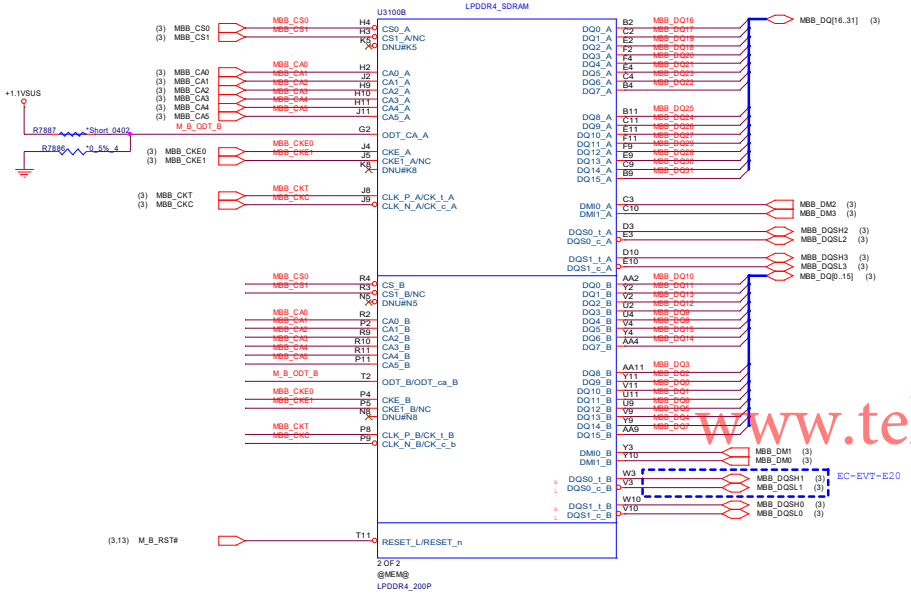


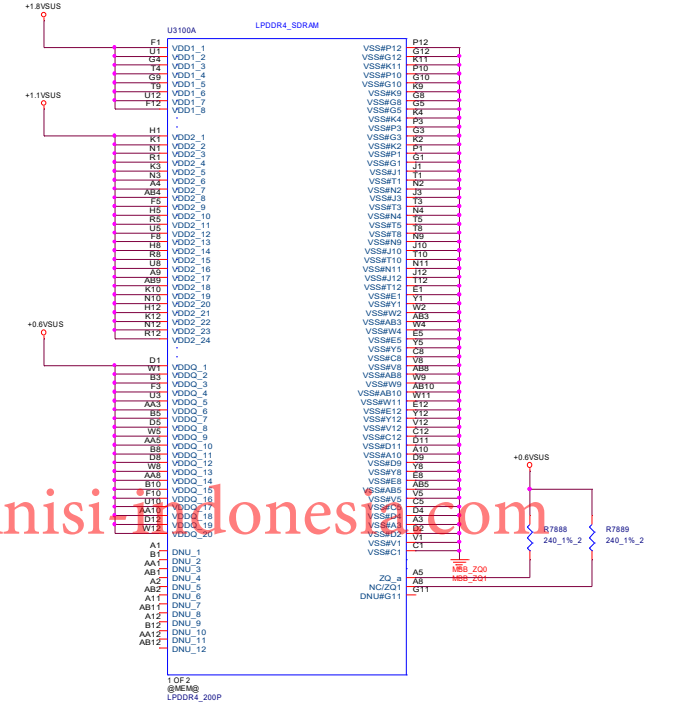
BU2	PROJECT : LS3 Quanta Computer Inc.		
	Size	Document Number LPDDR4_B Channel Memory Down	Rev 1A
	Date: Friday, January 17, 2020	Sheet 13 of 54	

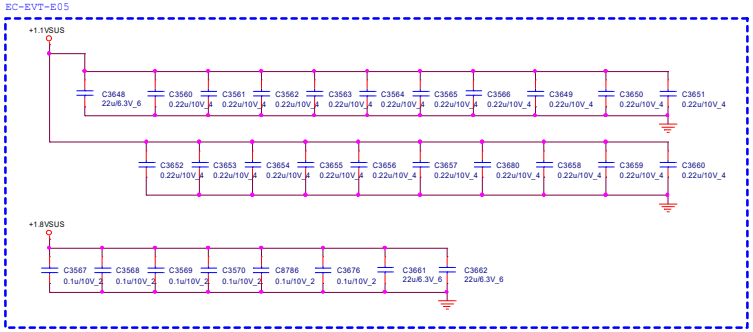
(3,9,11,12,13,39,48) +1.1VSUS
(5,6,9,16,17,19,23,24,25,27,29,30,31,32,41,47) +3V

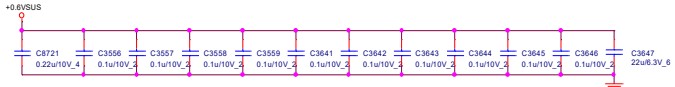
Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-MBB

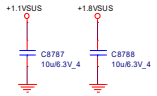








Close to Power Source

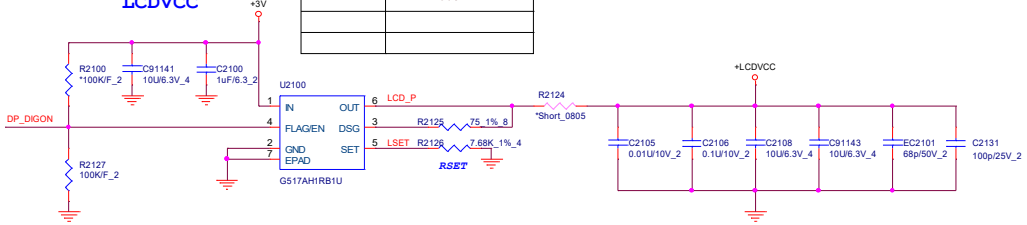


PROJECT : LS3
Quanta Computer Inc.
BU2
Size | Document Number: LPDDR4_B Channel_Memory Down | Rev: 1A
Date: Friday, January 17, 2020 | Sheet 14 of 54

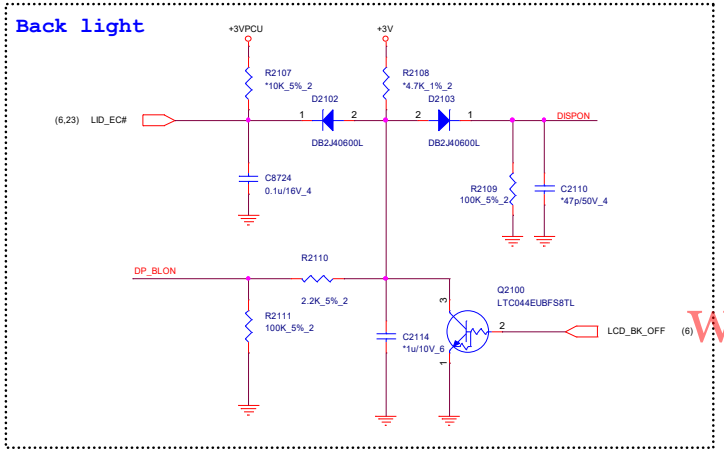
+3V (5,6,9,17,19,23,24,25,27,29,30,31,32,41,47)
+VIN (28,37,38,39,40,41,42,43,48,49)

G517AH	
RSET(KΩ)	Current Limit(A)
7.68	2.7
10.5	2
21	1
42	0.5

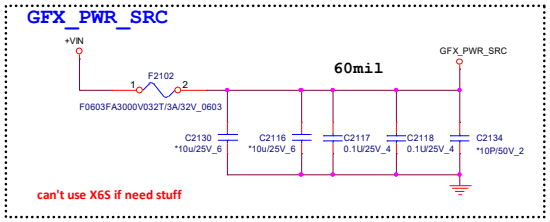
LCDVCC

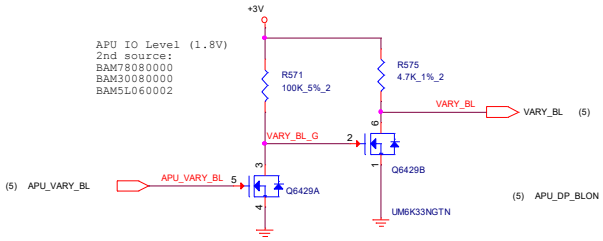


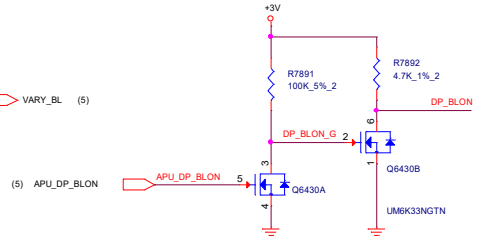
Back light

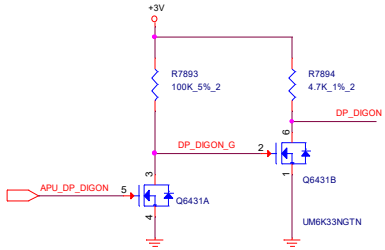


GFX_PWR_SRC

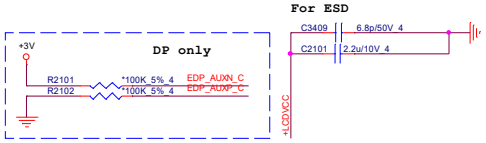




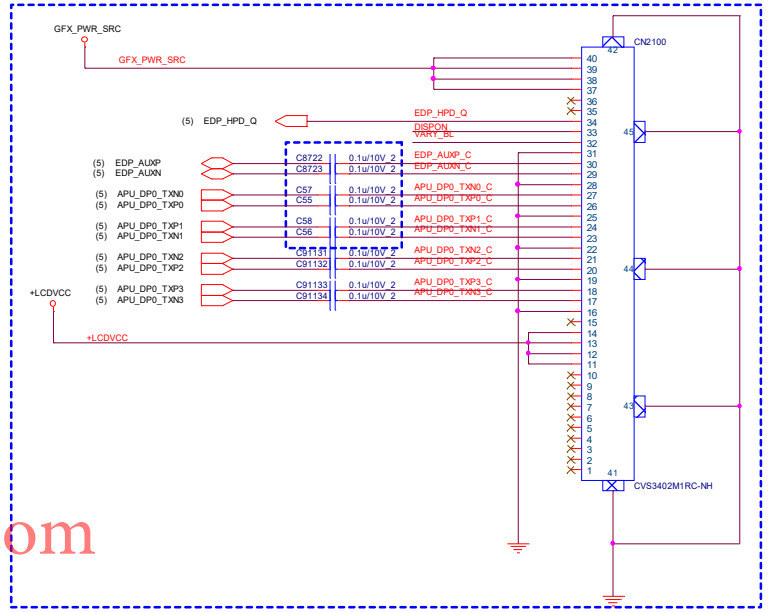




For ESD



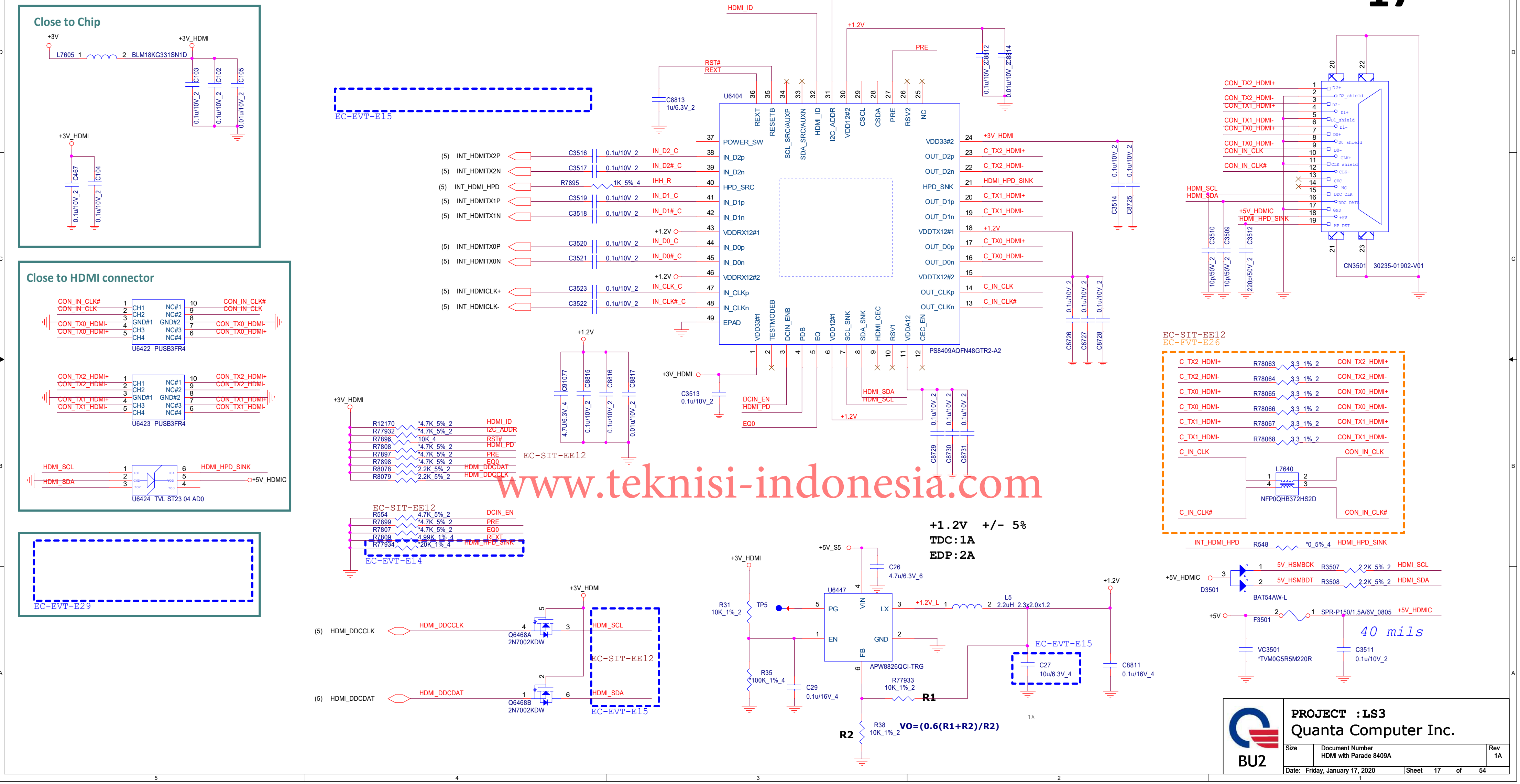
EC-EVT-E23



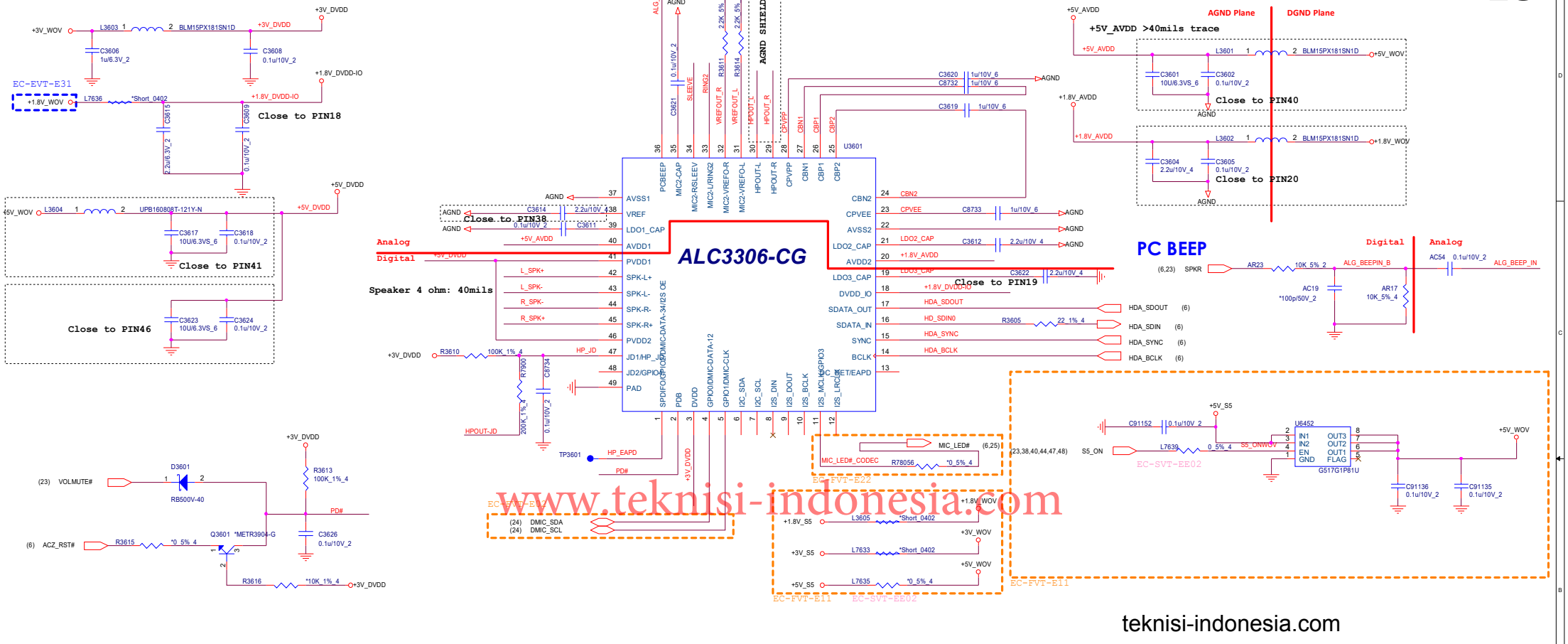
BU2

PROJECT : LS3
Quanta Computer Inc.
Size | Document Number eDP | Rev 1A
Date: Friday, January 17, 2020 | Sheet 16 of 54

HDMI with Parade 8409A



ALC3306-CG



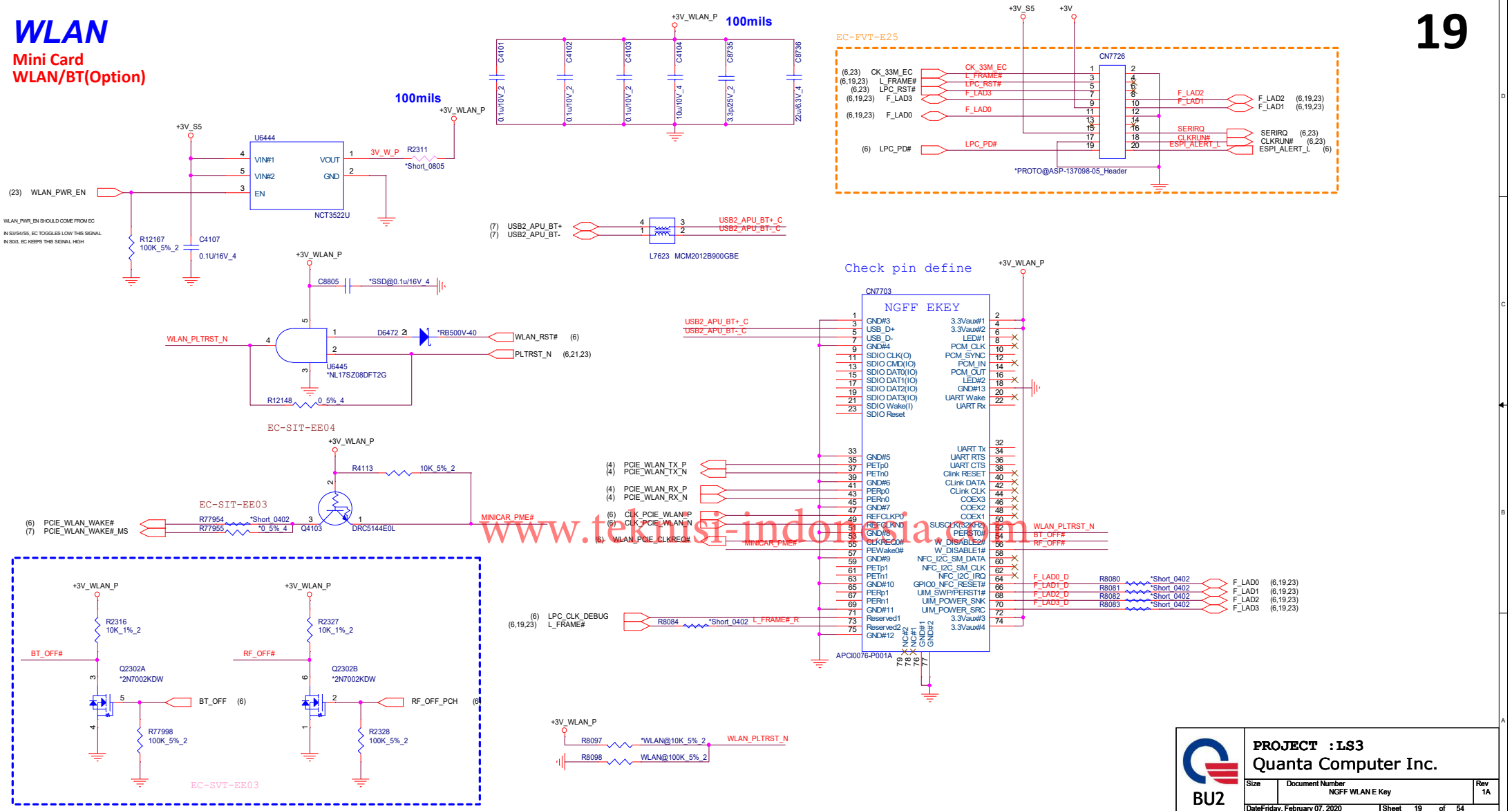
SPK CONN

Close to Speaker Speaker 4 ohm: 40mils

PROJECT	LS3
Quanta Computer Inc.	
BU2	
Size	
Document Number	Codec ALC3306
Rev	1A
Date	Friday, January 17, 2020
Sheet	18 of 54

WLAN

Mini Card
WLAN/BT(Option)



PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
BU2	NGFF WLAN E Key	1A
Date: Friday, February 07, 2020	Sheet 19 of 54	

M2SSD_PWREN SHOULD COME FROM EC

NVMe (PCIe or M.2) devices should be powered by S0 rail to reduce power consumption in MS.

SATA SSD should be powered by S5 rail as SATA SSD has DEVSLP feature to reduce power consumption.

(5,6,9,16,17,19,23,24,25,27,29,30,31,32,41,47) +3V

20

+V3DX_SDD2

+3V_SSD — R8122 *Short_0805

C8737 SSD@10u/6.3V_4
C8740 SSD@0.1u/16V_4
C8743 SSD@0.01u/50V_4

NEAR PIN 2/4

+V3DX_SDD2

C8738 SSD@10u/6.3V_4
C8741 SSD@0.1u/16V_4
C8744 SSD@0.01u/50V_4

NEAR PIN 12/14/16/18

+V3DX_SDD2

C8739 SSD@10u/6.3V_4
C8742 SSD@0.1u/16V_4
C8745 SSD@0.01u/50V_4

NEAR PIN 70/72/74

DC Current rating: 2.1 A (MAX)

CN7724

NGFF- Key M

1	GND_PRESENCE_IND	3.3Vaux	2
3	GND	3.3Vaux1	4
5	PERn3	N/C	6
7	PERp3	N/C1	8
9	GND1	DAS/DSS/LED#1(OD)	10
11	PETn3	3.3Vaux2	12
13	PETp3	3.3Vaux3	14
15	GND2	3.3Vaux4	16
17	PERn2	3.3Vaux5	18
19	PERp2	N/C2	20
21	GND3	N/C3	22
23	PETn2	N/C4	24
25	PETp2	N/C5	26
27	GND4	N/C6	28
29	PERn1	N/C7	30
31	PERp1	N/C8	32
33	GND5	N/C9	34
35	PETn1	N/C10	36
37	PETp1	DEVSLP	38
39	GND6	N/C11	40
41	PERn0/SATA-R+	N/C12	42
43	PERp0/SATA-R-	N/C13	44
45	GND7	N/C14	46
47	PETn0/SATA-T-	N/C15	48
49	PETp0/SATA-T+	PERST#	50
51	GND8	CLKREQ#	52
53	REFCLKn	PEWAKE#	54
55	REFCLKp	NC16	56
57	GND9	NC17	58
77	77	76	76
79	79		78
67	N/C18	SUSCLK(32kHz)	68
69	PEDET_OC-PCIE/GND-SATA	3.3Vaux6	70
71	GND10	3.3Vaux7	72
73	GND11	3.3Vaux8	74
75	GND12		

SSD@2280 SSD_NGFF CONN

(4) PCIE_SSD_RXN11
(4) PCIE_SSD_RXP11
(4) PCIE_SSD_TXN11
(4) PCIE_SSD_TXP11
(4) PCIE_SSD_RXN10
(4) PCIE_SSD_RXP10
(4) PCIE_SSD_TXN10
(4) PCIE_SSD_TXP10
(4) PCIE_SSD_RXN9
(4) PCIE_SSD_RXP9
(4) PCIE_SSD_TXN9
(4) PCIE_SSD_TXP9

EC-EVT-E04

(4) PCIE_SSD_RXP8
(4) PCIE_SSD_RXN8
(4) PCIE_SSD_TXN8
(4) PCIE_SSD_TXP8
(6) CLK_PCIE_SSD2_N
(6) CLK_PCIE_SSD2_P

+V3DX_SDD2

EC-EVT-E04 R7908 100K_5%_2

SSD_DET2

(6) SSD_DET2

SSD_DET2:
SSD_PCIE IF => Low

+V3DX_SDD2

+V3DX_SDD2

+V3DX_SDD2

EC-EVT-E16

+V3DX_SDD2 — R77993 *10K_5%_2 — DEVSLP0 (6)

DEVSLP[0] can be used for SATA Port 0 or 2.

SSD2_PLTRST_N

PCIE_SSD2_CLKREQ0# (6)

+V3DX_SDD2

+V3DX_SDD2

SSD2_PLTRST_N — R12087 *Short_0402 — SSD_PLTRST_N (21)

BU2

PROJECT :LS3

Quanta Computer Inc.

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	NGFF SSD M Key	1A

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M2SSD_PWREN SHOULD COME FROM EC

NVMe (PCIe or M.2) devices should be powered by S0 rail to reduce power consumption in MS.

SATA SSD should be powered by S5 rail as SATA SSD has DEVSLP feature to reduce power consumption.

(5,6,9,16,17,19,23,24,25,27,29,30,31,32,41,47) +3V

21

+V3DX_SDD
+3V_SSD R8121 *Short_0805
C3 SSD@10u/6.3V_4
C182 SSD@0.1u/16V_4
C127 SSD@0.01u/50V_4
NEAR PIN 2/4

+V3DX_SDD
C4 SSD@10u/6.3V_4
C176 SSD@0.1u/16V_4
C126 SSD@0.01u/50V_4
NEAR PIN 12/14/16/18

+V3DX_SDD
C5 SSD@10u/6.3V_4
C130 SSD@0.1u/16V_4
C129 SSD@0.01u/50V_4
NEAR PIN 70/72/74

DC Current rating: 2.1 A (MAX)

CN3 NGFF- Key M

1	GND_PRESENCE_IND	3.3Vaux	2
3	GND	3.3Vaux1	4
5	PERn3	N/C	6
7	PERp3	N/C1	8
9	GND1	DAS/DSS/LED#1(OD)	10
11	PETn3	3.3Vaux2	12
13	PETp3	3.3Vaux3	14
15	GND2	3.3Vaux4	16
17	PERn2	3.3Vaux5	18
19	PERp2	N/C2	20
21	GND3	N/C3	22
23	PETn2	N/C4	24
25	PETp2	N/C5	26
27	GND4	N/C6	28
29	PERn1	N/C7	30
31	PERp1	N/C8	32
33	GND5	N/C9	34
35	PETn1	N/C10	36
37	PETp1	DEVSLP	38
39	GND6	N/C11	40
41	PERn0/SATA-R+	N/C12	42
43	PERp0/SATA-R-	N/C13	44
45	GND7	N/C14	46
47	PETn0/SATA-T-	N/C15	48
49	PETp0/SATA-T+	PERST#	50
51	GND8	CLKREQ#	52
53	REFCLKn	PEWAKE#	54
55	REFCLKp	NC16	56
57	GND9	NC17	58
77	77	76	76
79	79		78
67	N/C18	SUSCLK(32kHz)	68
69	PEDET_OC-PCIE/GND-SATA	3.3Vaux6	70
71	GND10	3.3Vaux7	72
73	GND11	3.3Vaux8	74
75	GND12		

SSD@2280 SSD_NGFF CONN

(4) PCIE_SSD_RXN0
(4) PCIE_SSD_RXP0
(4) PCIE_SSD_TXN0
(4) PCIE_SSD_TXP0
(4) PCIE_SSD_RXN1
(4) PCIE_SSD_RXP1
(4) PCIE_SSD_TXN1
(4) PCIE_SSD_TXP1
(4) PCIE_SSD_RXN2
(4) PCIE_SSD_RXP2
(4) PCIE_SSD_TXN2
(4) PCIE_SSD_TXP2
EC-EVT-E04
(4) PCIE_SSD_RXP3
(4) PCIE_SSD_RXN3
(4) PCIE_SSD_TXN3
(4) PCIE_SSD_TXP3
(6) CLK_PCIE_SSD_N
(6) CLK_PCIE_SSD_P

+V3DX_SDD
EC-EVT-E04
R539 100K_5%_2
SSD_DET1
(6) SSD_DET1

SSD_DET1:
SSD_PCIE IF => Low

+V3DX_SDD
+V3DX_SDD
+V3DX_SDD

EC-EVT-E16
+V3DX_SDD
R77994 *10K_5%_2
DEVSLP1 (6)
DEVSLP[1] can be used for SATA Port 1 or 3

SSD_PLTRST_N
PCIE_SSD_CLKREQ0# (6)

+V3DX_SDD
R467 SSD@10K_5%_2 +V3DX_S0I3

+V3DX_SDD
C429 SSD@0.1u/16V_4

(20) SSD_PLTRST_N
SSD_PLTRST_N
R468 *SSD@100K_5%_2
U6425 NL17SZ08DFT2G
SSD_RST# (6)
+V3DX_S0I3 R78050 *0_5%_4 PLTRST_N (6,19,23)
R12149 *0_5%_4

EC-FVT-E20

BU2

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Quanta Computer Inc.

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	NGFF SSD M Key	1A
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Quanta Computer Inc.	PROJECT : LS3	
Custom <Doc>	Size: BU2	Document Number: 1A	Rev
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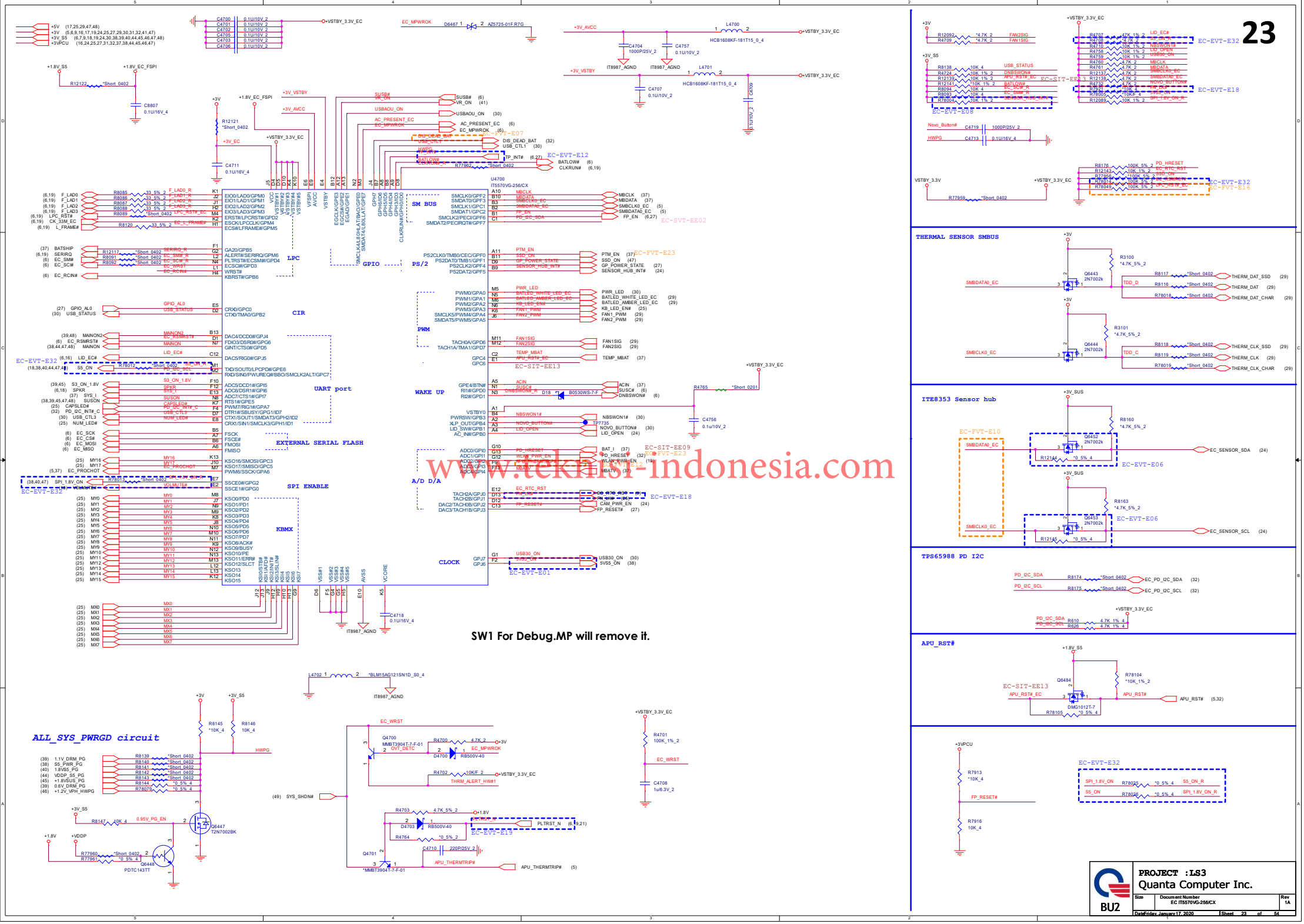
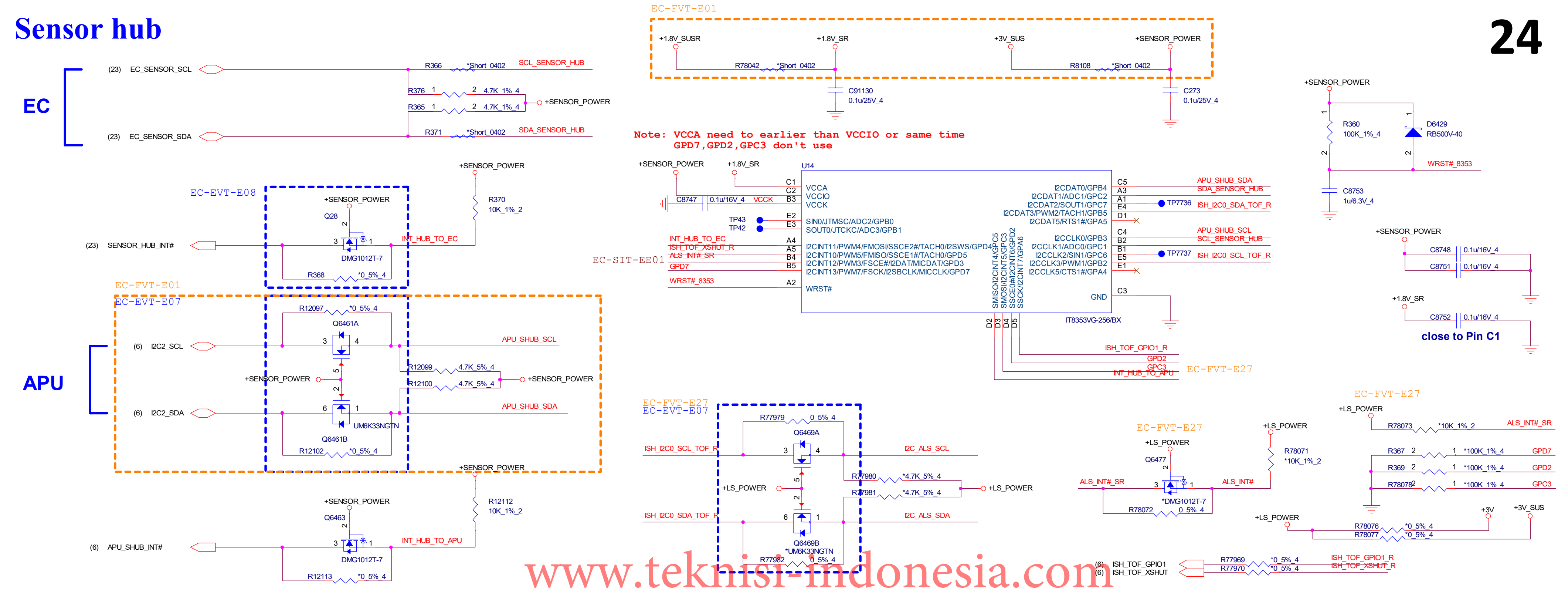
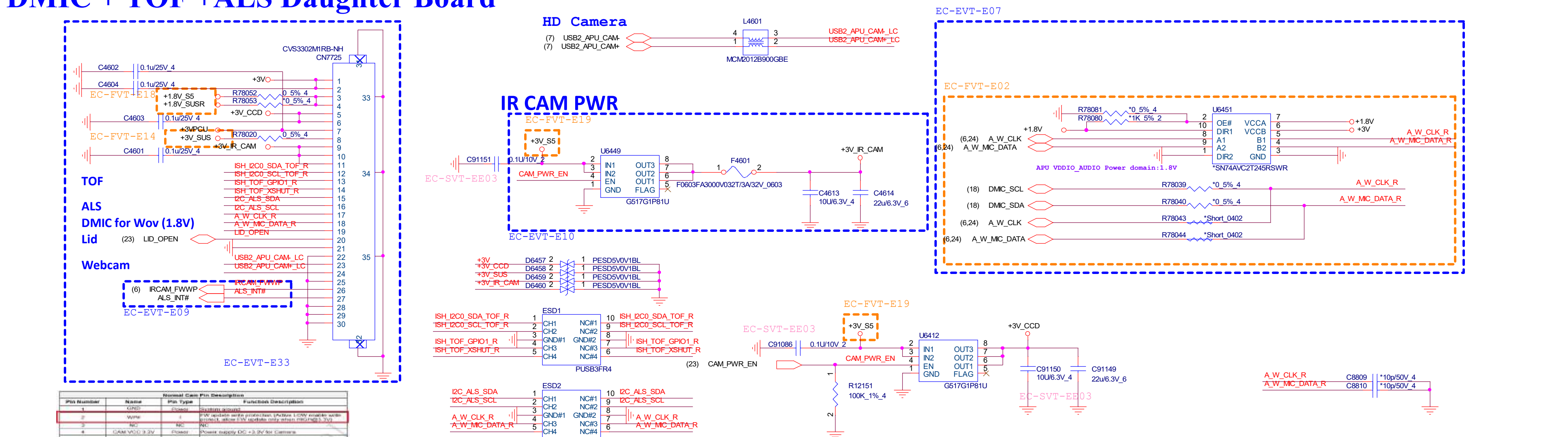


Sensor hub



DMIC + TOF +ALS Daughter Board



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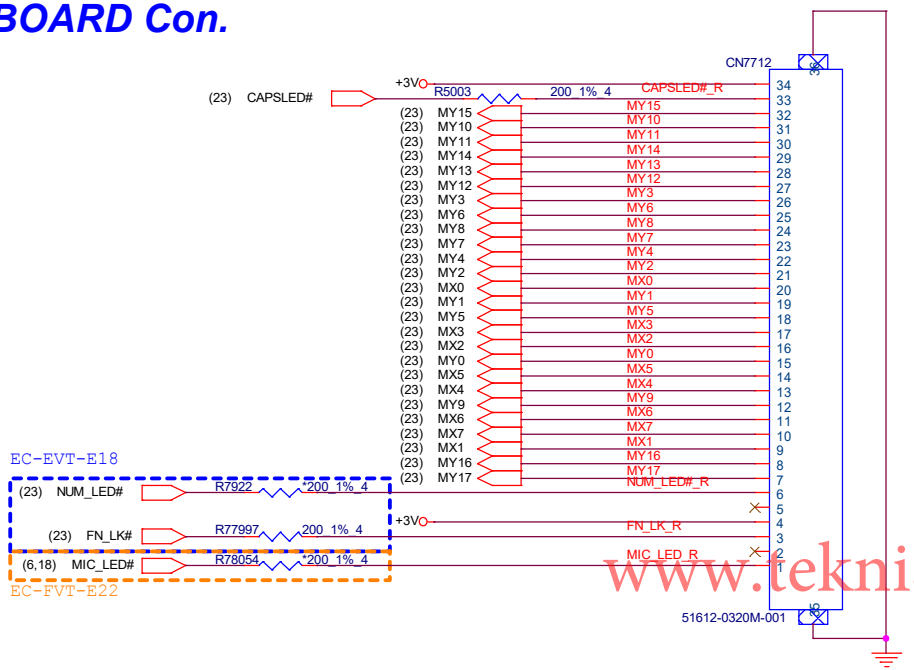
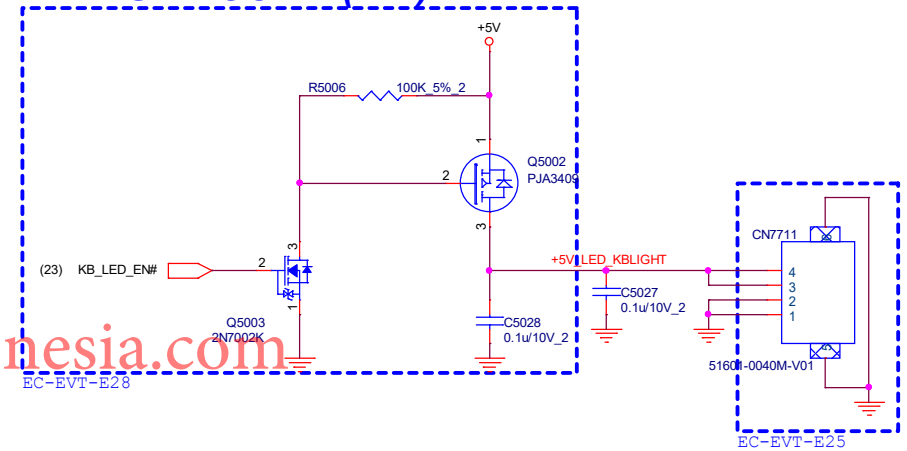
Quanta Computer Inc.	
Size	Document Number: TOF/ALS/LID/SENSOR_HUB	Rev 1A
Date: Tuesday, February 04, 2020	Sheet 24 of 54

+3V_S5 (6,7,9,18,19,23,24,30,38,39,40,44,45,46,47,48)
+3V (5,6,9,16,17,19,23,24,27,29,30,31,32,41,47)
+5V_S5 (17,18,27,29,30,32,38,41,42,45,47)

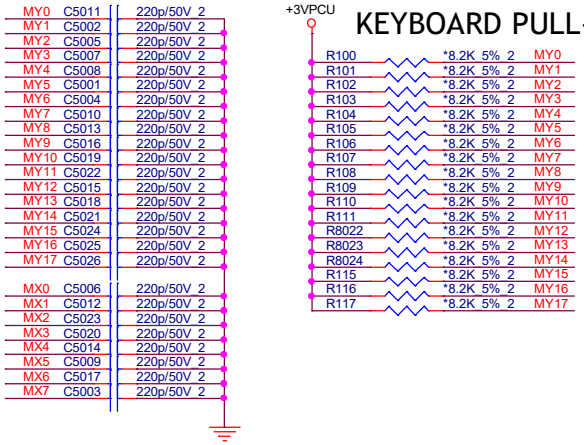
KEYBOARD Con.



KB LIGHT CONN (14")



KEYBOARD PULL-UP



BU2

PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
	Kerboard/Keyboard Backlight	1A
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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discrete TPM	1A
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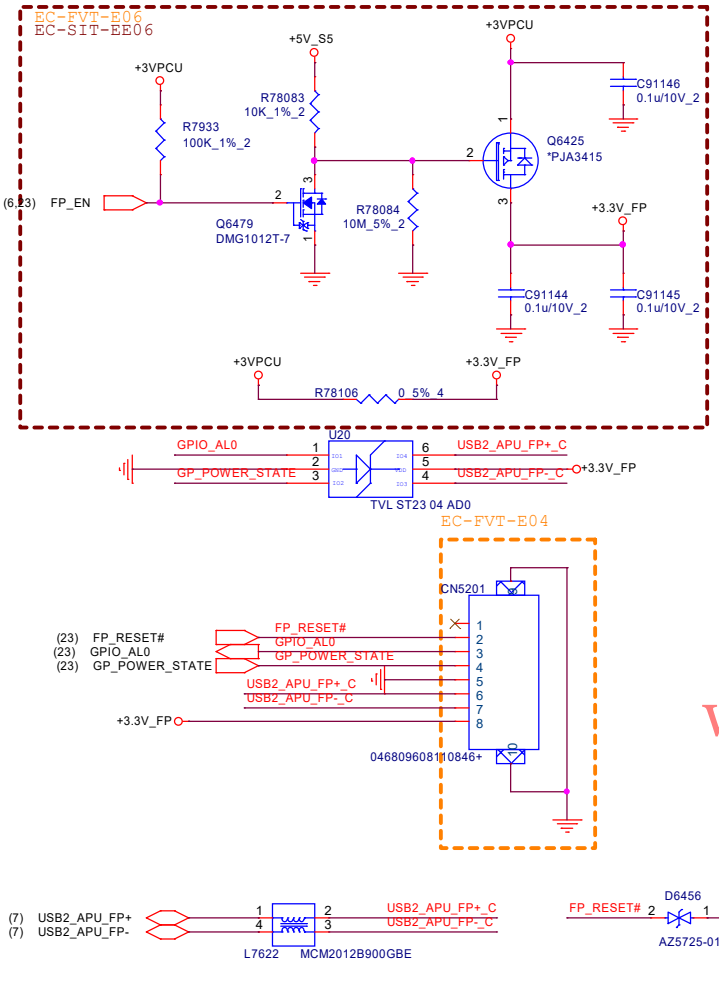
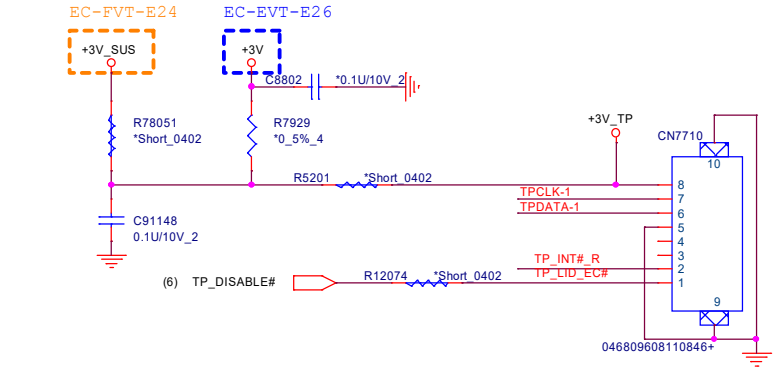
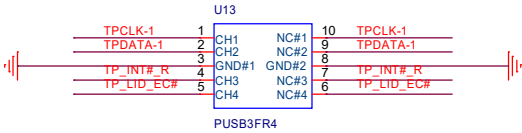
Finger print

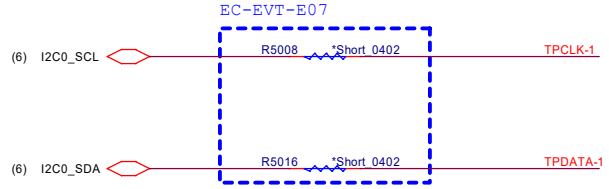


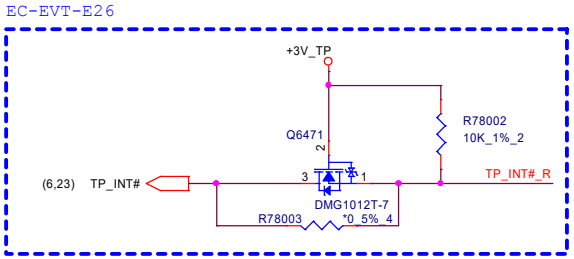
Pin No.	Symbol	Description
1	LED	LED SINGNAL
2	RESETN	MCU RESETN SINGAL
3	GPIO_AL0	POWER SHIELD
4	DELINK	POWER STATUS
5	DGND	GROUND
6	DP	USB DATA+
7	DM	USB DATA-
8	D3V3	POWER 3.3V

Touch Pad









Pin Number	Pin Name	Description
1	VDD	Power
2	I2C-CLK	I2C Clock
3	I2C-DAT	I2C Data
4	GND	Ground
5	NC	NC
6	NC	NC
7	ATTN	Attention
8	GPIO for LID CLOSE	LID Close

BU2

PROJECT : LS3

Quanta Computer Inc.

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	Touch Pad/Fingerprint	1A

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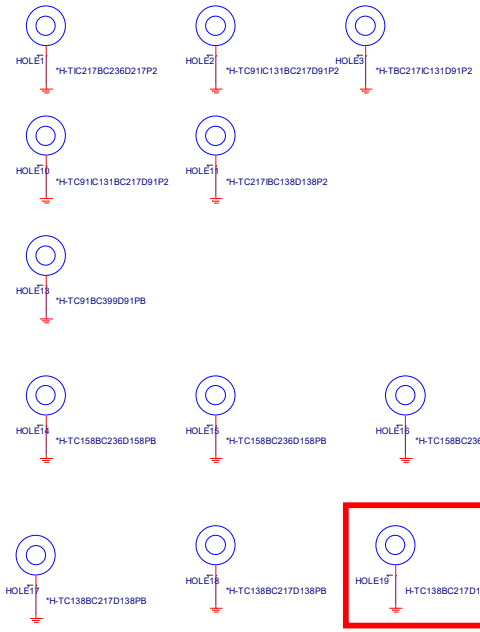
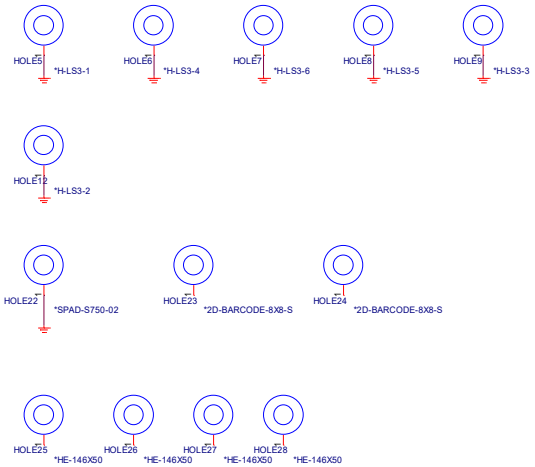
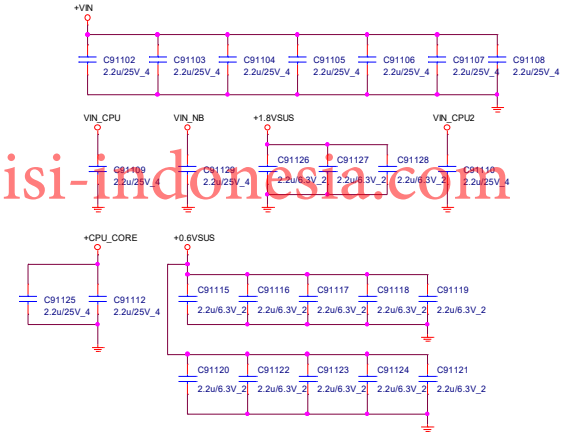
HOLE



WLAN Nut

SSD Nut

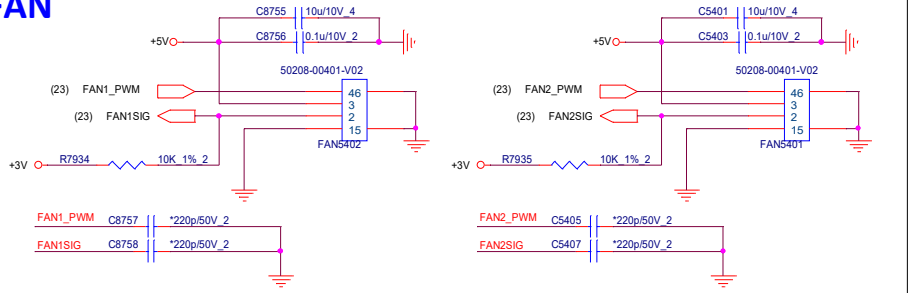




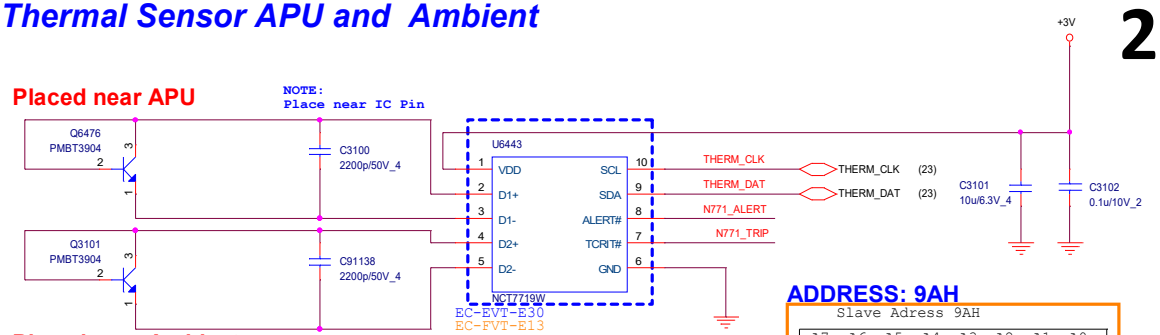
PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HOLE	1A
BU2	Date: Friday, January 17, 2020	Sheet 60

FAN



Thermal Sensor APU and Ambient

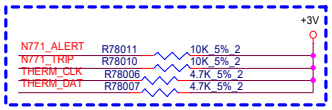


ADDRESS: 9AH

Slave Adress 9AH

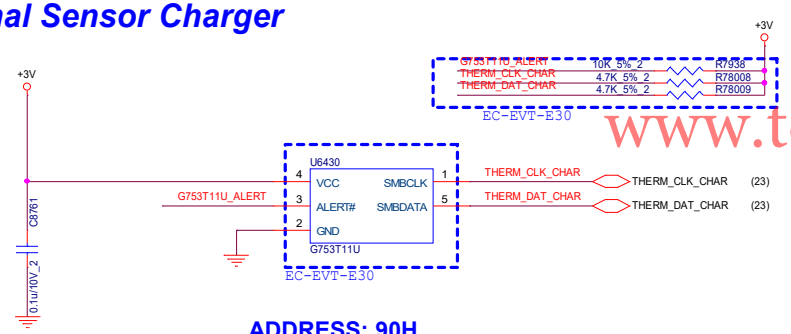
A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	1	0	1	0

EC-EVT-E30



GMT	G753T11U		90h	AL000753000
Nuvoton	NCT7719W	SMBus Address	9Ah	AL007719000
GMT	G751-2P8F	SMBus Address	92h	AL000751016
GMT	G781-1P8	SMBus Address	9Ah	AL000781039

Thermal Sensor Charger

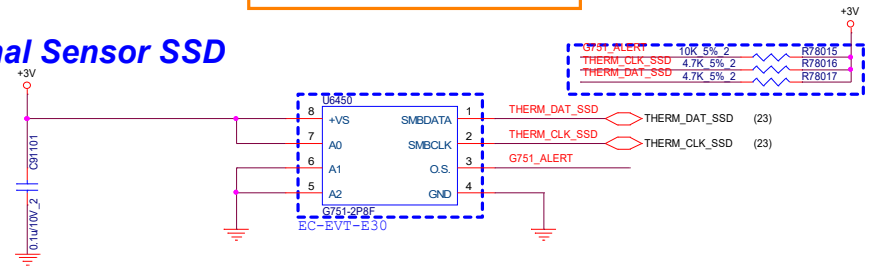


ADDRESS: 90H

Slave Adress 90H

A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	0	0	0	0

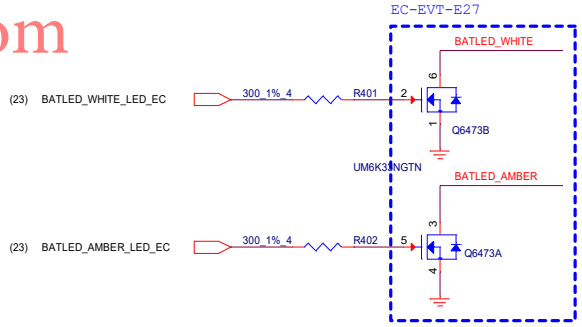
Thermal Sensor SSD

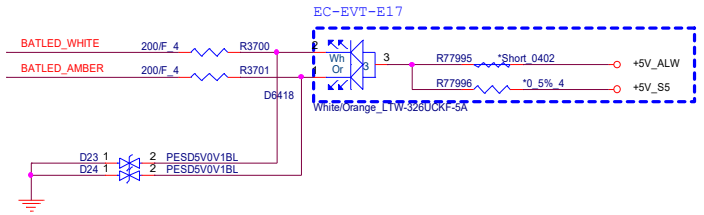


ADDRESS: 92H

Slave Adress 92H

						A2	A1	A0
1	0	0	1	0	0	1	0	





BU2

PROJECT : LS3

Quanta Computer Inc.

Size	Document Number	Rev
	FAN/Thermal Sensor	1A

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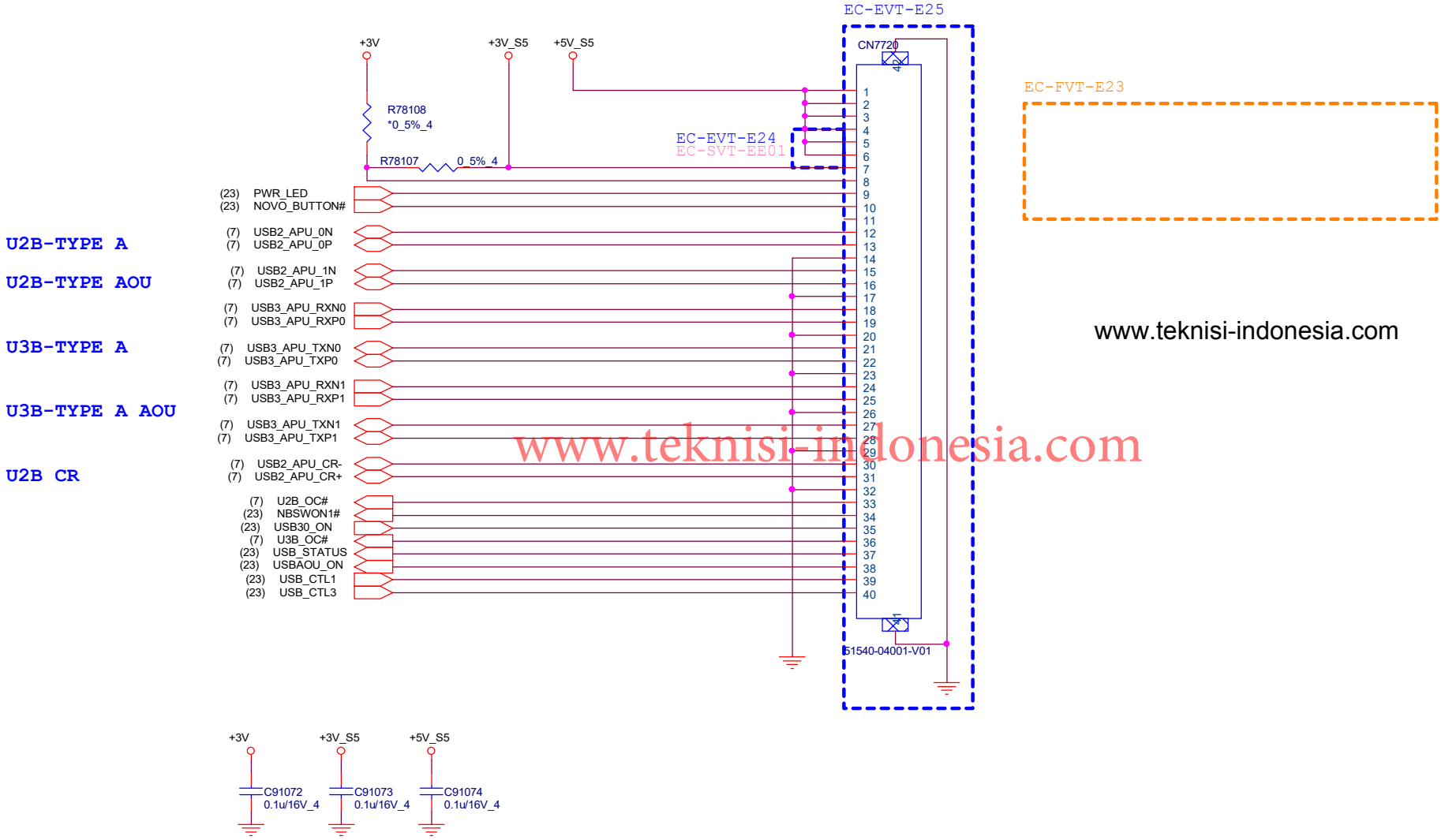
USB3+SD Daughter Board



Custom BU2	PROJECT : LS3 Quanta Computer Inc.	
	Size: Document Number: USB3+SD Daughter Board conn	Rev: 1A
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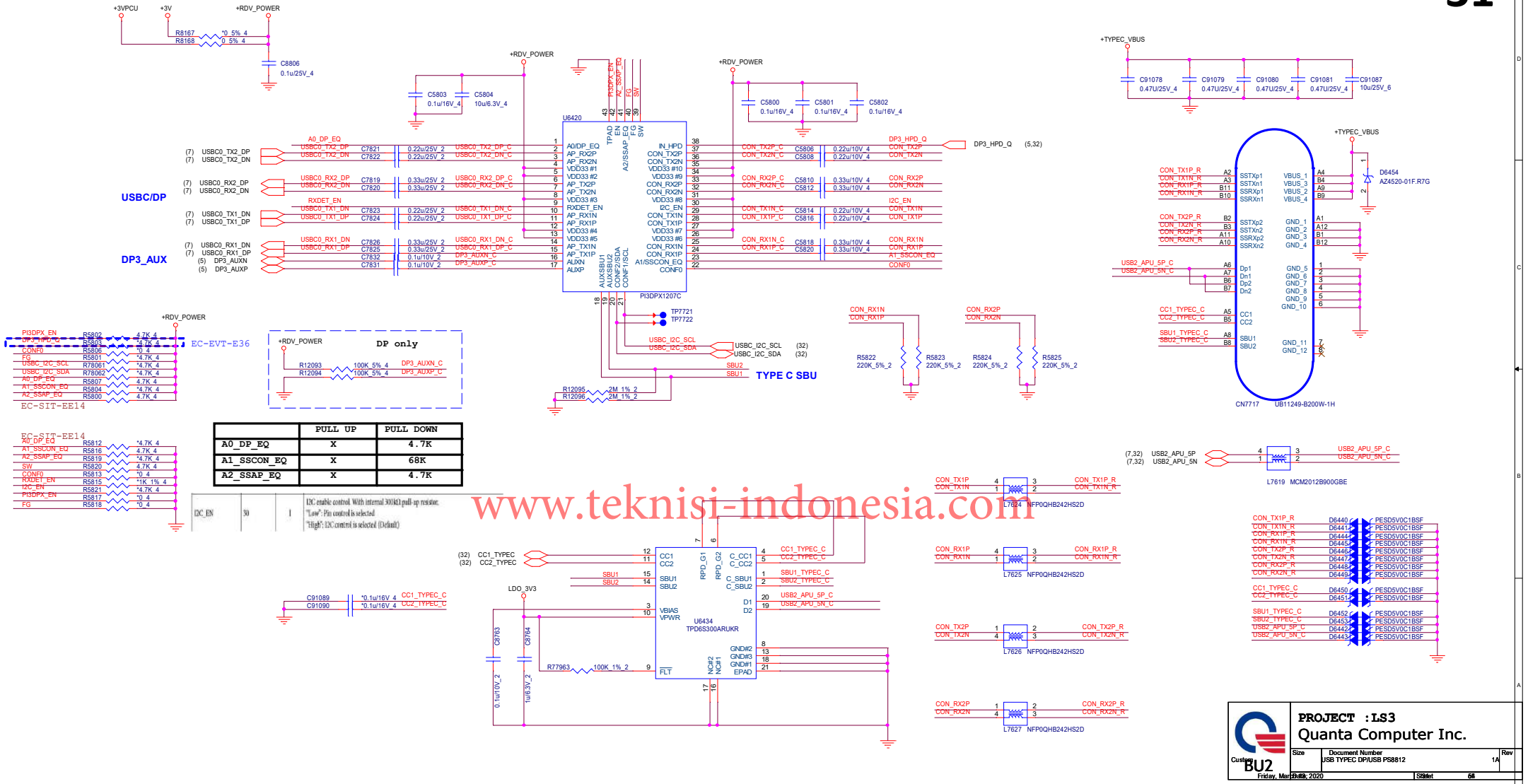

	PULL UP	PULL DOWN
A0_DP_EQ	X	4.7K
A1_SSCON_EQ	X	68K
A2_SSAP_EQ	X	4.7K

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Quanta Computer Inc.
Custom BU2
Size
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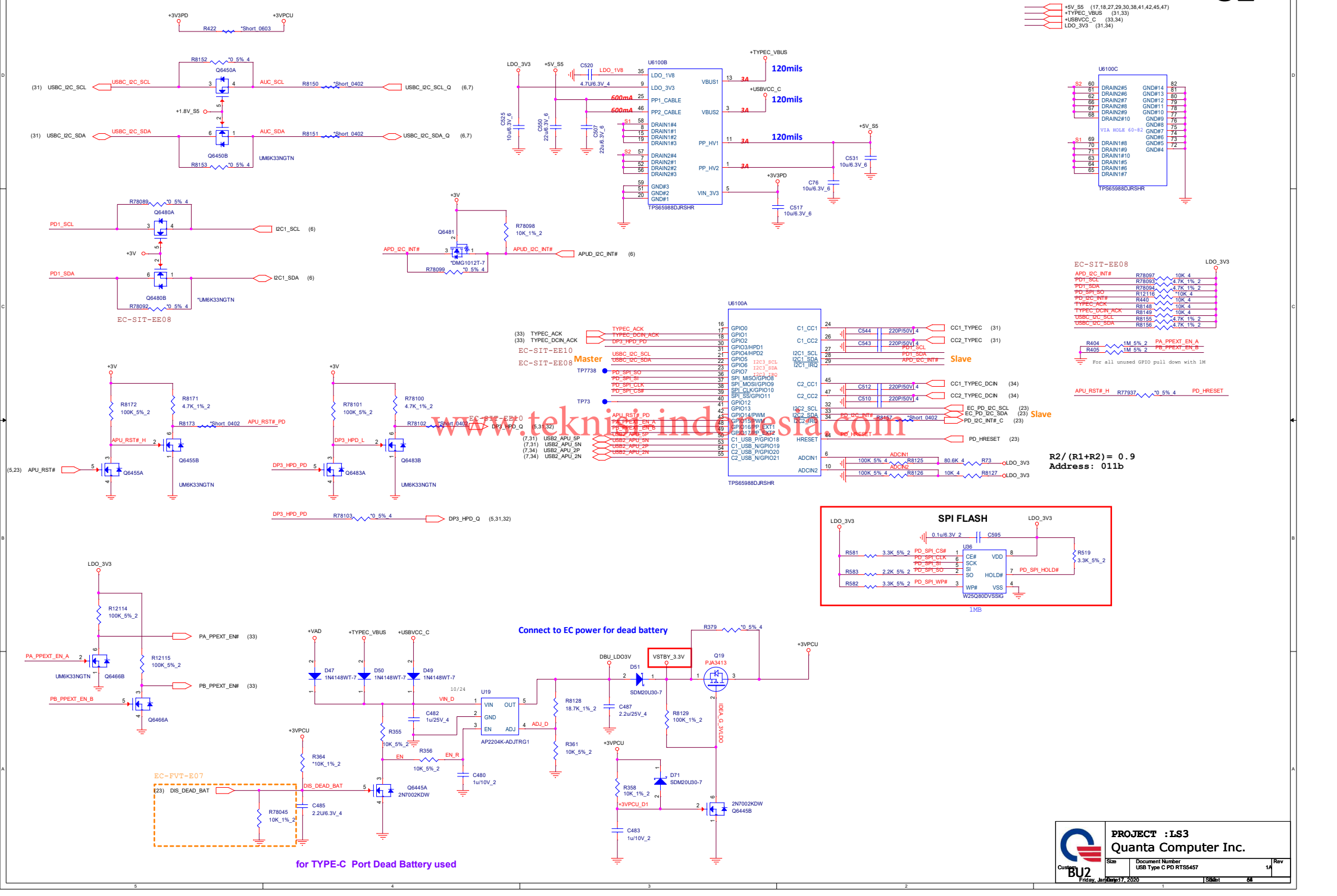
USB TYPEC DP/USB PS8812
Rev 1A
Friday, March 13, 2020
Sheet 68

USB TYPEC PD



TYPE-C Load Switch

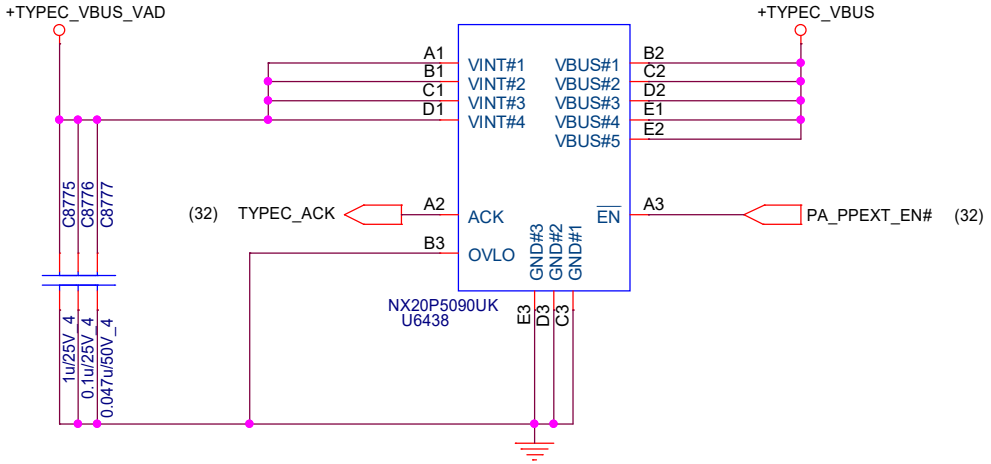
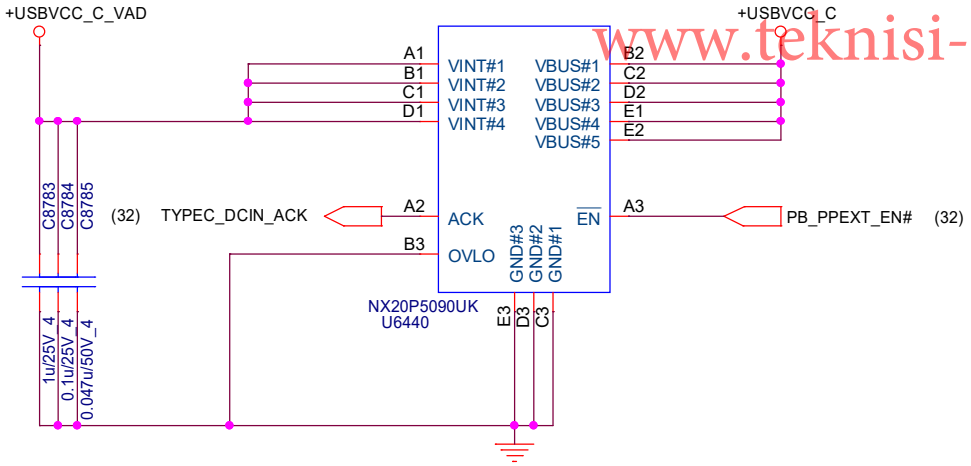


Table 4. Function table[1]

$\overline{EN}$	VBUS	VINT	ACK	Operation mode
L	< 2.5 V	X	Z	Under-voltage lockout; switch open
L	2.5 V < VBUS < V_{OVLO}	X	L	Enabled; switch closed; charging mode
L	X	X	Z	Over-temperature protection; switch open
L	> V_{OVLO}	X	Z	Over-voltage lockout; switch open
H	X	X	Z	Disable; switch open
X	X	VINT>VBUS	Z	Reverse Current Protection; Switch open

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state.

TYPE-C ADP Load Switch



8.5 ACK output

The ACK output is an open-drain output that requires an external pull-up resistor. ACK pin indicates the state of the power switch, when no fault is detected and power switch is conducting, ACK will output low, otherwise it will stay at high impedance. The pull up resistor value is recommend to be 10KΩ to 200KΩ.

BU2

PROJECT : LS3

Quanta Computer Inc.

Size	Document Number	Rev
	Load Switch for Power Delivery	1A
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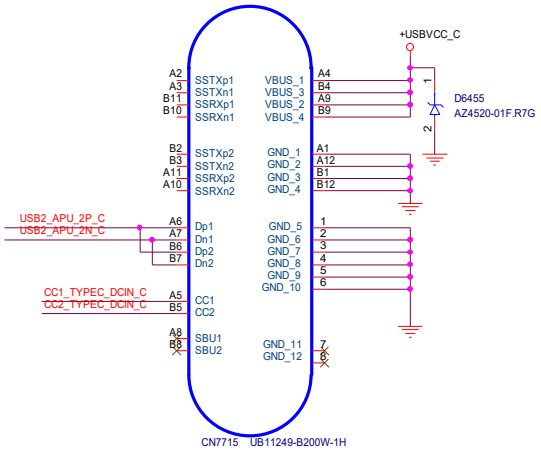
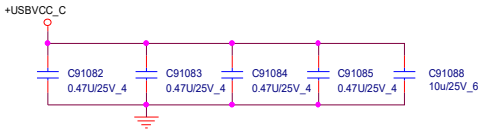
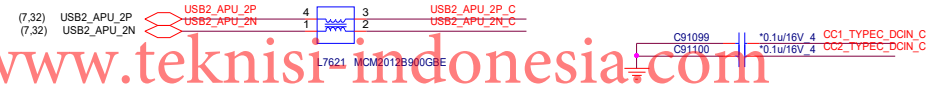
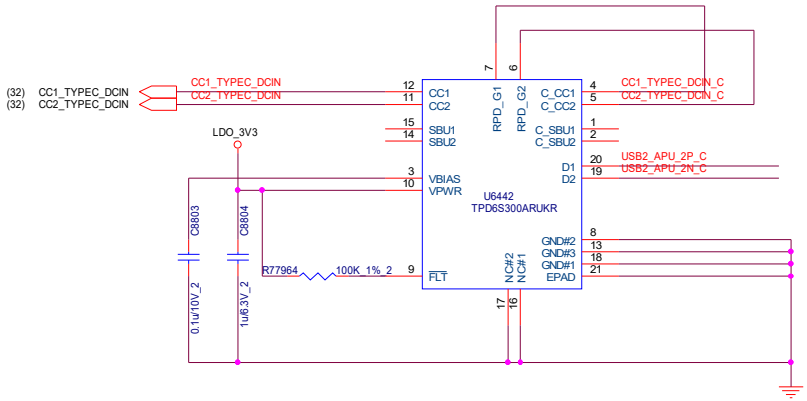
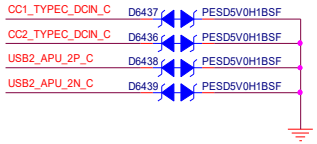
USB TYPEC PD-DCIN ONLY











PROJECT : LS3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB Type C PD RTS5457	1A
BU2		
Friday, January 17, 2020	Sheet 58	

TYPE-C ADP Load Switch

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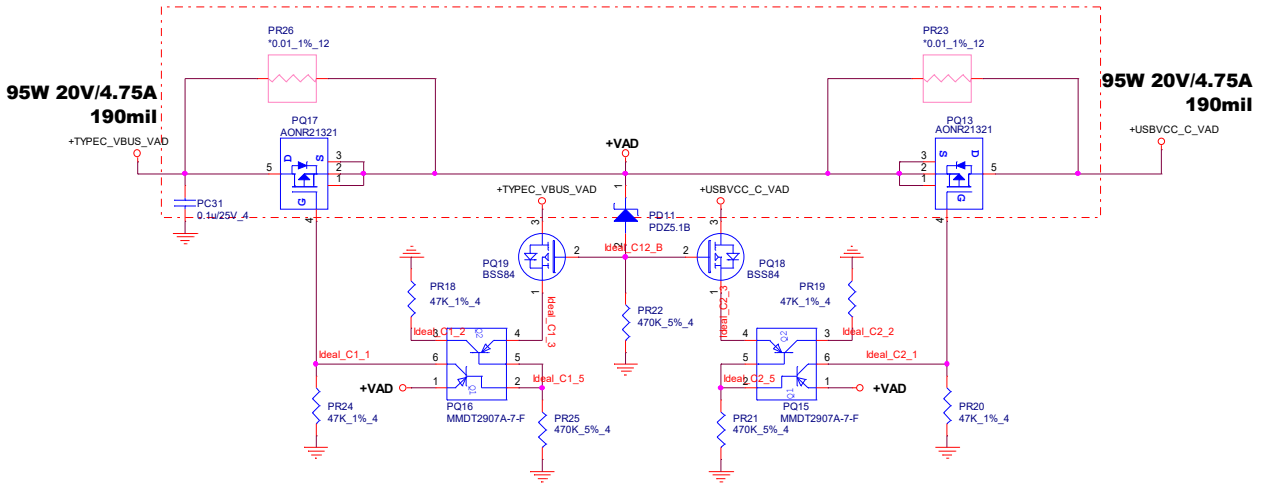
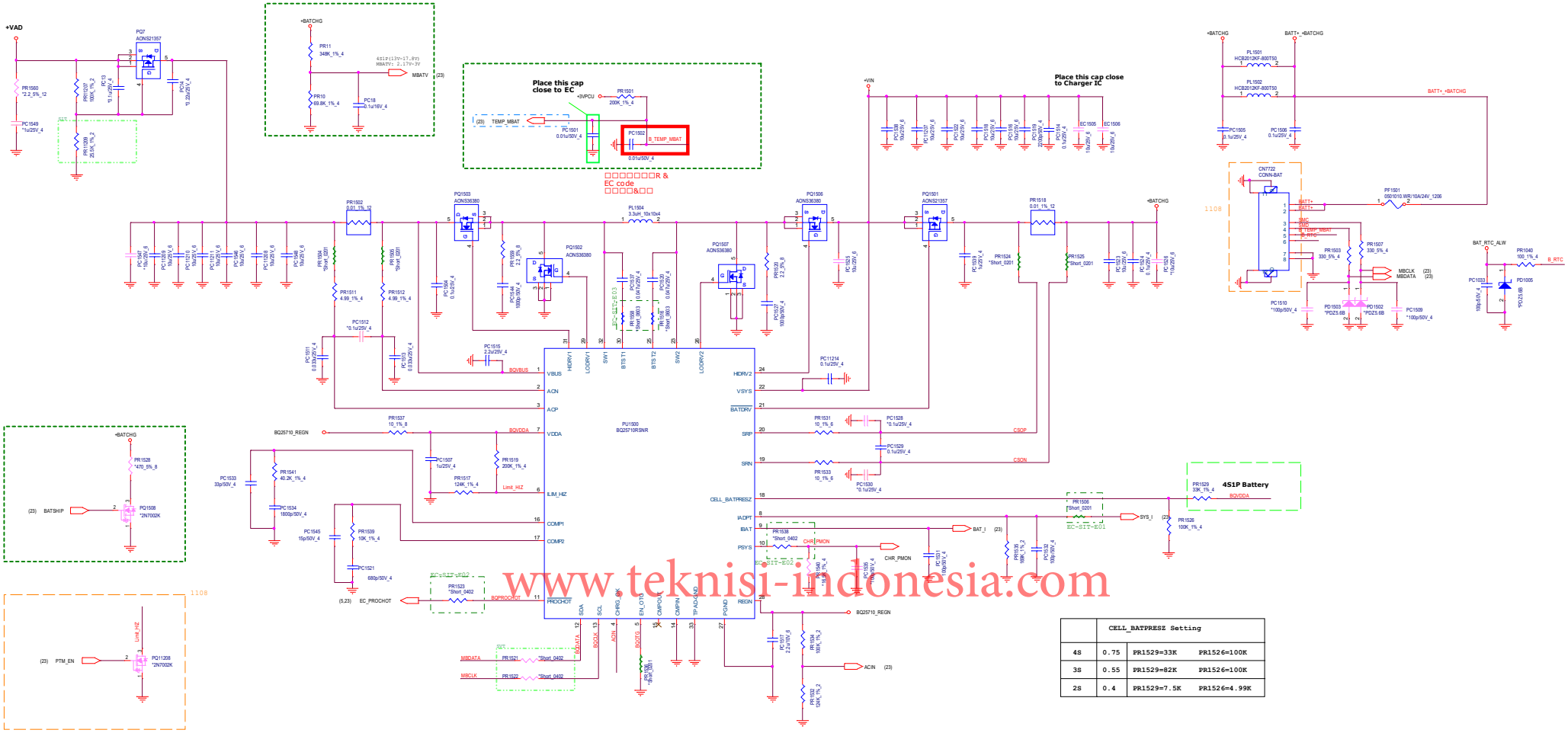
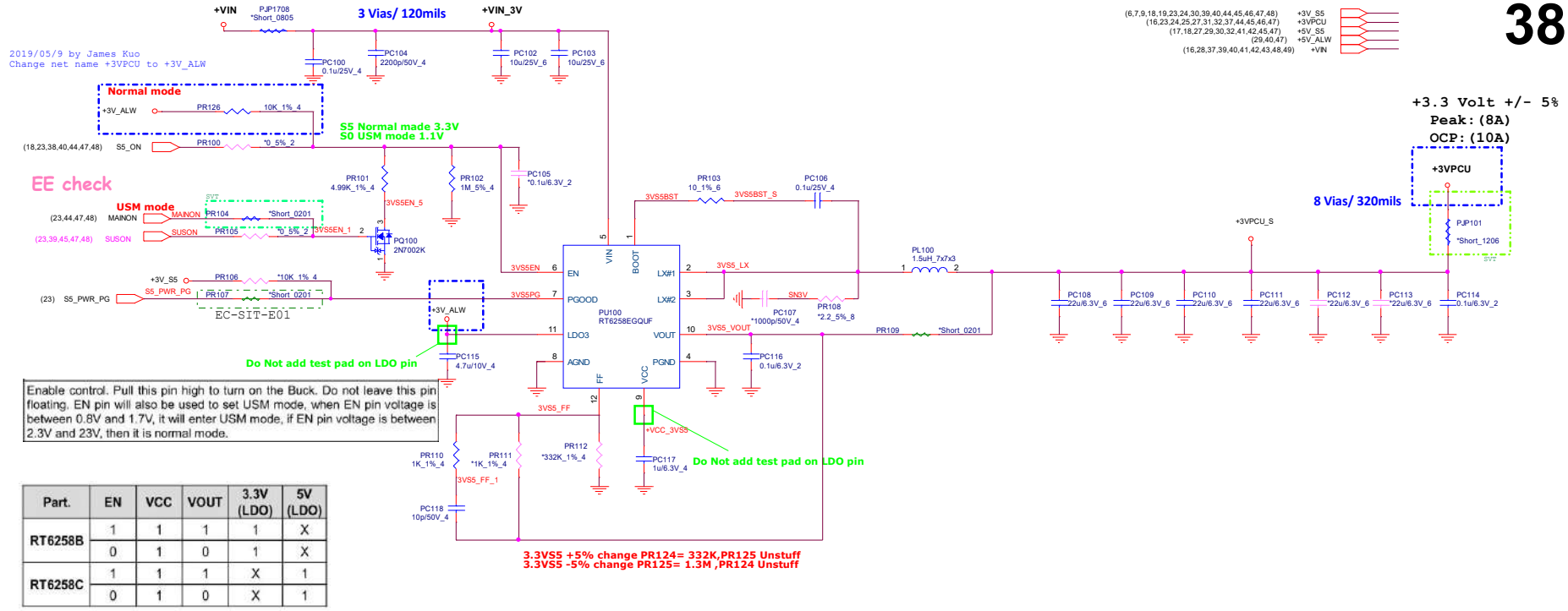
A	BU2	PROJECT : LS3 Quanta Computer Inc.
Size	Document Number TYPE-C ADP Load Switch	Rev 1A
Date: Friday, January 17, 2020	Sheet 35 of 51	



BU5	PROJECT : X36A Quanta Computer Inc.	
Size: Custom	Document Number: TYPEC load switch MOSFET	Rev: 1A
Date: Friday, January 17, 2020	Sheet: 36 of 54	



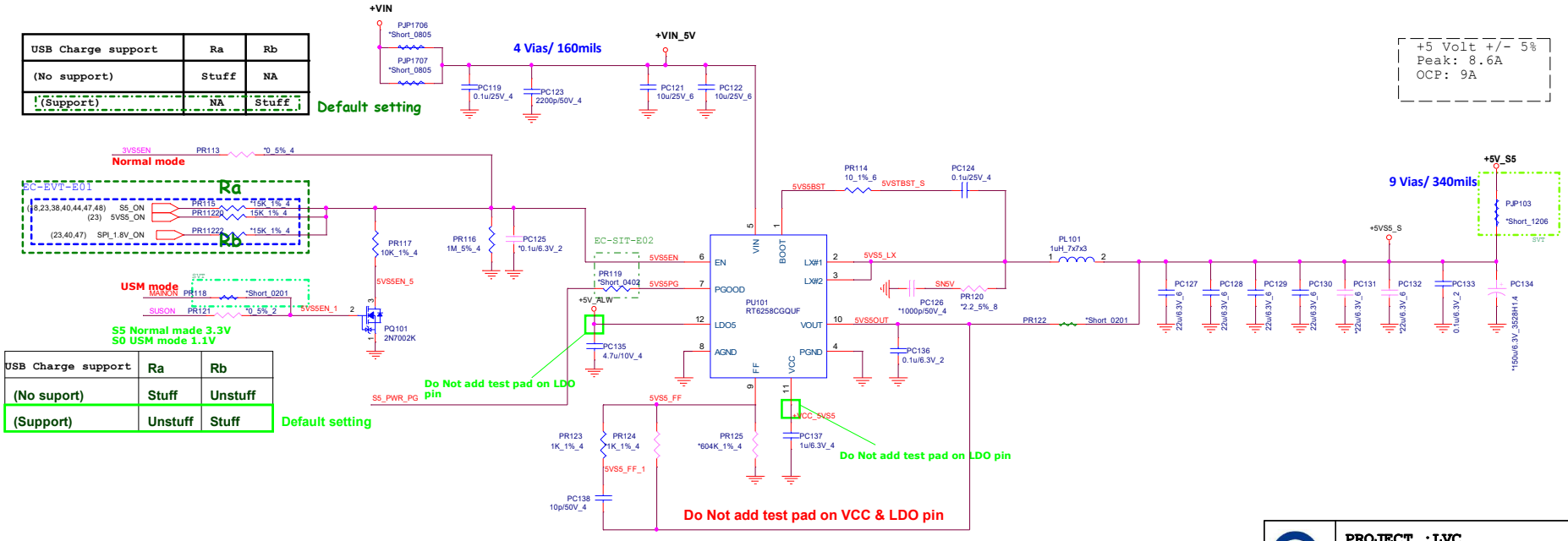
PROJECT : LVC
Quanta Computer Inc.
Size: BU2
Document Number: Charger (BQ25710RSNR)
Rev: 1A
Friday, January 17, 2020
Sheet: 48



Part.	EN	VCC	VOUT	3.3V (LDO)	5V (LDO)
RT6258B	1	1	1	1	X
	0	1	0	1	X
RT6258C	1	1	1	X	1
	0	1	0	X	1

USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

Default setting



USB Charge support	Ra	Rb
(No suport)	Stuff	Unstuff
(Support)	Unstuff	Stuff

Default setting

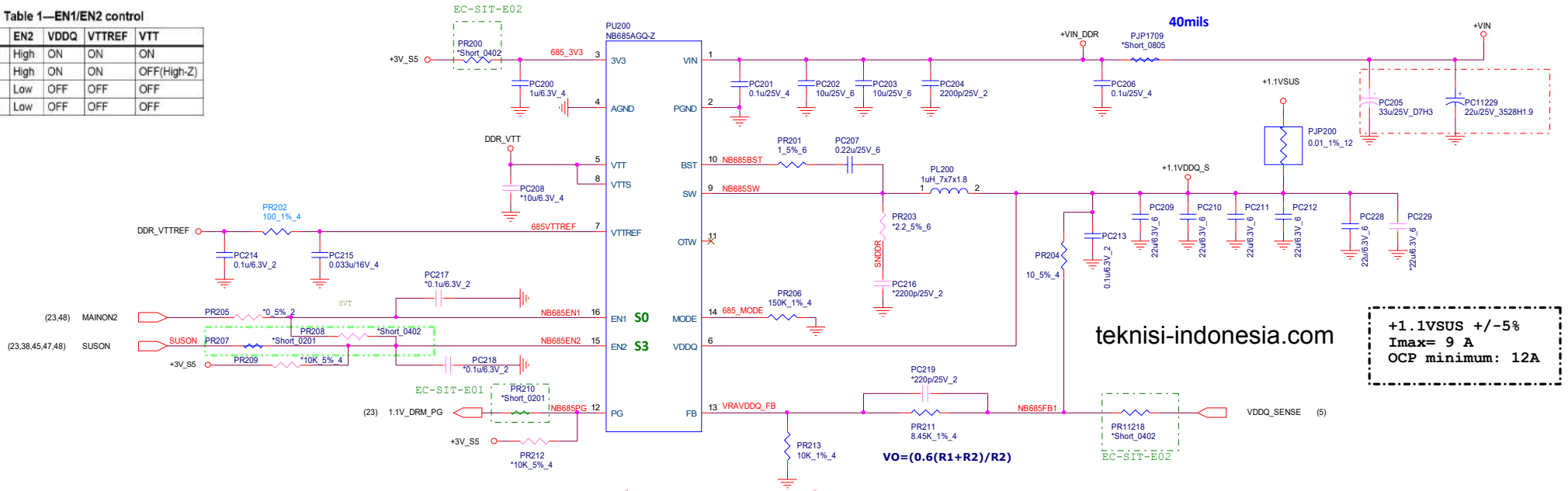
PROJECT :LVC
Quanta Computer Inc.

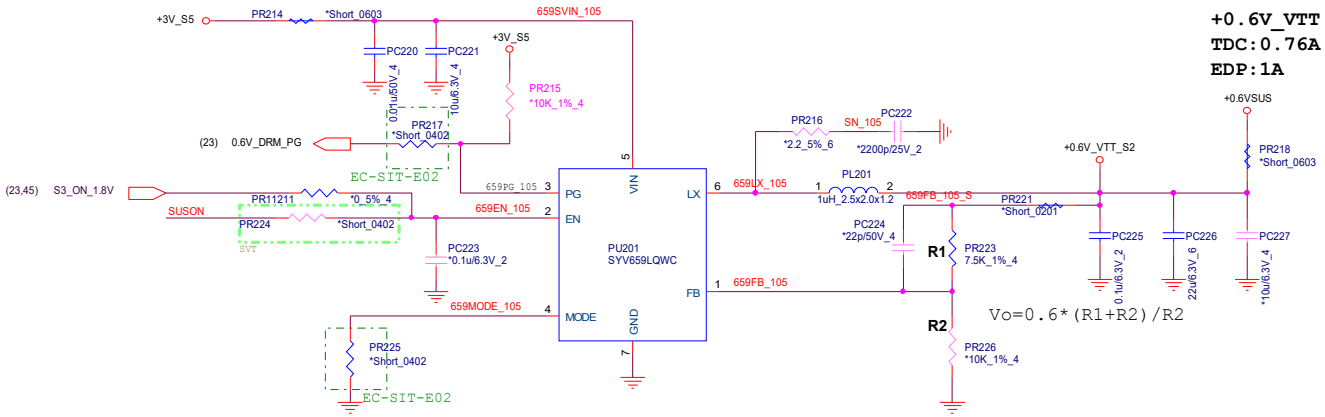
Size	Document Number	Rev
Custom	+3/5VS5 (RT6256B/RT6258C)	1A
	Friday, January 17, 2020	Sheet 38

(6,7,9,18,19,23,24,30,38,40,44,45,46,47,48)
(16,28,37,38,40,41,42,43,48,49)
+3V_S5
+VIN
VDDQ

Table 1—EN1/EN2 control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF





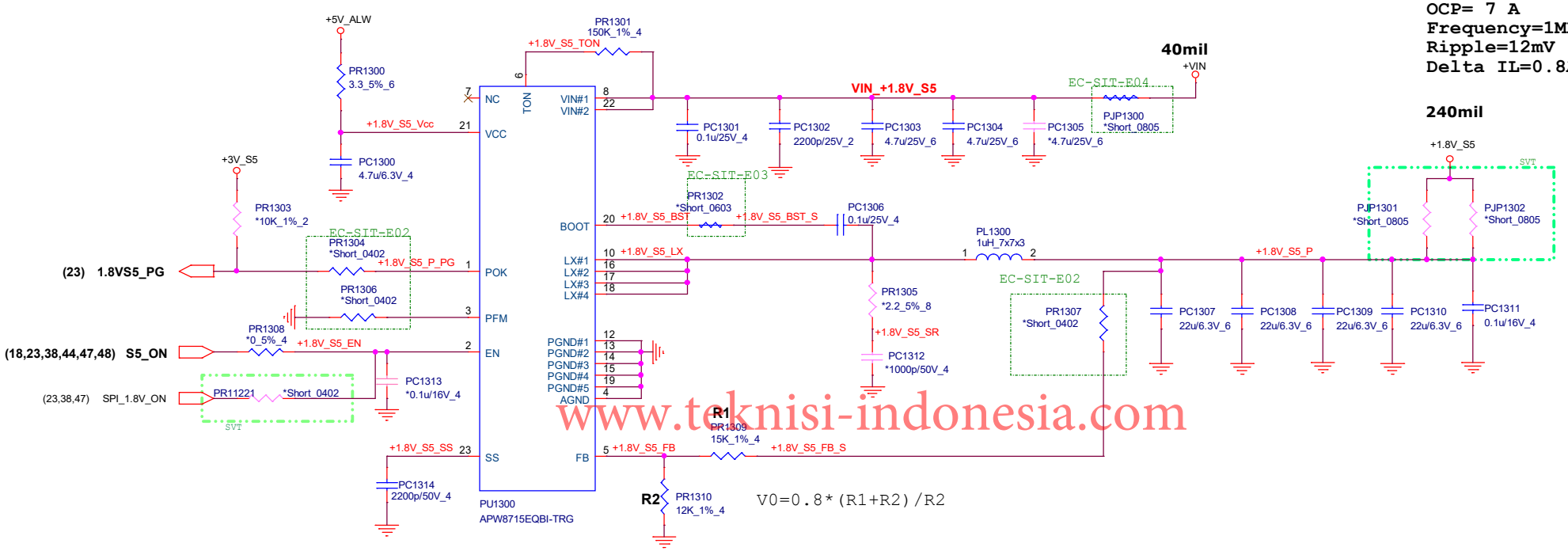
BU5

PROJECT : X3A
Quanta Computer Inc.

Size	Document Number	Rev
	LPDDR4X (NB685A)	1A
Date: Friday, January 17, 2020	Sheet 39 of 54	

+1.8V_S5
Imax= 3.7A
OCP= 7 A
Frequency=1MHz
Ripple=12mV
Delta IL=0.8A

240mil



Quanta Computer Inc.
Project: HP-MONK-P/D

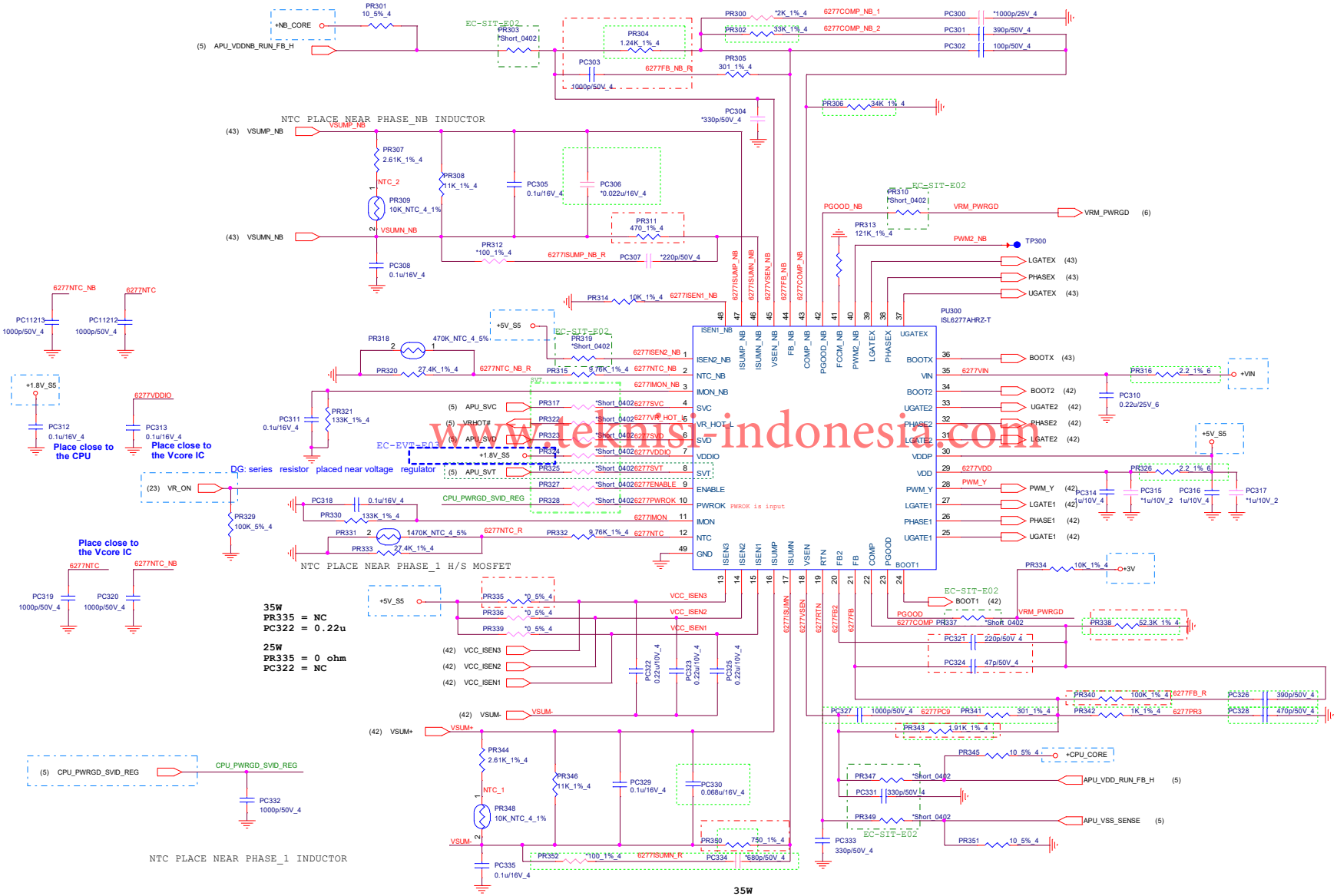
Title		
+1.8V_S5		
Size	Document Number	Rev
	--	A1A
Page Modified: Friday, January 17, 2020		Sheet 40 of 54

NOTE : □□□□□□□□□ , □□□□□□□ , □□□□□FAE□□□□□Low line & OCP & RC time constant
1. EN□□ & VID & VRHOT# & PG net name & pull high □EE□□□□□EE□□□□□
2. Pull high & Output name□□□□□EE□□

□□□□□□□□
□□□□□DB□□□□□□□

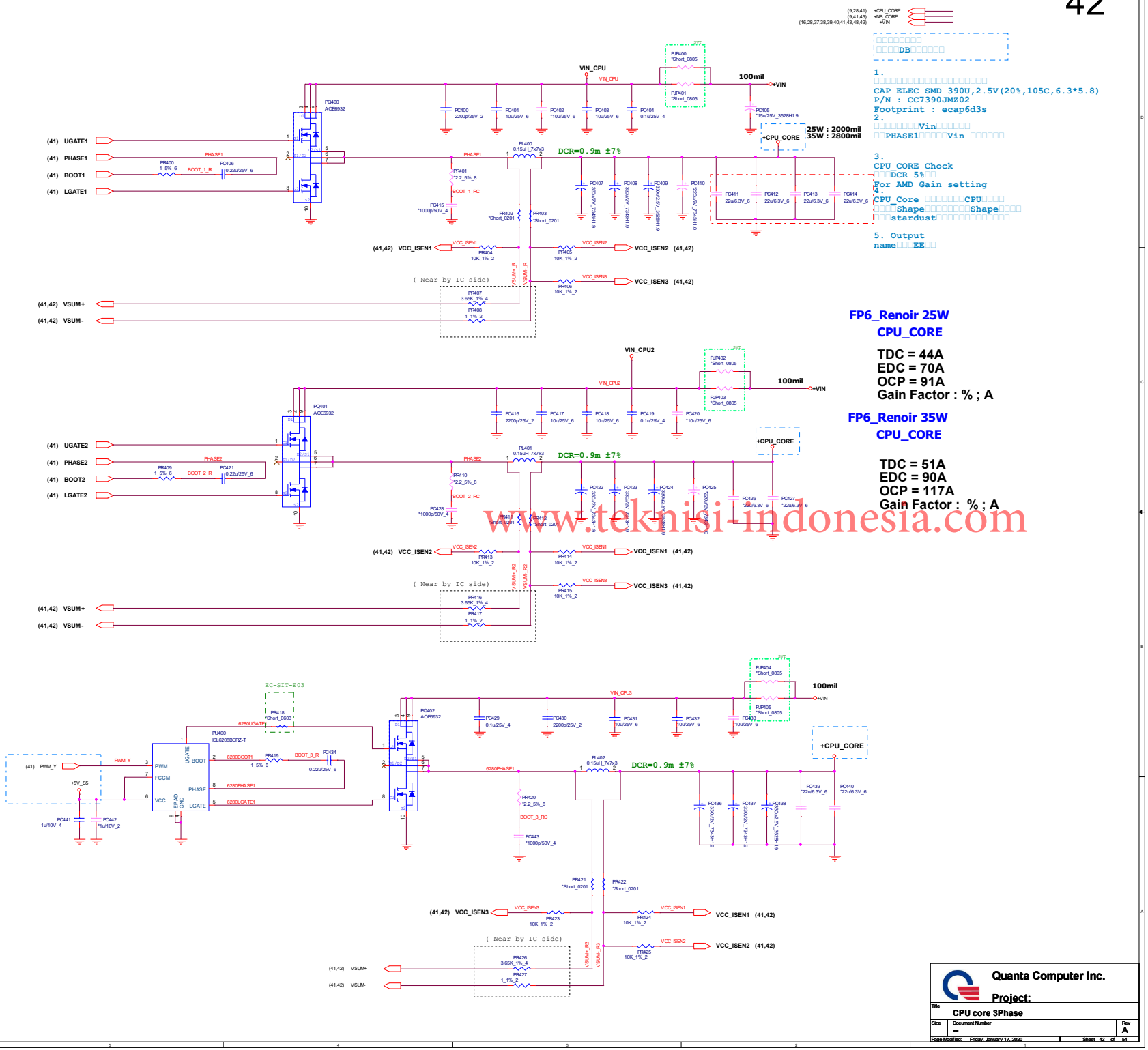
CPU_CORE
NB_CORE
(17,18,27,29,30,32,38,42,45,47) +5V_S5
(5,9,23,24,47,48) +1.8V
(5,6,9,16,17,19,23,24,25,27,29,30,31,32,47) +3V
(16,28,37,38,39,40,42,43,48,49) +VIN

VCORE/VDDNB (ISL6277AHRTZ-T and ISL6208CRZ-T)



Quanta Computer Inc.
Project:

Title	CPU_CORE (ISL6277AHRZ-T)	
Size	Document Number	Rev
	--	A
Page Modified: Friday, March 13, 2020		Sheet 41 of 54



(9,28,41) +CPU_CORE
(9,41,43) +NB_CORE
(16,28,37,38,39,40,41,43,48,49) +VIN

1.
CAP ELEC SMD 390U,2.5V(20%,105C,6.3*5.8)
P/N : CC7390JMZ02
Footprint : ecap6d3s
2.
PHASE1 Vin
3.
CPU_CORE Chock
DCR 5%
For AMD Gain setting
4.
CPU_Core CPU
Shape Shape
stardust
5. Output
name EE

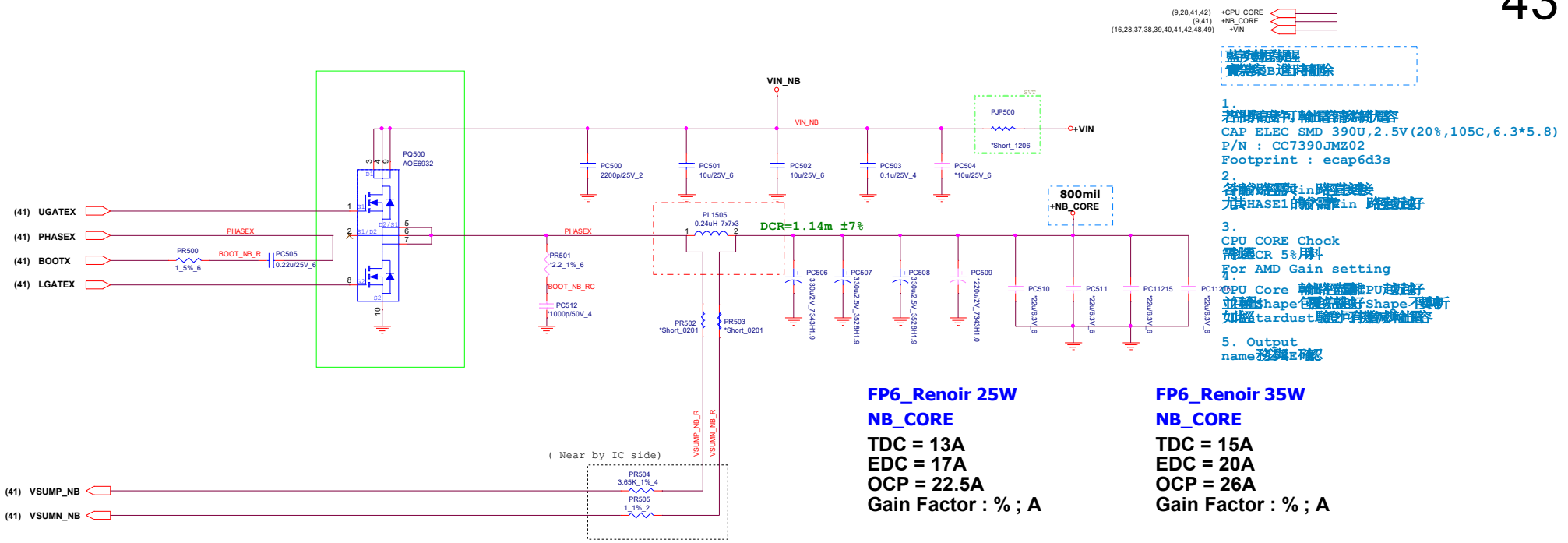
FP6_Renoir 25W
CPU_CORE

TDC = 44A
EDC = 70A
OCP = 91A
Gain Factor : % ; A

FP6_Renoir 35W
CPU_CORE

TDC = 51A
EDC = 90A
OCP = 117A
Gain Factor : % ; A

Quanta Computer Inc.		
Project:		
Title: CPU core 3Phase		
Size	Document Number: --	Rev: A
Date Modified: Friday, January 17, 2020	Sheet 42 of 54	



1.
CAP ELEC SMD 390U,2.5V(20%,105C,6.3*5.8)
P/N : CC7390JMZ02
Footprint : ecap6d3s

2.

3.
CPU CORE Chock
For AMD Gain setting

4.

5. Output

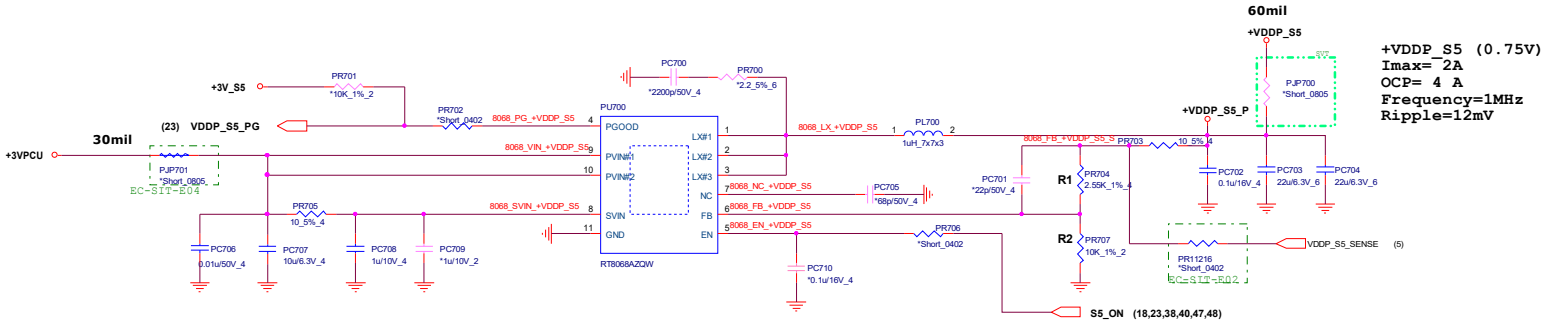
FP6_Renoir 25W
NB_CORE
TDC = 13A
EDC = 17A
OCP = 22.5A
Gain Factor : % ; A

FP6_Renoir 35W
NB_CORE
TDC = 15A
EDC = 20A
OCP = 26A
Gain Factor : % ; A

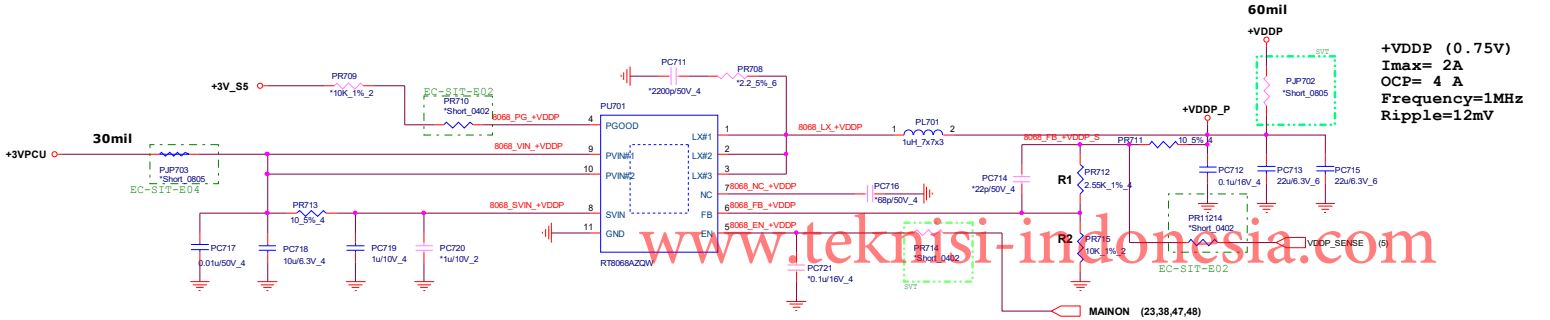
Quanta Computer Inc.
Project:

Title: NB core 1Phase		
Size	Document Number: --	Rev: A
Page Modified: Friday, January 17, 2020		Sheet 43 of 54

(6,7,9,18,19,23,24,30,38,39,40,45,46,47,48) +3V_S5
(17,18,27,29,30,32,38,41,42,45,47) +5V_S5
(16,28,37,38,39,40,41,42,43,48,49) +VIN
(9,48) +VDDP_S5
(5,9,23,48) +VDDP



V0=0.6*(R1+R2)/R2



V0=0.6*(R1+R2)/R2

Quanta Computer Inc.
Project: HP-MONK-P/D

Title: +VDDP (RT8068 & AOZ2261)

Size	Document Number	Rev
	--	A1A

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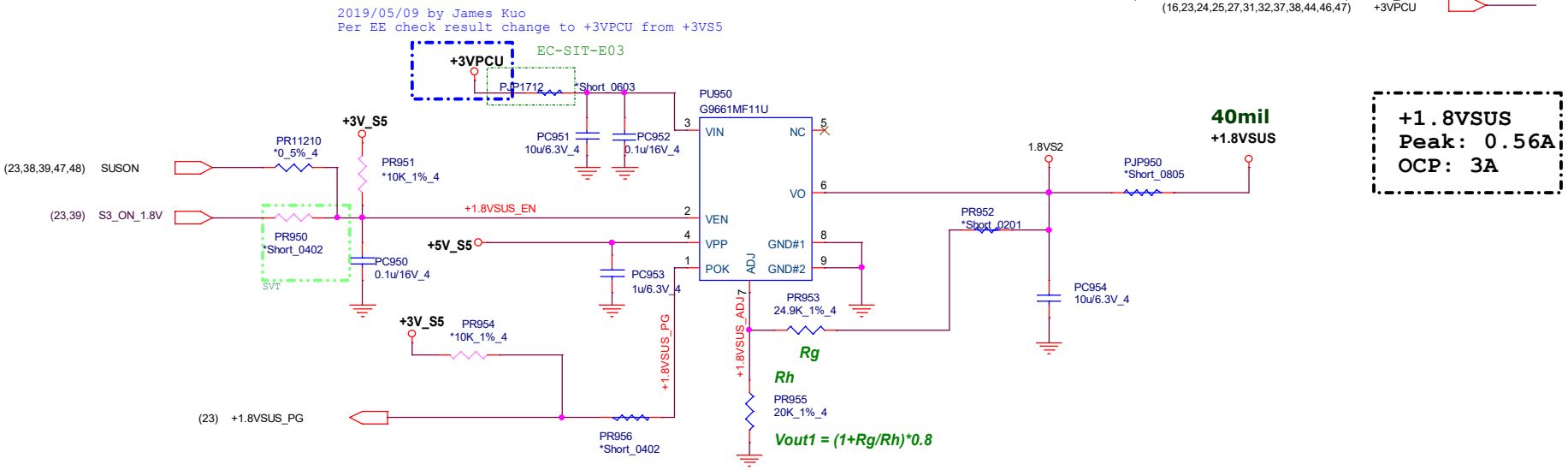
(11,12,13,14,28) +1.8VSUS
(17,18,27,29,30,32,38,41,42,47) +5V_S5
(6,7,9,18,19,23,24,30,38,39,40,44,46,47,48) +3V_S5
(16,23,24,25,27,31,32,37,38,44,46,47) +3VPCU



6.1. Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Core Power 1	VDD1	1.70	1.80	1.95	V	1,2
Core Power 2 & CA Power	VDD2	1.06	1.10	1.17	V	1,2,3
I/O Buffer Power	VDDQ	0.57	0.60	0.65	V	2,3

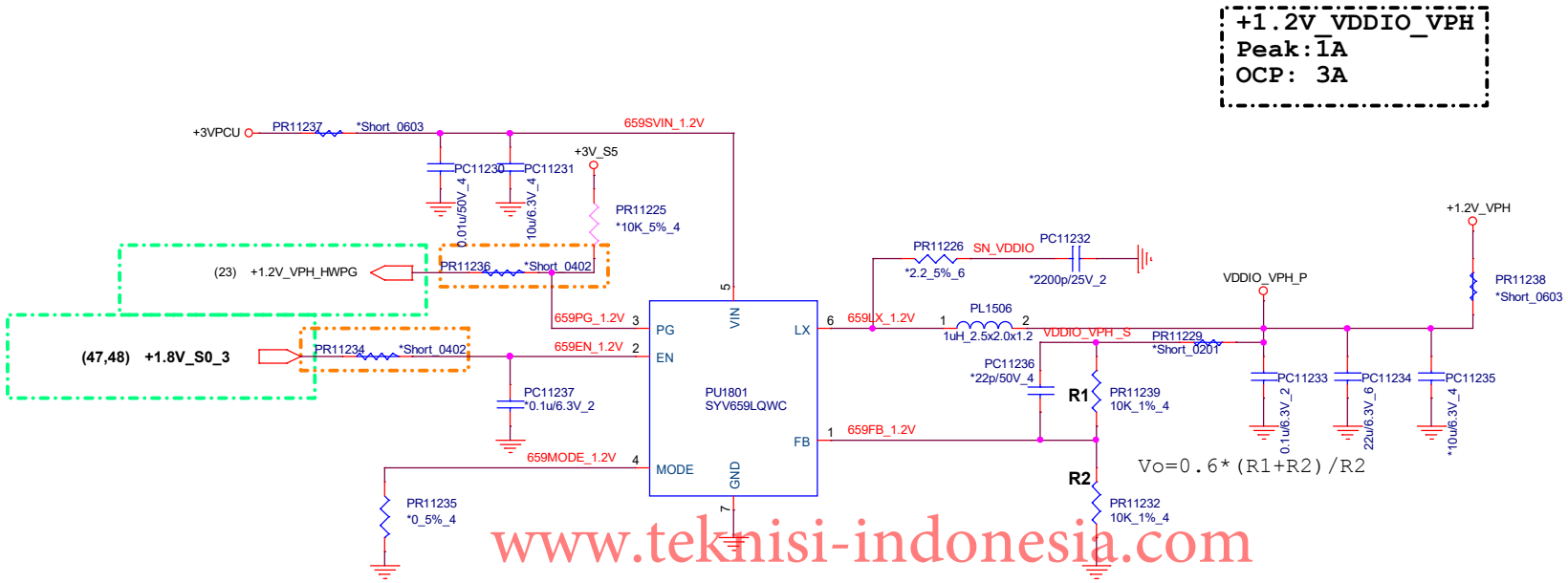
1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table "Voltage Ramp Conditions". VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

Table - Voltage Ramp Conditions

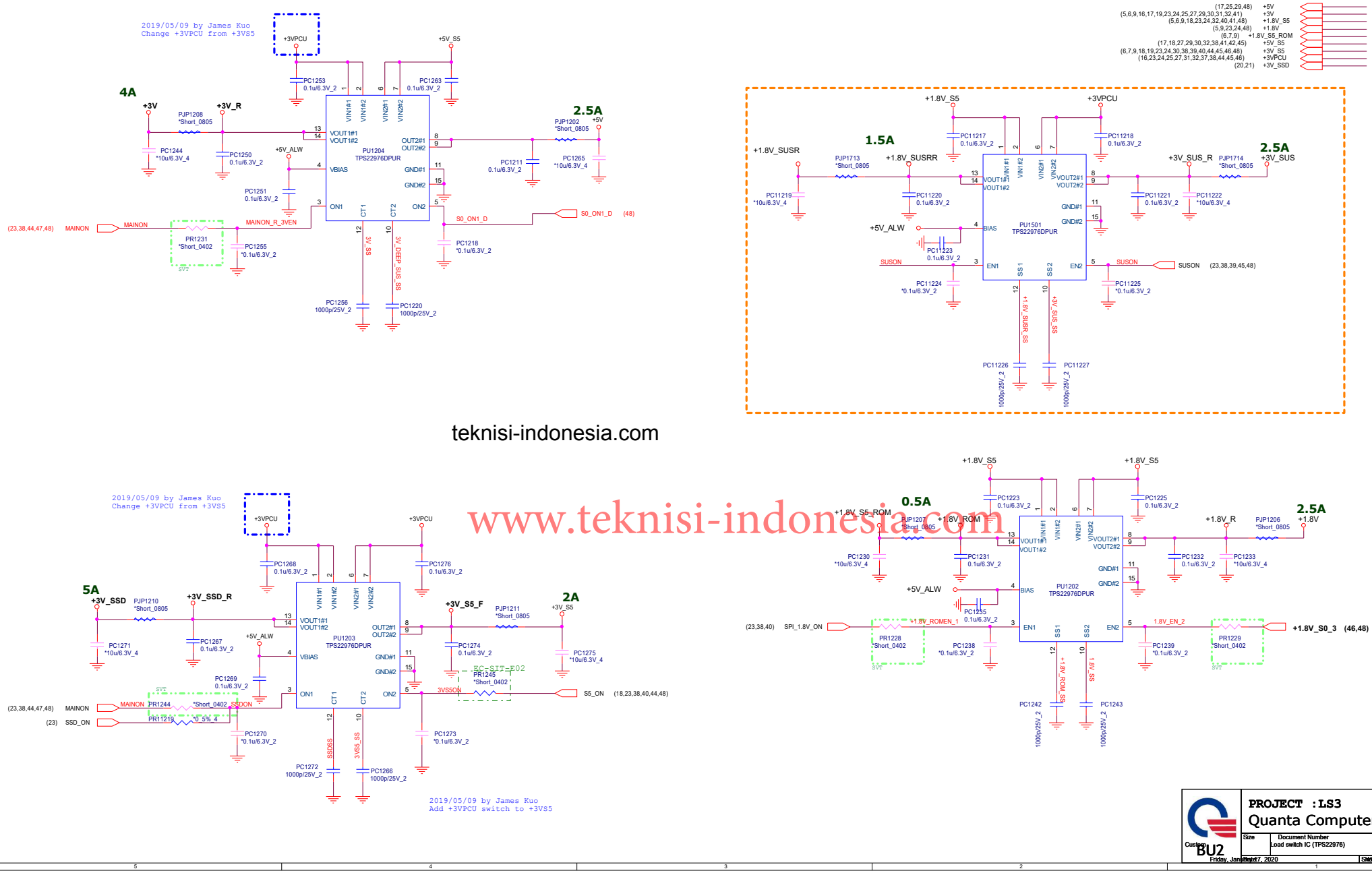
After...	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

PROJECT : LVC
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.8V_GFX(RT8068)/+3V_GFX	1A
BU2	Friday, January 17, 2020	Sheet 58



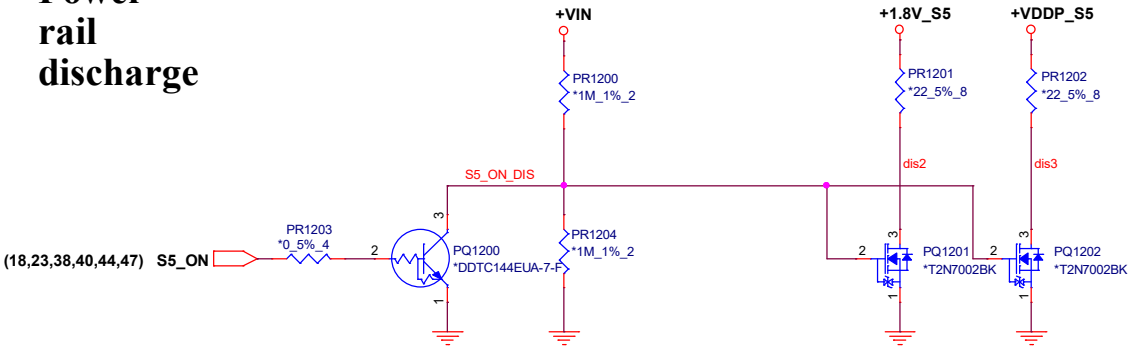
Custom: BU2	PROJECT : LVC Quanta Computer Inc.	
Size	Document Number +1.8V_S5 (RT8068AZQW)	Rev 1A
Friday, January 17, 2020	Date:	Sheet 58

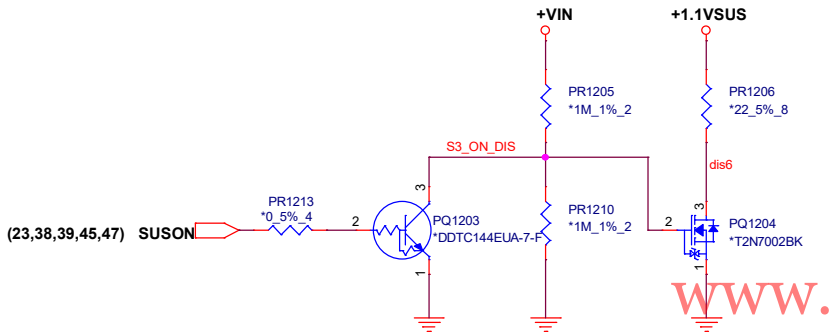


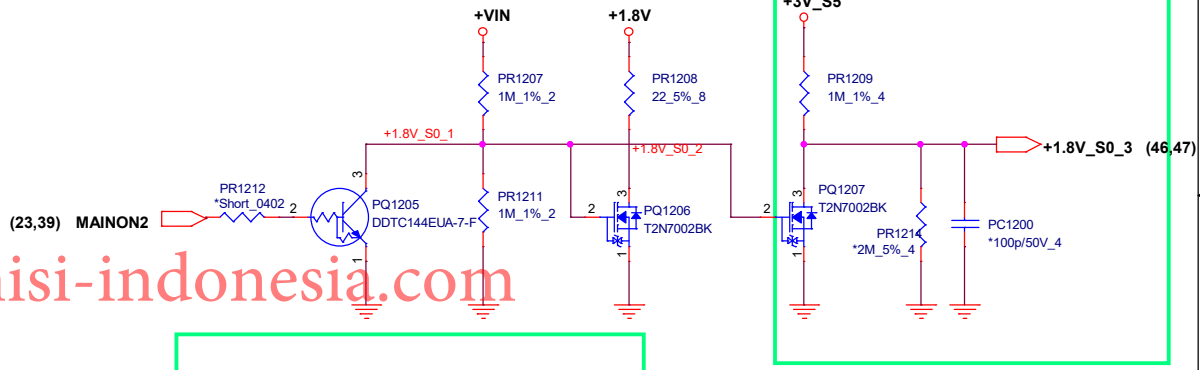
Custom	PROJECT : LS3 Quanta Computer Inc.		
BU2	Size	Document Number Load switch IC (TPS22976)	Rev 1A
Friday, January 17, 2020		Sheet	58

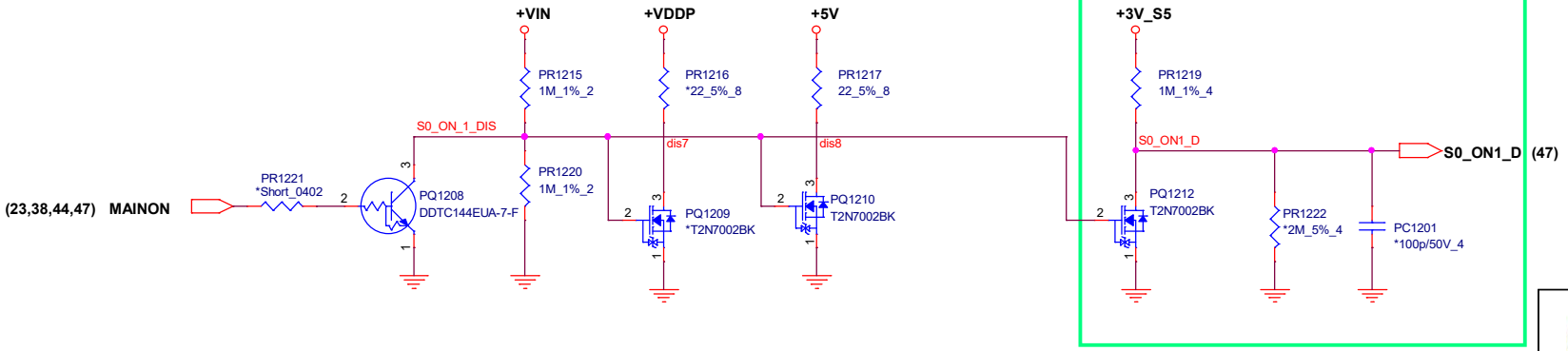
Power rail discharge

(16,28,37,38,39,40,41,42,43,49) +VIN
(6,7,9,18,19,23,24,30,38,39,40,44,45,46,47) +3V_S5
(3,9,11,12,13,14,39) +1.1VSUS
(9,44) +VDDP_S5
(5,6,9,18,23,24,32,40,41,47) +1.8V_S5
(5,9,23,44) +VDDP
(5,9,23,24,47) +1.8V
(17,25,29,47) +5V



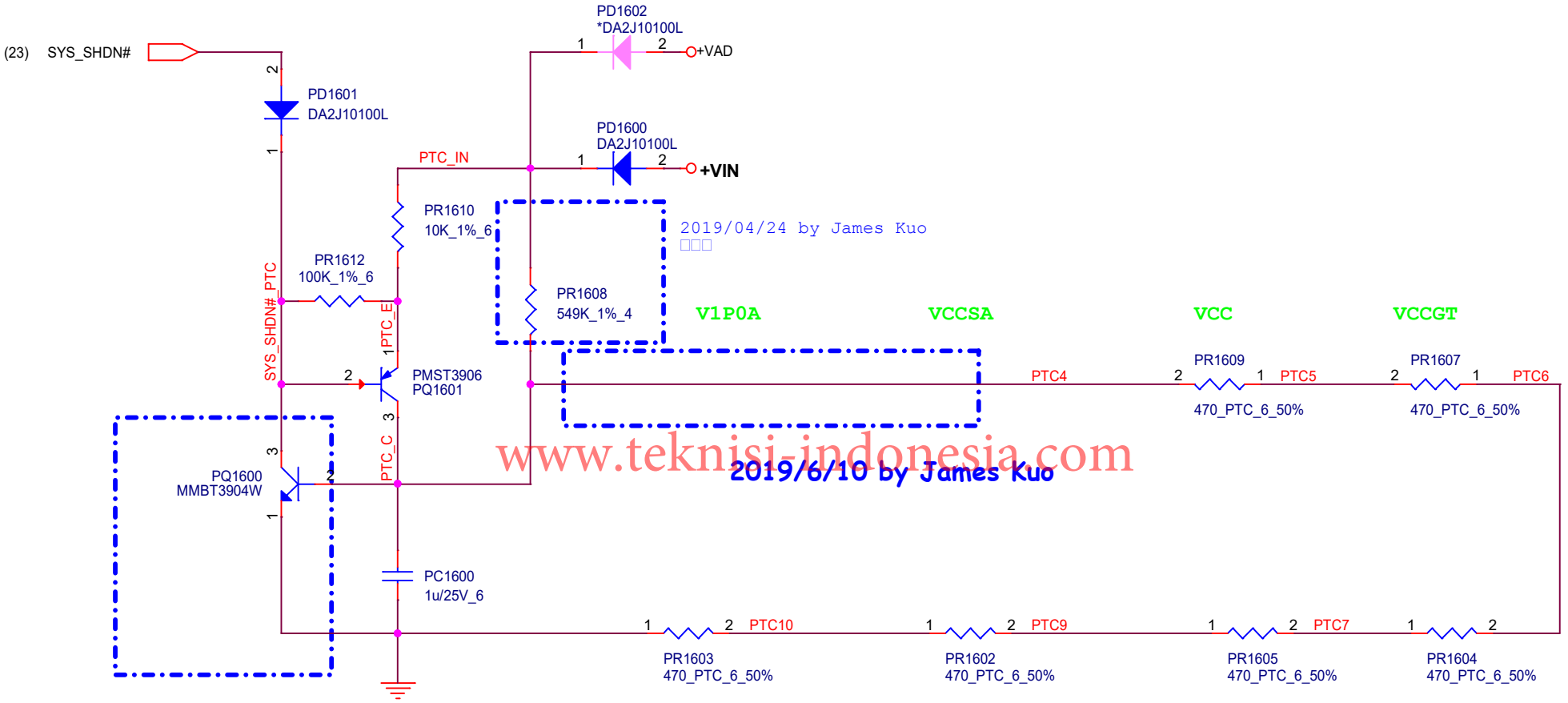






Quanta Computer Inc.
Project: HP-MONK-P/D

Title: Discharge		
Size	Document Number: --	Rev: A1A
Page Modified: Friday, January 17, 2020		Sheet 48 of 54



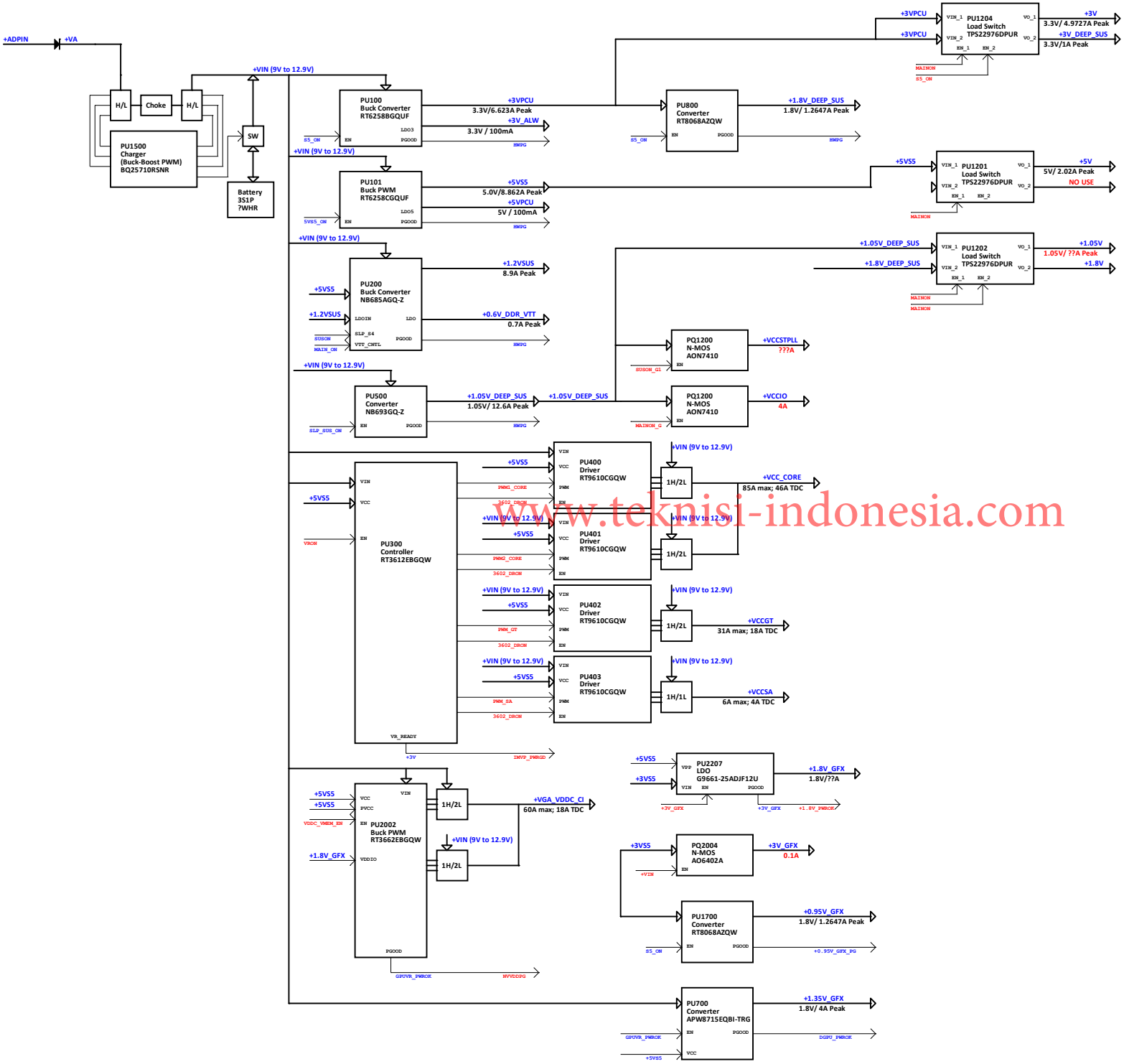
2019/6/10 by James Kuo

2019/04/23 by James Kuo
PQ1600 change to BA039040019 from BA0390400B1

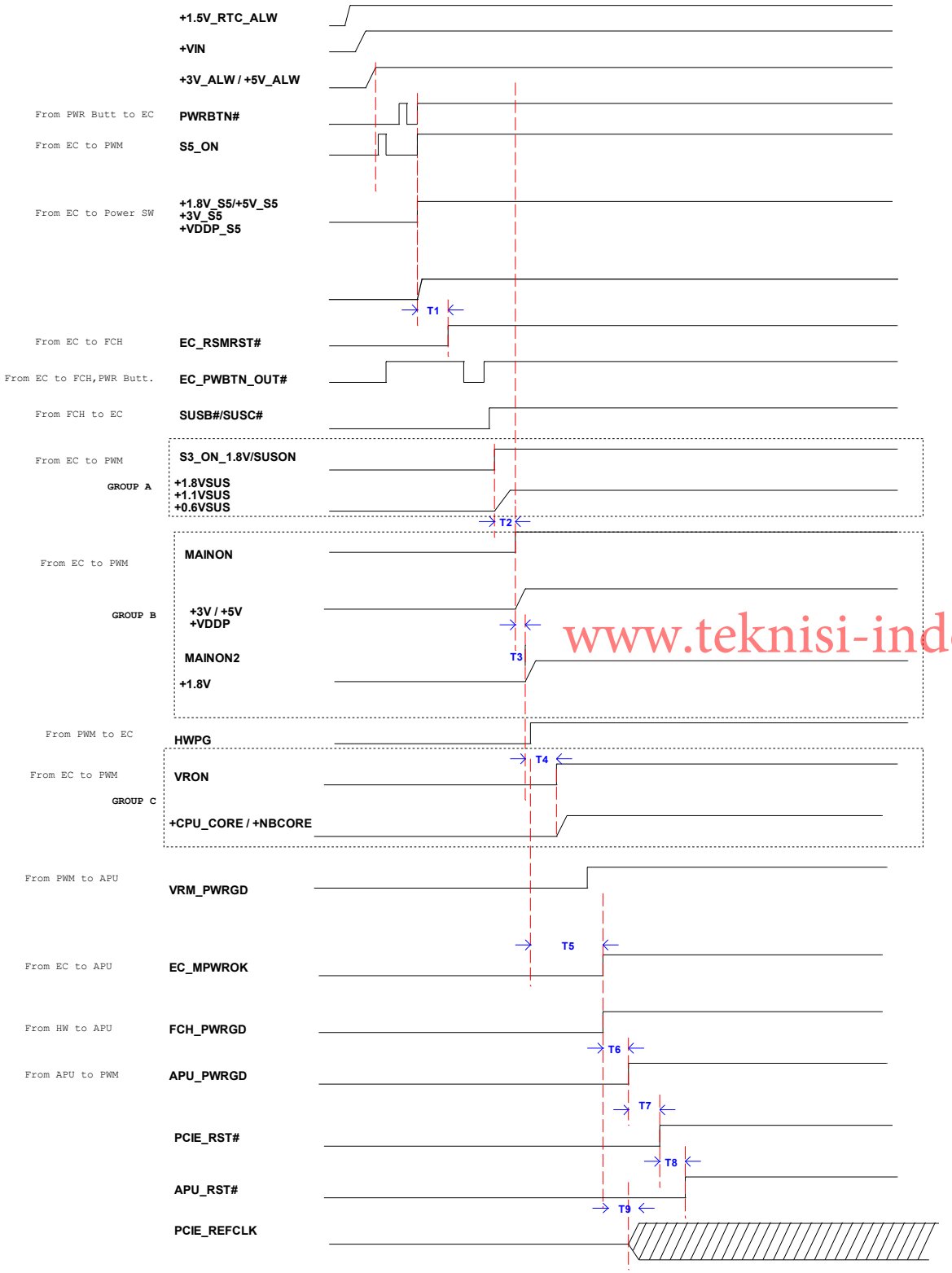
Custom	PROJECT : LVC Quanta Computer Inc.	
BU2	Size: — Document Number: PTC Circuit	Rev: 1A
Friday, January 17, 2020	Date:	Sheet 49 of 54

No.	Change details	Location/Description	Page	Remark
EC-EVT-E01	Change 5V_S5 power rails enable to S5_ON and 5VS5_ON	PR115	38	
EC-EVT-E02	Change APU RTC VCC to 3V_ALW,remove U17	U17,R77985	09	
EC-EVT-E03	Change APU SIV ID VDDIO to 1.8V_S5	PU300	13	
EC-EVT-E04	Change pin41 pin 43 pin define for support SATA	CN3,CN7724,R539,R7908	20,21	
EC-EVT-E05	Change LPDDR4 CAP part number to CH4222K9B04 0402 size		11,12,13,14	
EC-EVT-E06	Stuff Q6452 Q6453 for EC to sensor hub leakage	Q6452,Q6453		
EC-EVT-E07	Change dual mos polar for current leakage	Q6460,Q6467,Q6461,Q5000	24,27	
EC-EVT-E08	Add mos for prevent current leakage	Q28,Q6470	24,32	
EC-EVT-E09	Add IRCAM_FW for FW update	R77986	6,24	
EC-EVT-E10	Add U6449 for IRCAM power control	U6449	24	
EC-EVT-E11	Delete R260 for duplicate netname	R260	06	
EC-EVT-E12	Add TP_INT# for Lenovo reqoest of KB light off		23	
EC-EVT-E13	Add pull high MA,MB EVENT_L for follow AMD REF SCH	R77989,R77990	03	
EC-EVT-E14	Swap DDI1 signals for HDMI pin define		05	
EC-EVT-E15	Reserved re-driver CLK DAT path for debug use	R77991,R77992	17	
EC-EVT-E16	Change GPIO pin for AMD request and sata ssd		20,21	
EC-EVT-E17	Change battery LED power rails to 5V_S5	R77996	29	
EC-EVT-E18	change FN LED netname and add 200 ohm	R77997	25	
EC-EVT-E19	Add Diode to prevent leakage current	D6468	6,23	
EC-EVT-E20	change MBB_DQSH1,L1 order for layouthouse swap modify		14	
EC-EVT-E21	change USB3.0 USB 2.0 TYPEC order for AMD limitation		7	
			5	
EC-EVT-E23	Change CN2100 pin define for follow common design	CN2100	16	
EC-EVT-E24	add 5V_S5 one pin for increase current		25	
EC-EVT-E25	change CN7720,CN7711 footprint	CN7720,CN7711	25,30	
EC-EVT-E26	change I2C0,I2C1 power domain from 1.8V to 3.3V and remove level shifter		6,27	
EC-EVT-E27	change battery led control use mos instead of BJT reduce s5 power comsuption		29	
EC-EVT-E28	change KB light control	Q5003,Q5003	25	
EC-EVT-E29	change HDMI EMI resister	R3501,R3502,R73503,R3504	17	
EC-EVT-E30	change sensor smbus addresss add pull up resister for SMBUS	R78006,R78007,R78008,R78009	29	
EC-EVT-E31	change Audio DVDD-IO to 1.8V		18	
EC-EVT-E32	change S5_ON and SPI_1.8V_ON on EC pin order to avoid EC load code fail		23	
EC-EVT-E33	change CN7725 footprint		24	
EC-EVT-E34	Reserve UART interface for support WLAN 802.11ax card		6,19	
EC-EVT-E35	Add CPU CAP for stable CPU power		9	
EC-EVT-E36	unstuff R5803 for TPS65988 HPD is pushpull type		31	
EC-FVT-E01	Change sensor hub to SUS power rails to support wake on TOF	R78042,R8108,Q6461	24	
EC-FVT-E02	Reserve Aufio PDM level shifter for WoV feature		24	
EC-FVT-E03	Change Speaker bead to 0 ohm		18	
EC-FVT-E04	Change FP conn pin define	CN5201	27	
EC-FVT-E05				
EC-FVT-E06	Change FP power rails to 3VPCU to support SSO		27	
EC-FVT-E07	Add EC pin to control dead battery function		32	
EC-FVT-E08				
EC-FVT-E09	Remove GPIO67,76 for HW strip pin		6	
EC-FVT-E10	change sensor hub I2C interface location from EC		23	
EC-FVT-E11	Reserve S5 and S3 power rails for support Wov feature		18	
EC-FVT-E12	Add APU_THERMTRIP# to prevent restart issue		23	
EC-FVT-E13	Change thermal sensor NCT7719W for AMD STT2.0		29	
EC-FVT-E14	Change TOF sensor power rails same as sensor hub		24	
EC-FVT-E15	Change Y1 Y2 CAP value for EA test		6	
EC-FVT-E16	Add pull down GPD2 for ITE5570 HW issue		23	
EC-FVT-E17				
EC-FVT-E18	Change DMIC power rails same as APU AUDIO_VDDIO power rails		24	
EC-FVT-E19	Change camera power rails to S5 power for MS3 issue		24	
EC-FVT-E20	Add AND gate to meet PCIe specification		21	
EC-FVT-E21	Change head phone damp resister for EA test		18	
EC-FVT-E22	Add DMIC led control for Audio codec and APU		6,18,25	
EC-FVT-E23	Add FP LED for EC control		23,30	
EC-FVT-E24	Add SUS power for touch pad		27	
EC-FVT-E25	Add LPC header for MS3 debug		19	
EC-FVT-E26				
EC-FVT-E27				
EC-SIT-EE01	Change ALS interrupter pin define		19	
EC-SIT-EE02	Add 1.2V_VPH for EDP panel power saving		6	
EC-SIT-EE03	Keeping WLAN wake pin to oringnal location		6,7,19	
EC-SIT-EE04	Change WLAN,PD interrupt,s0i3 setting		6,19	
EC-SIT-EE06	Change FP power control for LVA suggest		27	
EC-SIT-EE08	Change PD I2C location for support PDFW update		6,32	
EC-SIT-EE09	ADD PD reset pin to EC		23	
EC-SIT-EE10	ADD PD HPD levle shifter for PD leakage issue		32	
EC-SIT-EE11	ADD cap for RSMRST#_R noise		6	
EC-SIT-EE12	Change HDMI SCL,SDA and damping resister		17	
EC-SIT-EE13	ADD mos for APU_RST# to EC notify		23	

POWER BLOCK DIAGRAM



PROJECT : LVC
Quanta Computer Inc.

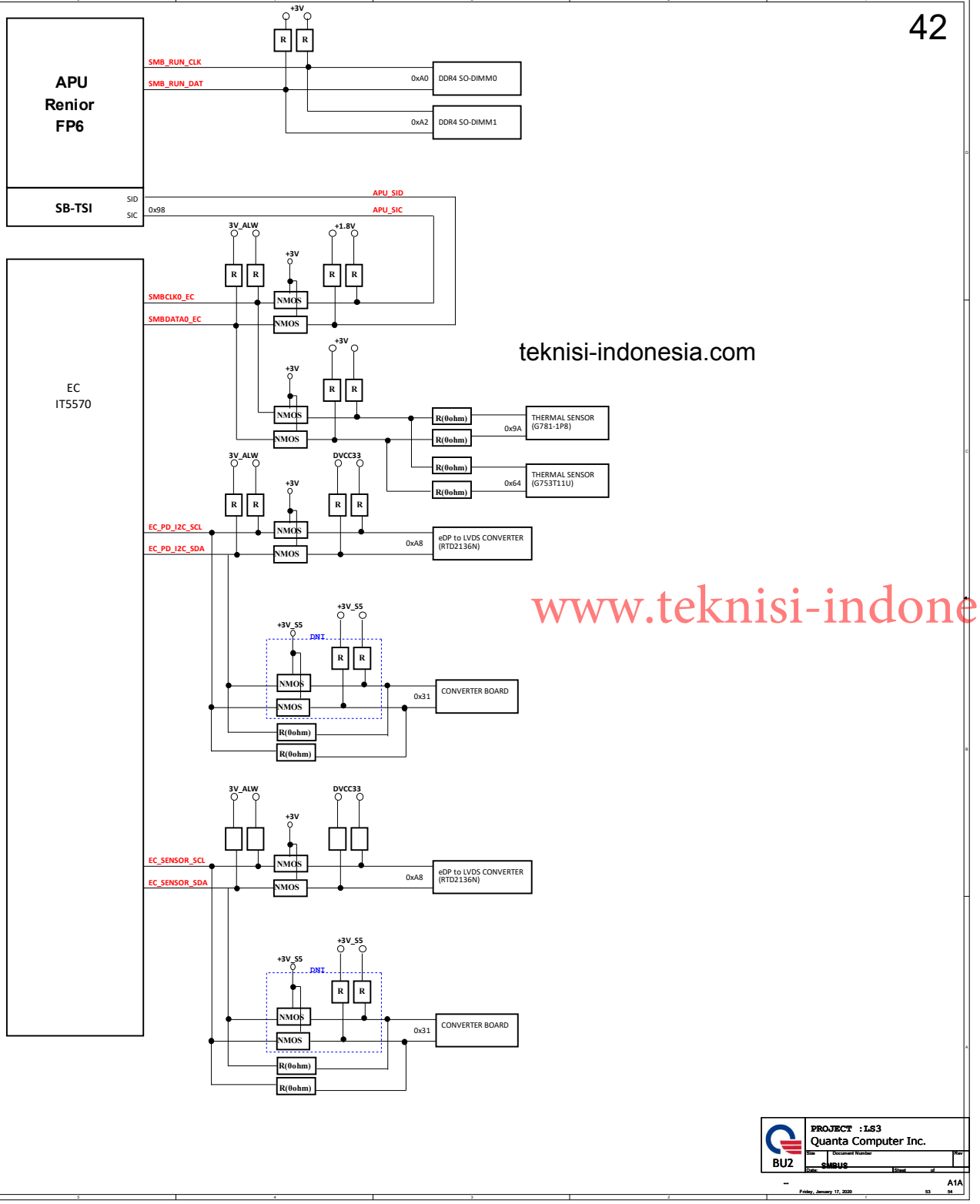


System Power Sequence

EC Control:
T1: S5_ON TO EC_RSMRST# = 20ms
T2: S3_ON TO MAIN_ON1=10ms
T3: MAIN_ON1 TO MAIN_ON2 = 1ms
T4: MAIN_ON2 TO VRON = 10ms
T5: HWPG TO MPWROK =99ms

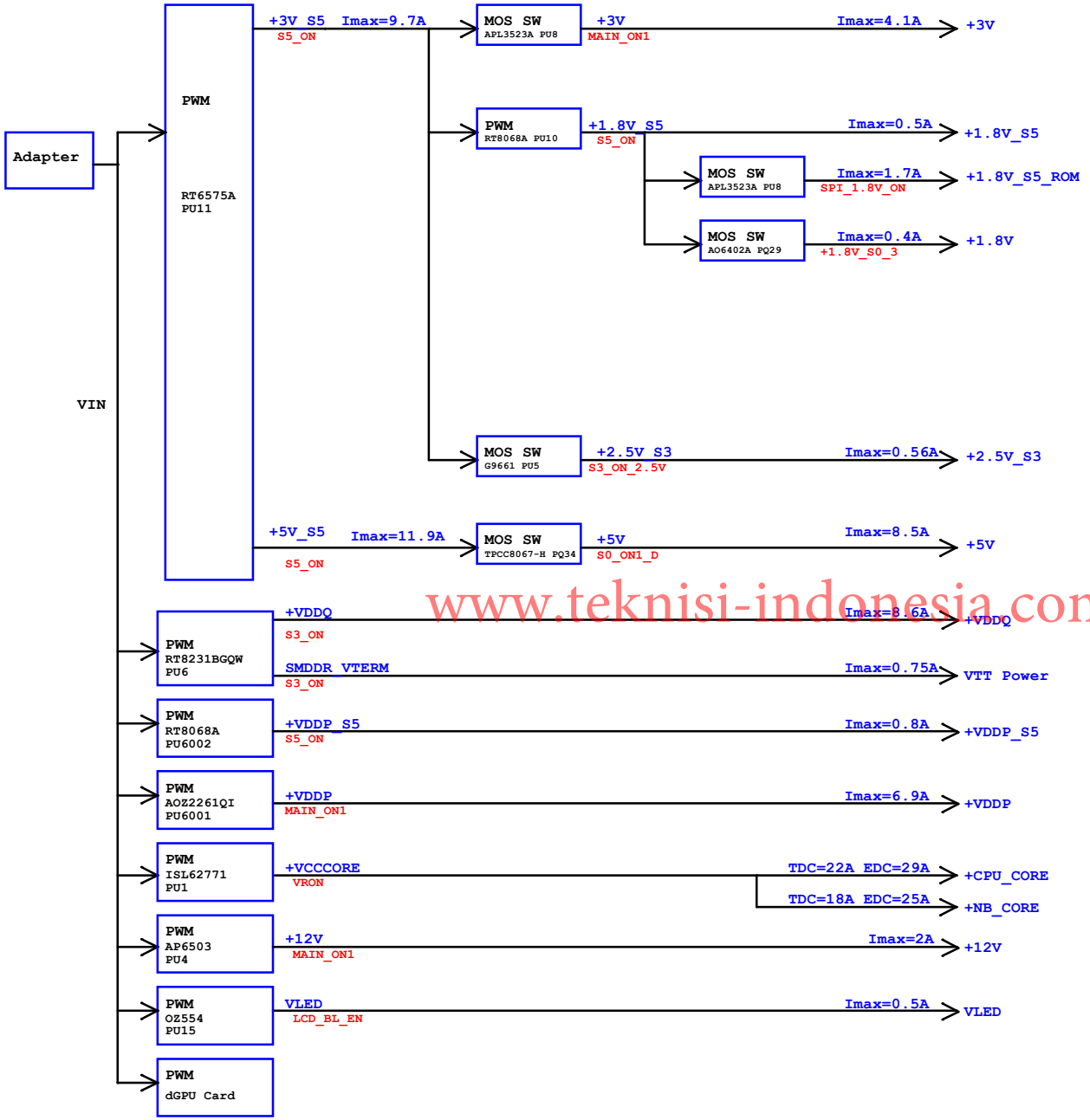
Timing spec:
T1 Spec:10ms min
Power Up Spec:
Group A > Group B > Group C
T6: FCH_PWRGD TO APU_PWRGD = 108.6~118.6 ms
T7: APU_PWRGD TO PCIE_RST# = 114.2~124.2 ms
T8: PCIE_RST# TO APU_RST# = 111.9~121.9 ms
T9: FCH_PWRGD TO PCIE_REFCLK = 37.6~47.6 ms

PROJECT : LS3
Quanta Computer Inc.
BU2
Power Sequence
A1A



PROJECT : LS3
Quanta Computer Inc.
BU2
SMBUS
A1A
Friday, January 17, 2020
53
54

Power Delivery Map



HP Restricted Secret

BU2	PROJECT : LS3 Quanta Computer Inc.
Size	Document Number: Power Delivery Map — Rev: --
Date: Friday, January 17, 2020	Sheet 54 of 54 — A1A