what's a CPU simulator ?

CPUlator is a functional simulator of a computer system (CPU and I/O devices), a debugger, and (an interface to) an assembler

There are four main components in a typical development flow for simple assembly programs: Source code written by the user, an assembler (or compiler for a higher-level language) to transform the source code into executable machine code, a computer system to run the machine code, and a debugger to observe the behaviour of the program running on the computer. CPUlator provides the assembler, computer, and debugger inside a web browser.

CPUlator's design was based on the Altera Monitor Program, so there are many similarities. In the Altera Monitor Program development flow, the Monitor Program provides the assembler and debugger, while the computer system is running on an FPGA development board attached to the host PC over a programming cable. (Top-most option in the figure below)

Compiling Code:

Internally, the CPUlator simulator simulates executable machine code (it does not directly simulate assembly source code). You can compile your source code using the built-in assembler, Altera Monitor Program, or any other development tools you wish. The built-in editor and assembler is limited to working with a single assembly-language source file. If your program requires more than one file or is written in another language (e.g, C), you must compile the program yourself and simulate the compiled executable.

what are some popular simulators ?

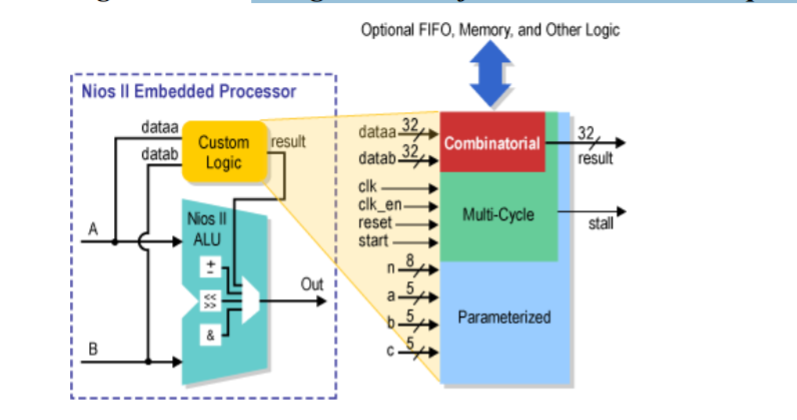
there are many simulators, including CPUIator, MARS 4.5, QtSPIM 9.1.20, ARMSim 1.91 and NIAS II

Compariason chart :

NIOS II :

The Nios® II family of soft-core processors is Altera’s second-generation embedded processor for FPGAs. With over 200 DMIPs of performance in designs targeting the Stratix® II family of high-performance FPGAs, the Nios II family delivers mainstream performance to address a broad range of embedded applications. The Nios II family consists of three members – fast, economy and standard – each optimized for a specific price and performance range. All three cores use the same instruction set architecture (ISA) and are 100% binary code compatible. Nios II processors can be added to a designer’s system using the SOPC Builder system development tool now featured in the Quartus® II development software

k diagram view of custom instruction implementation in the Nios II CPU :



* Separate instruction and data caches (512 [B](https://en.wikipedia.org/wiki/Byte) to 64 [KB](https://en.wikipedia.org/wiki/Kilobyte))
* Optional [MMU](https://en.wikipedia.org/wiki/Memory_management_unit) or [MPU](https://en.wikipedia.org/wiki/Memory_protection_unit)
* Access to up to 2 [GB](https://en.wikipedia.org/wiki/Gigabyte) of external address space
* Optional tightly coupled memory for instructions and data
* Six-stage pipeline to achieve maximum [DMIPS](https://en.wikipedia.org/wiki/DMIPS)/MHz
* Single-cycle hardware multiply and barrel shifter
* Optional hardware divide option
* Dynamic [branch prediction](https://en.wikipedia.org/wiki/Branch_predictor)
* Up to 256 custom instructions and unlimited hardware accelerators
* [JTAG](https://en.wikipedia.org/wiki/JTAG) debug module
* Optional JTAG debug module enhancements, including hardware breakpoints, data triggers, and real-time trace

NIOS II in the industry :

NiosII processor core is the FPGA industry’s most widely used soft processor based on design starts, as confirmed by the market research firm Gartner in its most recent report “Market Trends: ASIC Design Starts 2007.” Altera’s Nios II processor core is a configurable, 32-bit FPGA-based soft microprocessor that is used in a wide variety of applications and end markets such as wireline, broadcast, military, wireless, automotive, and consumer.