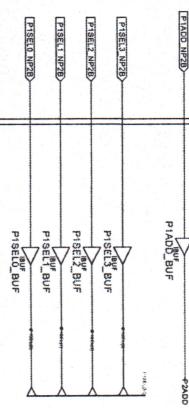
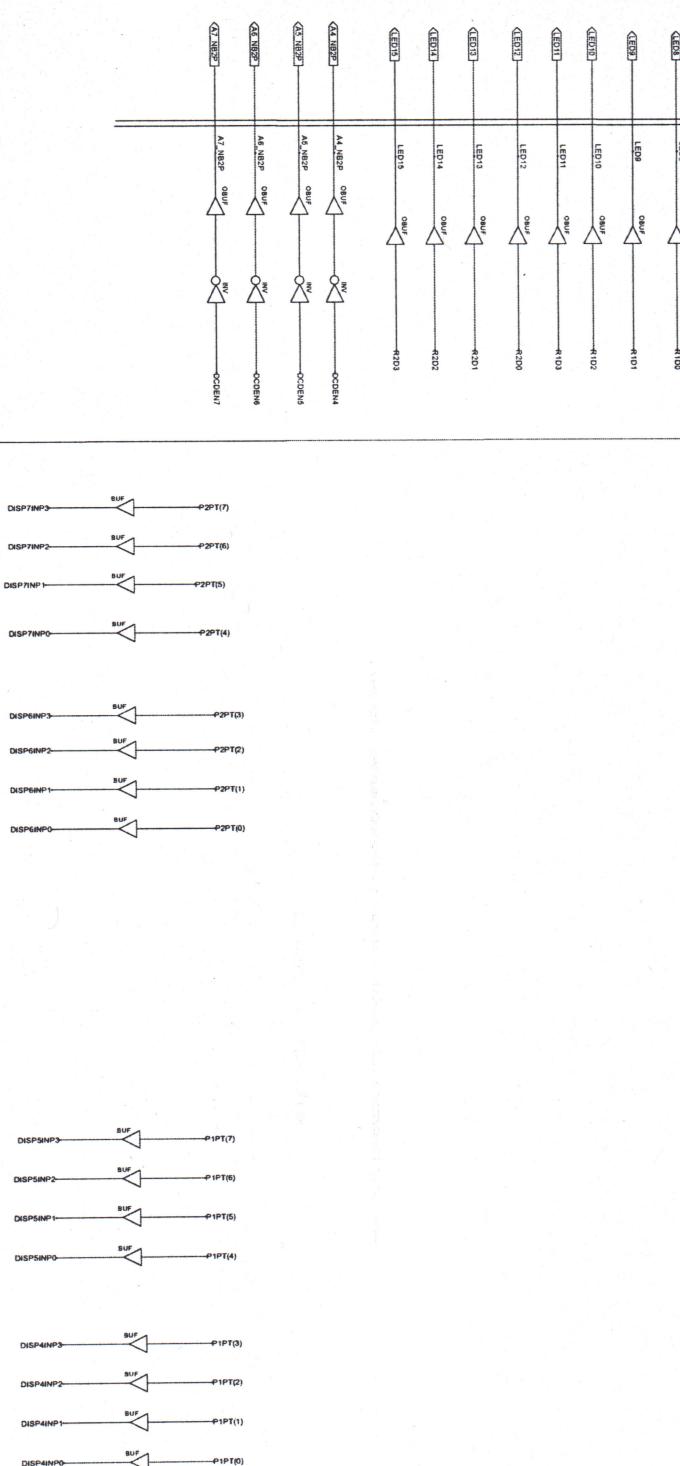


SEVENSEGMENTDECODER



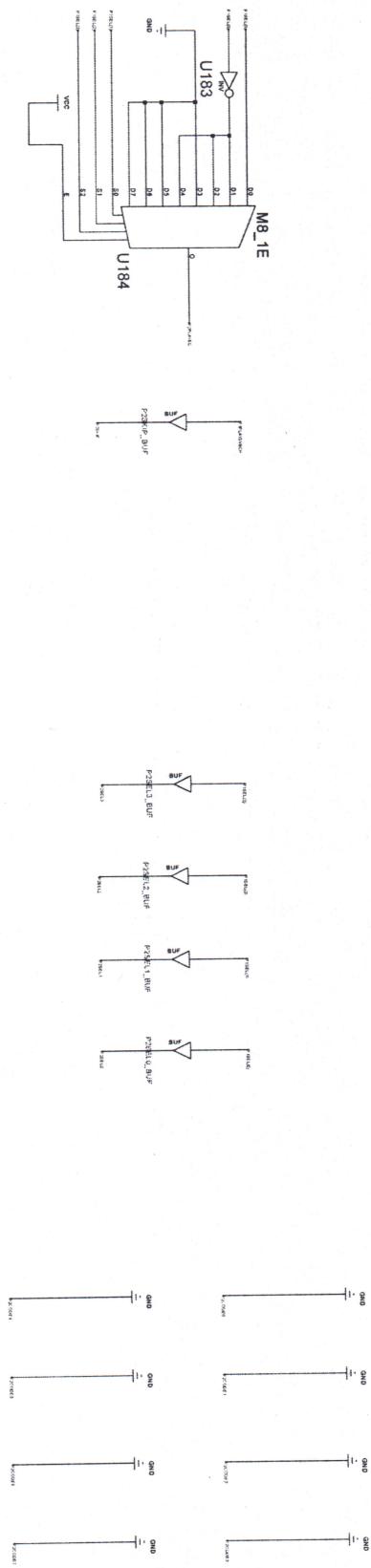
IO PADS

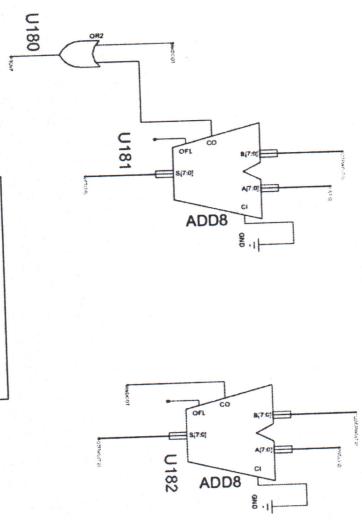
IO BUFFER SUB-BLOCK



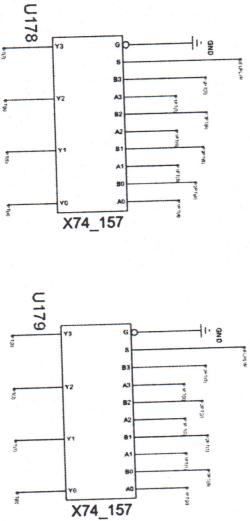


XC3S100E-2TQ144-100V
NAND Flash 128Mbit
NAND Flash 128Mbit
NAND Flash 128Mbit





POINTS ADDITION SUB-BLOCK



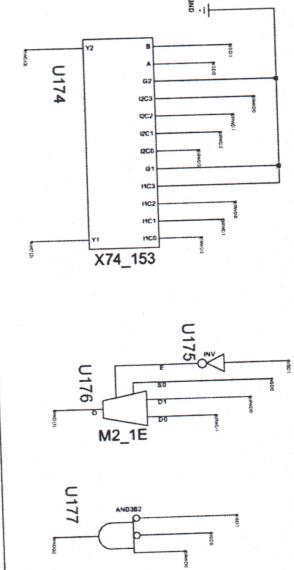
The diagram shows two integrated circuits, U178 and U179, each containing a 74157 logic component. The 74157 is a 16-pin integrated circuit package with the following pinouts:

- Pin 1 (GND):** Ground connection.
- Pin 2 (S):** Input enable or clock pin.
- Pin 3 (Y3):** Output Y3.
- Pin 4 (Y2):** Output Y2.
- Pin 5 (Y1):** Output Y1.
- Pin 6 (Y0):** Output Y0.
- Pin 7 (A3):** Input A3.
- Pin 8 (A2):** Input A2.
- Pin 9 (A1):** Input A1.
- Pin 10 (A0):** Input A0.
- Pin 11 (B3):** Input B3.
- Pin 12 (B2):** Input B2.
- Pin 13 (B1):** Input B1.
- Pin 14 (B0):** Input B0.
- Pin 15 (Z):** Output Z.
- Pin 16 (V_D):** Power supply connection.

U178: The inputs A3 through A0 are connected to the outputs Y3 through Y0 respectively. The inputs B3 through B0 are connected to the outputs Z, Y1, Y2, and Y3 respectively. The output Y0 is connected to the input A3 of U179. The output Y1 is connected to the input A2 of U179. The output Y2 is connected to the input A1 of U179. The output Y3 is connected to the input A0 of U179. The output Z is connected to the input B3 of U179. The output Y1 is also connected to the input B2 of U179. The output Y2 is connected to the input B1 of U179. The output Y3 is connected to the input B0 of U179.

U179: The inputs A3 through A0 are connected to the outputs Y3 through Y0 respectively. The inputs B3 through B0 are connected to the outputs Z, Y1, Y2, and Y3 respectively. The output Y0 is connected to the input A3 of U178. The output Y1 is connected to the input A2 of U178. The output Y2 is connected to the input A1 of U178. The output Y3 is connected to the input A0 of U178. The output Z is connected to the input B3 of U178. The output Y1 is also connected to the input B2 of U178. The output Y2 is connected to the input B1 of U178. The output Y3 is connected to the input B0 of U178.

Points Subblock



The diagram illustrates the logic connections between four integrated circuits: U174, U175, U176, and U177.

- U174:** An 8-to-3 decoder with enable input E. Its outputs are labeled Y1 through Y8. The output Y1 is connected to the enable input E of U175. The outputs Y2 and Y3 are connected to the enable inputs E of U176 and U177 respectively. The outputs Y4 through Y8 are connected to the inputs of an AND gate M2_1E, which has an output labeled M2_1E.
- U175:** A 4-to-1 multiplexer with enable input E. Its outputs are labeled D0 through D3. The output D0 is connected to the enable input E of U176. The outputs D1 and D2 are connected to the enable inputs E of U177. The output D3 is connected to the inputs of AND gate M2_1E.
- U176:** A 4-to-1 multiplexer with enable input E. Its outputs are labeled D0 through D3. The output D0 is connected to the enable input E of U177. The outputs D1 and D2 are connected to the enable inputs E of AND gate M2_1E. The output D3 is connected to the inputs of AND gate M2_1E.
- U177:** An AND gate with two inputs. Its output is connected to the inputs of AND gate M2_1E.
- M2_1E:** An AND gate with four inputs. Its output is labeled M2_1E.

The diagram illustrates two integrated circuit packages, U172 and U173, connected to a memory component X74_153.

- U172:** Contains an AND3 gate (labeled AND3) and a D flip-flop (labeled DFF). The AND3 gate has inputs from the memory (Q1, Q2, Q3, Q4) and output Y2. The DFF has inputs from Y2 and the memory (Q1, Q2, Q3, Q4), and outputs Y1 and Y3.
- U173:** Contains a 16x1 RAM array (labeled RAM-16x1) with address inputs A through H and data inputs D0 through D15. It also includes a 4-to-1 multiplexer (MUX) with select inputs S1 and S0, and a 4-to-1 decoder (DECODE) with inputs from the memory (Q1, Q2, Q3, Q4).
- X74_153:** A 16x1 RAM array with address inputs A through H and data inputs D0 through D15. It receives data from U173 and provides address signals (Q1, Q2, Q3, Q4) to both U172 and U173.

The diagram illustrates two integrated circuit packages, U172 and U173, connected to a memory component X74_153.

- U172:** Contains an AND3 gate (labeled AND3) and a D flip-flop (labeled DFF). The AND3 gate has inputs from the memory (Q1, Q2, Q3, Q4) and output Y2. The DFF has inputs from Y2 and the memory (Q1, Q2, Q3, Q4), and outputs Y1 and Y3.
- U173:** Contains a 16x1 RAM array (labeled RAM-16x1) with address inputs A through H and data inputs D0 through D15. It also includes a 4-to-1 multiplexer (MUX) with select inputs S1 and S0, and a 4-to-1 OR gate (labeled OR4).
- X74_153:** A 16x1 RAM array with address inputs A through H and data inputs D0 through D15.

Connections include:

- Address lines A through H from U173 are connected to the address inputs of both RAM arrays.
- Data lines D0 through D15 from U173 are connected to the data inputs of both RAM arrays.
- Control lines S1 and S0 from U173 are connected to the MUX select inputs of both RAM arrays.
- Control line OR4 from U173 is connected to the OR gate input of both RAM arrays.
- Output Y1 from U172 is connected to the data input of RAM array X74_153.
- Output Y3 from U172 is connected to the data input of RAM array U173.
- Outputs Q1, Q2, Q3, and Q4 from RAM array U173 are connected to the inputs of the AND3 gate in U172.
- Outputs Q1, Q2, Q3, and Q4 from RAM array X74_153 are connected to the inputs of the DFF in U172.
- Outputs Y2 and Y3 from U172 are connected to the data inputs of RAM array X74_153.
- Outputs Y1 and Y3 from U172 are connected to the data inputs of RAM array U173.

Regular Reward Calculation Subblock

Regular Reward Calculation Subblock

Unencoded Adjacency Subsubblock

Unencoded Adjacency Subsubblock

Encoded Adjacency Subsubblock

Encoded Adjacency Subsubblock

Equality Check Subsubblock

Equality Check Subsubblock

The diagram illustrates the signal flow through the 1U95 equalizer system. The input signal enters the first stage, labeled COMP4, which contains a series of six compressor modules (B3, B2, B1, B0, A3, A2, A1, A0). The output of COMP4 then passes through an equalizer stage (EQ), followed by a second stage labeled U159, which contains a series of six graphic equalizer modules (B3, B2, B1, B0, A3, A2, A1, A0). Finally, the signal passes through a third stage labeled COMP4, which contains a series of six compressor modules (B3, B2, B1, B0, A3, A2, A1, A0). The output of the final stage is labeled "Output".

The diagram illustrates the signal flow through the 1U95 equalizer system. The input signal enters the first stage, labeled COMP4, which contains a series of six compressor modules (B3, B2, B1, B0, A3, A2, A1, A0). The output of COMP4 then passes through an equalizer stage (EQ), followed by a second stage labeled U159, which contains a series of six graphic equalizer modules (B3, B2, B1, B0, A3, A2, A1, A0). Finally, the signal passes through a third stage labeled COMP4, which contains a series of six compressor modules (B3, B2, B1, B0, A3, A2, A1, A0). The output of the final stage is labeled "Output".

The diagram illustrates a logic circuit composed of six AND2 gates (U163 through U168) and their connections to various buffers. The inputs for each AND2 gate are labeled as follows:

- U163:** IN1 = GND, IN2 = U164 OUT
- U164:** IN1 = GND, IN2 = U165 OUT
- U165:** IN1 = GND, IN2 = U166 OUT
- U166:** IN1 = GND, IN2 = U168 OUT
- U167:** IN1 = GND, IN2 = U168 OUT
- U168:** IN1 = GND, IN2 = U167 OUT

The outputs of these AND2 gates are connected to the following buffers:

- U163:** AND2 output connects to R1D1/EC02_BUF.
- U164:** AND2 output connects to R1D2/EC02_BUF.
- U165:** AND2 output connects to R1U1/EC02_B.
- U166:** AND2 output connects to R1D1/EC1...BUF.
- U167:** AND2 output connects to R1D2/EC1...BUF.
- U168:** AND2 output connects to R1D3/EC02_BUF.

Circuit diagram showing the connection of six AND2 gates (U163-U168) to RODP/EQ2_BUF buffers. The connections are as follows:

- U163 AND2 output → RODP/EQ2_BUF input
- U164 AND2 output → U163 AND2 input
- U165 AND2 output → RODP/EQ1_B BUF input
- U165 AND2 output → U166 AND2 input
- U166 AND2 output → RODP/EQ1_B BUF input
- U166 AND2 output → U167 AND2 input
- U167 AND2 output → RODP/EQ2_B BUF input
- U168 AND2 output → RODP/EQ2_B BUF input

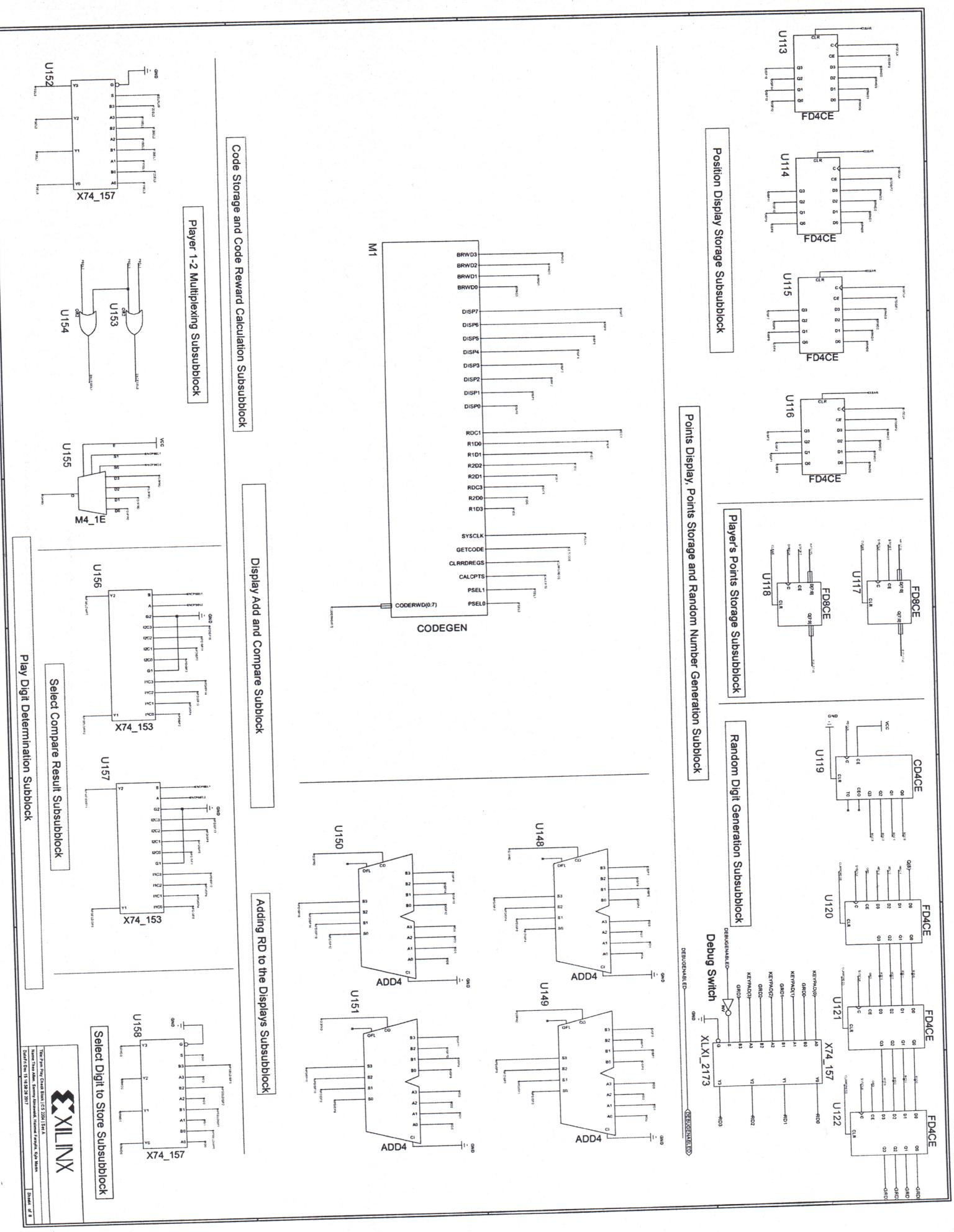
The diagram illustrates the internal logic of the X74_153 integrated circuit. It shows two main logic blocks, U169 and U170, connected to an output X74_153.

Block U169: This block contains a 4-to-16 decoder. Its inputs are labeled A, B, C, and D. The outputs of the decoder are labeled S1 through S15, plus a ground connection. The output S15 is connected to the output X74_153. The other outputs S1-S14 are connected to the inputs of block U170.

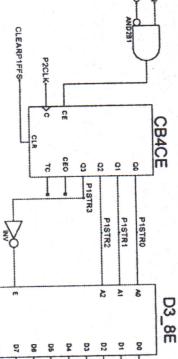
Block U170: This block contains a 16-to-1 multiplexer. Its inputs are labeled S1 through S15, plus a ground connection. The output of U170 is labeled Y1. The output Y1 is connected to the output X74_153. The control inputs for the multiplexer are labeled T1, T2, and T3.

Output X74_153: The final output of the circuit is labeled X74_153.

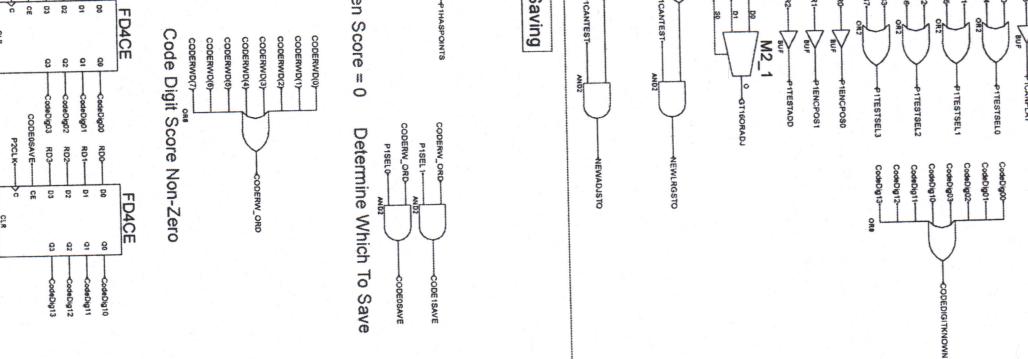
Adjacency Subblock



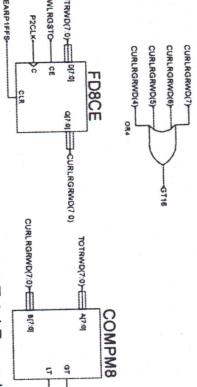
Sequencing Subblock



Control Signal Generation



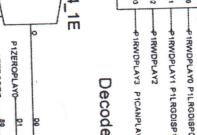
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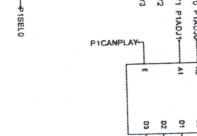
Largest Total Reward FF

Largest Total Reward Comp

Output



Decoders for the Positions

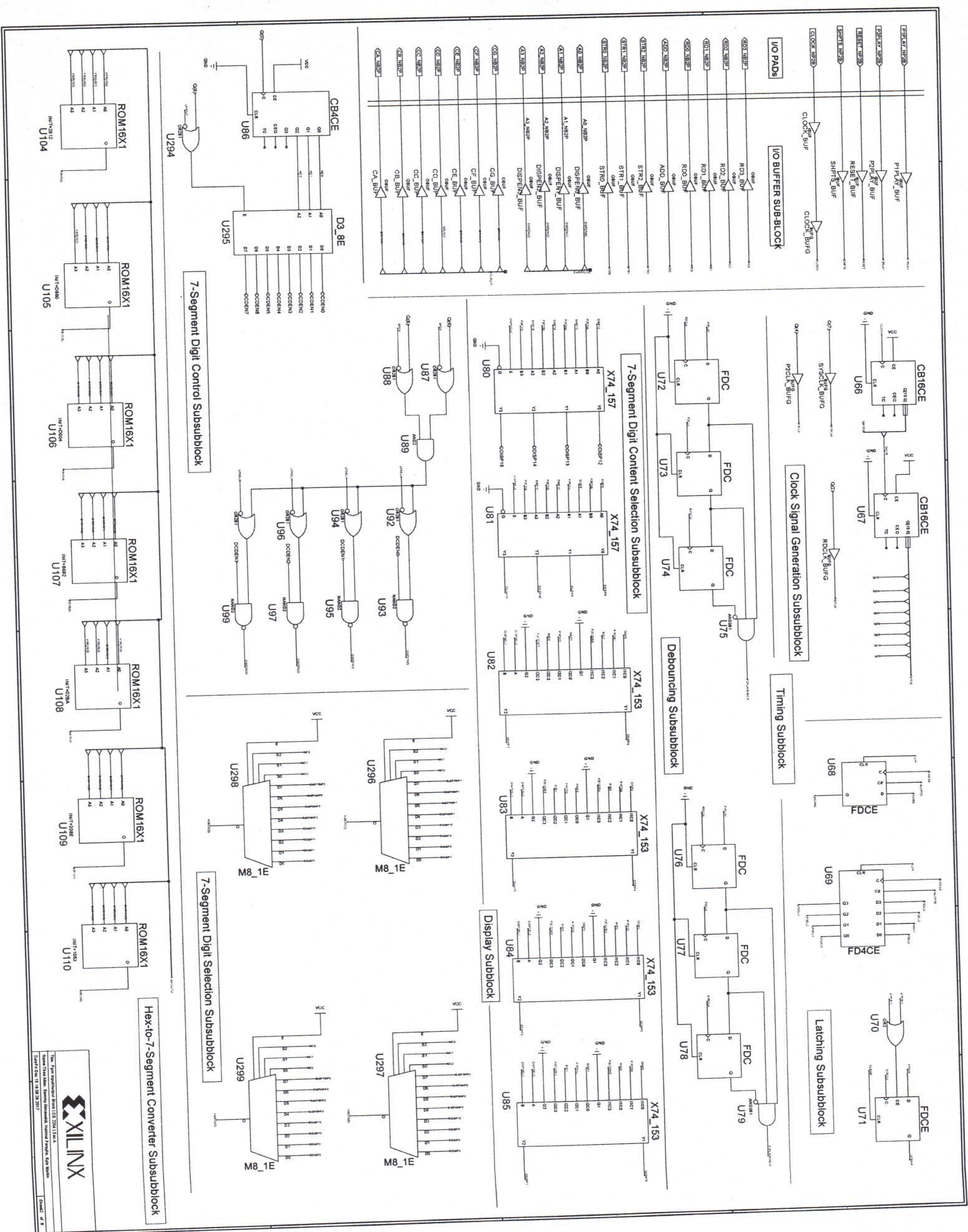


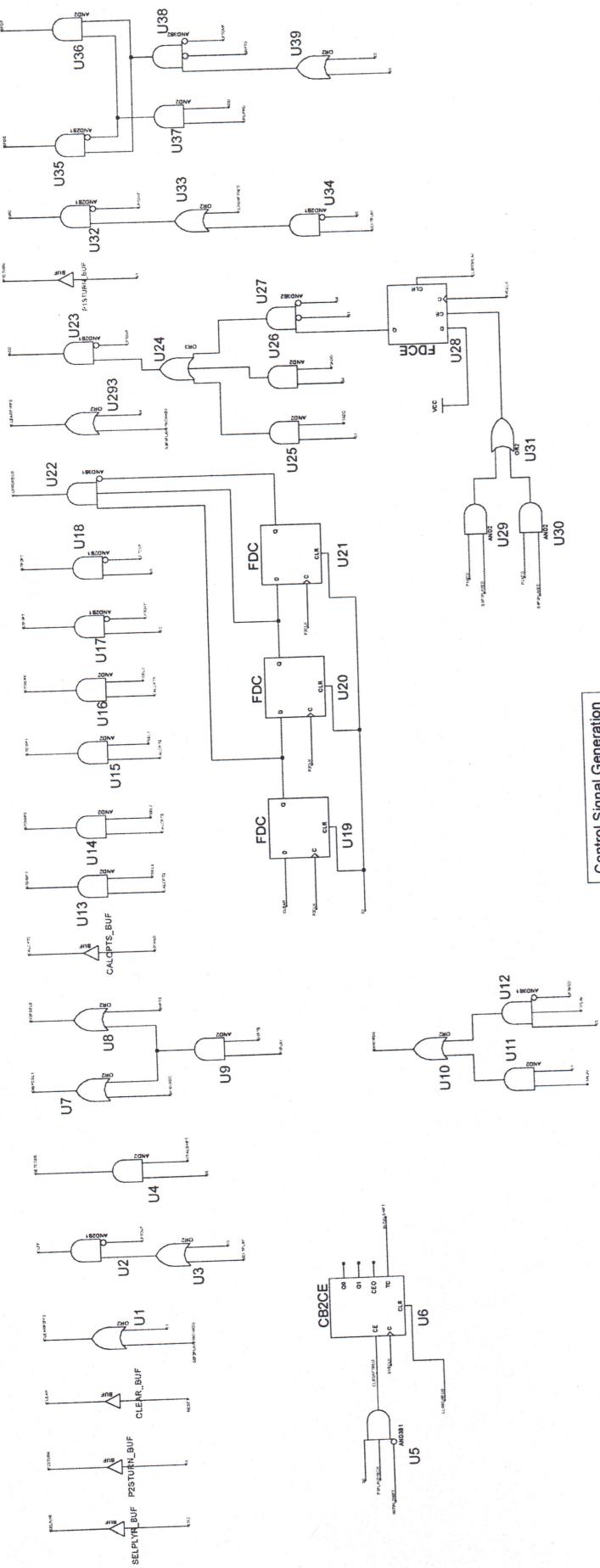
Output

D2_4E

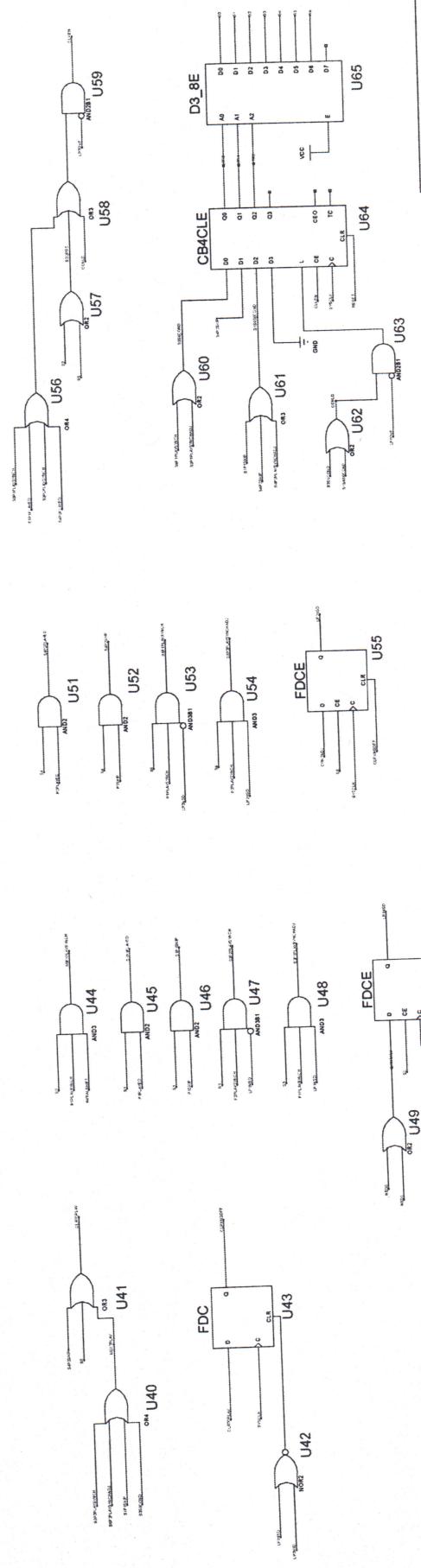
M4_1E

D2_4E





Control Signal Generation



XILINX

Part: Pin Configuration CS220015-A
Name: File Name: Survey Altimeter - Home / Projects / Xilinx
Date File Date: 01/15/06 20:20:00

Sheet 8