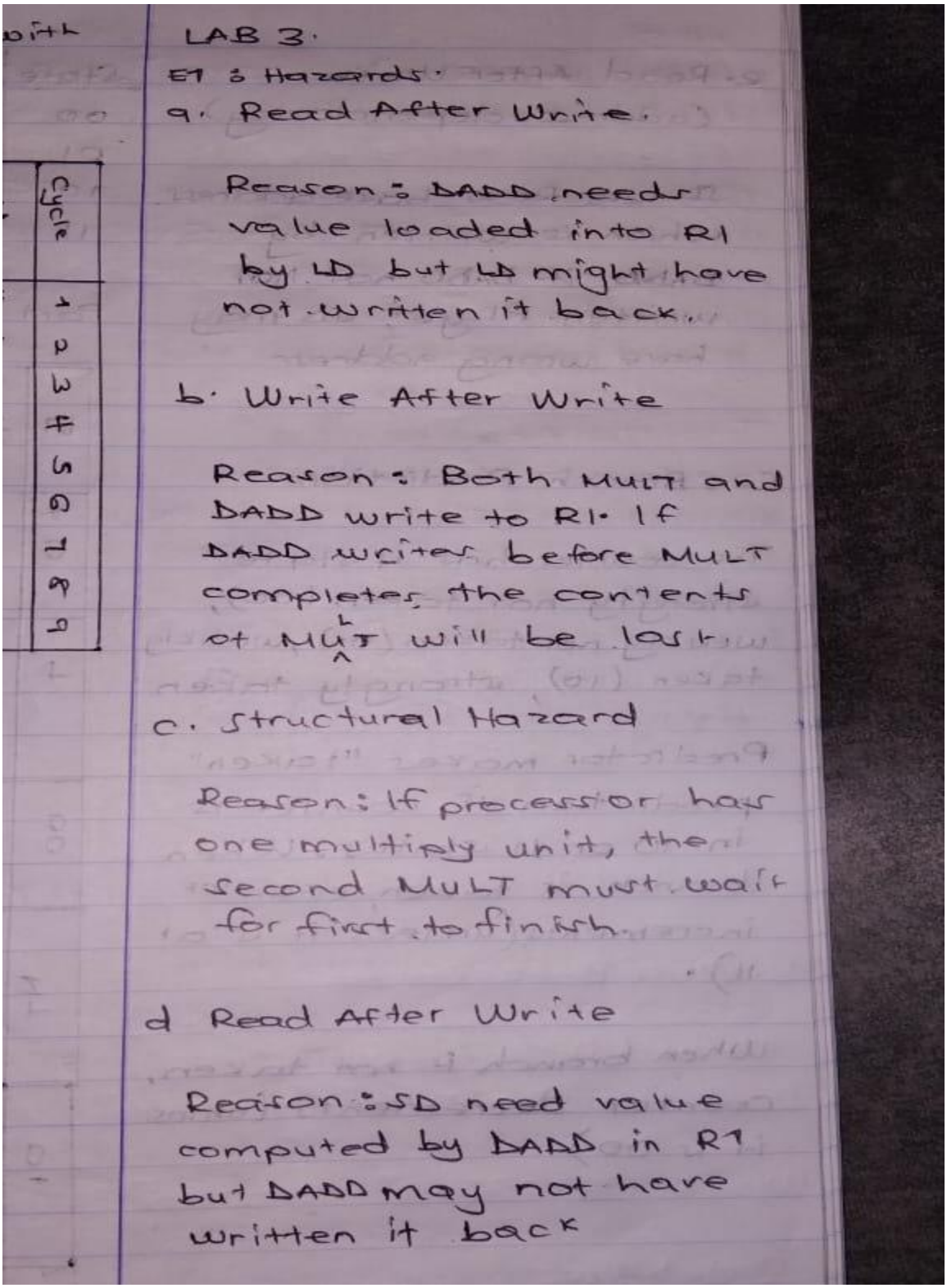
WANJOHI ELVIS MUTHUMBI. SCT212-0043/2021

COMPUTER ARCHITECTURE. LAB 3.



with

Cycle
1
2
3
4
5
6
7
8
9

LAB 3.

E1 : Hazards.

a. Read After Write.

Reason : DADD needs value loaded into R1 by LD but LD might have not written it back.

b. Write After Write

Reason : Both MULT and DADD write to R1. If DADD writes before MULT completes, the contents of MULT will be lost

c. Structural Hazard

Reason: If processor has one multiply unit, the second MULT must wait for first to finish.

d Read After Write

Reason : SD need value computed by DADD in R1 but DADD may not have written it back

e. Read After Write (address dependancy)

SD uses R1 as base address which is written by DADD, if DADD has not written R1 yet, SD may have wrong address

E2: Branch Prediction.

The counter has 4 state strongly not taken (00), weakly not taken (01), weakly taken (10), strongly taken

Predictor makes "taken" prediction if counter is in 10 or 11 states. When branch is taken, counter increments (unless it is at 11).

When branch is not taken, counter decrements (unless it is 00)

NT → Not taken
T → Taken

State	Name	Pred	On Tak	Not Tak
00	SNT	NT	01	00
01	WNT	NT	10	00
10	WT	T	11	01
11	ST	T	11	10

Part B.

Iteration	x(i)	Outcome	Counter Before	Prediction	Counter After	Correct?
0	0	NT	00	NT	00	Y
1	≠0	T	00	NT	01	N
2	0	NT	01	NT	00	Y
3	≠0	T	00	NT	01	N
4	0	NT	01	NT	00	Y
5	≠0	T	00	NT	01	N