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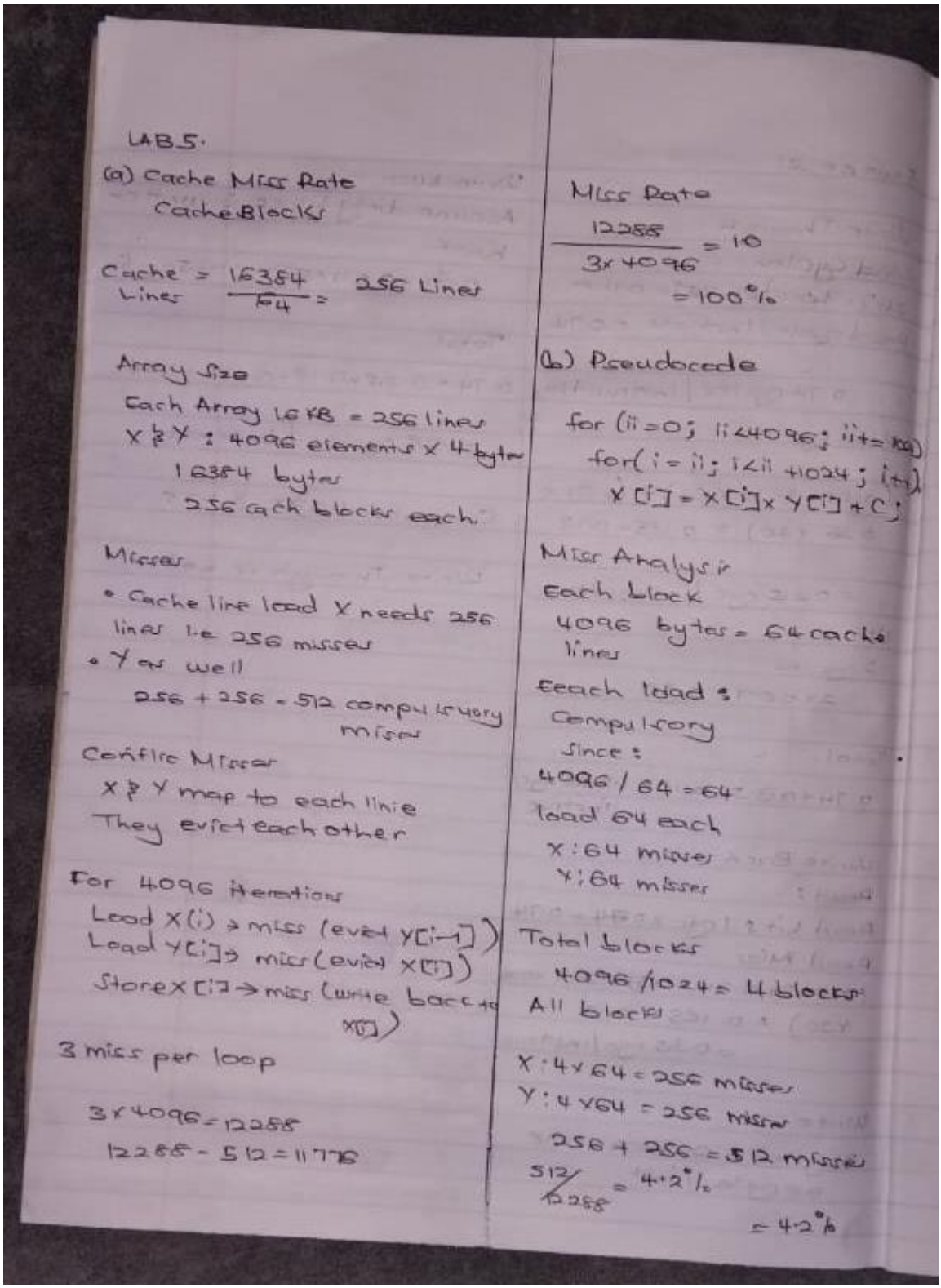
COMPUTER ARCHITECTURE. LAB 5.



LAB 5.

(a) Cache Miss Rate

Cache Blocks

Cache Lines = 16384 / 64 = 256 Lines

Array Size

Each Array 16 KB = 256 lines

X & Y : 4096 elements x 4 bytes

16384 bytes

256 each blocks each

Misses

- Cache line load X needs 256 lines i.e 256 misses
- Y as well

256 + 256 = 512 compulsory misses

Conflict Misses

X & Y map to each line

They evict each other

For 4096 Iterations

Load X(i) → miss (evict Y[i-1])

Load Y[i] → miss (evict X[i])

Store X[i] → miss (write back X[i])

3 miss per loop

3 x 4096 = 12288

12288 - 512 = 11776

Miss Rate

12288 / (3 x 4096) = 10

= 100%

(b) Pseudocode

```
for (ii=0; ii<4096; ii+=1024)
  for(i=ii; i<ii+1024; i++)
    X[i] = X[i] x Y[i] + C;
```

Miss Analysis

Each block

4096 bytes = 64 cache lines

Each load:

Compulsory

Since:

4096 / 64 = 64

load 64 each

X: 64 misses

Y: 64 misses

Total blocks

4096 / 1024 = 4 blocks

All blocks

X: 4 x 64 = 256 misses

Y: 4 x 64 = 256 misses

256 + 256 = 512 misses

512 / 12288 = 4.2%

= 4.2%

c) Hardware Solution

Solution : 2 way set Associative Cach.

Instead of direct map, use 2 way cache

Now

X[i] & Y[i] reside with same i can reside in different ways in same set avoiding conflict miss