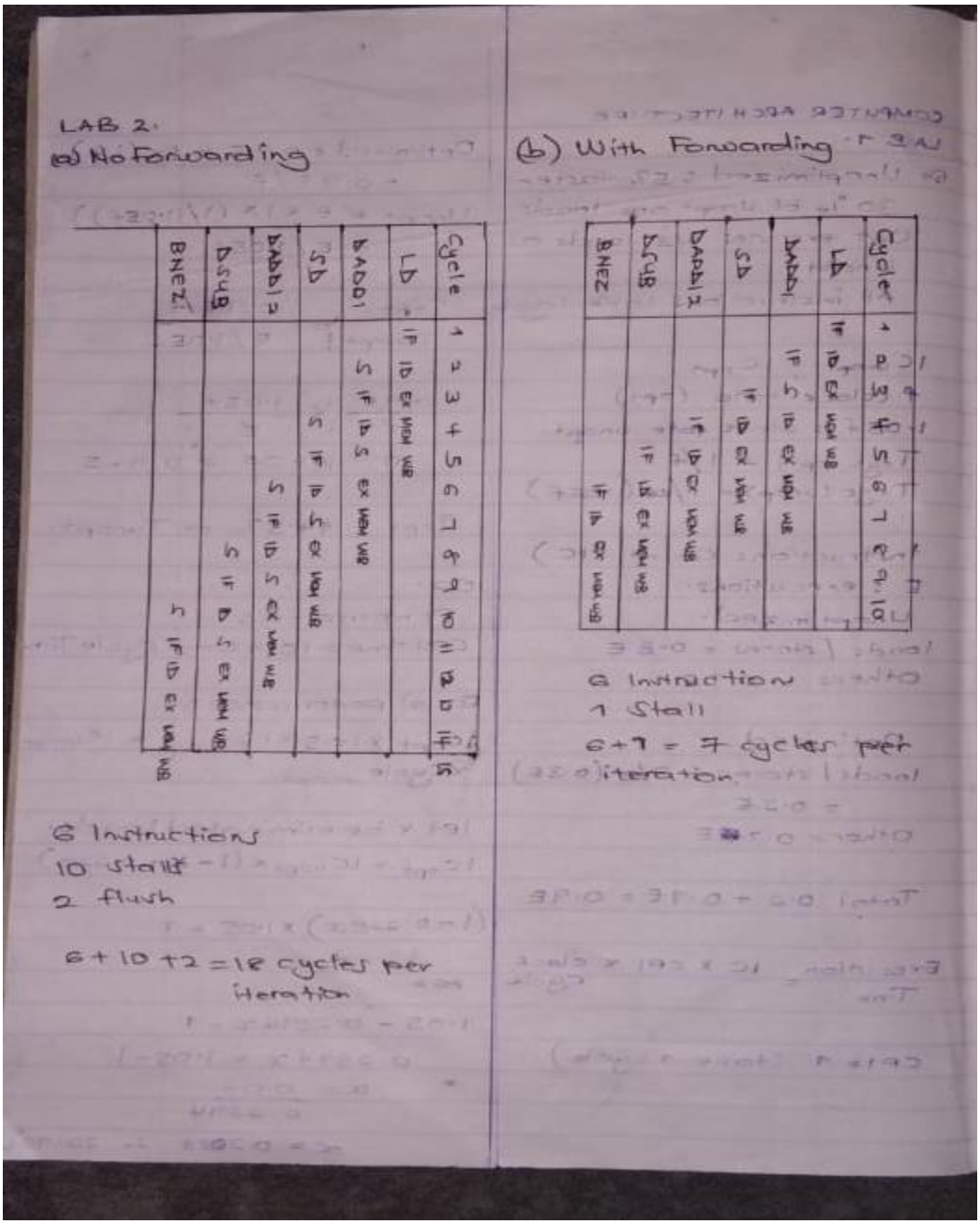
WANJOHI ELVIS MUTHUMBI. SCT212-0043/2021

COMPUTER ARCHITECTURE. LAB 2.



Single Cycle Delayed with Forwarding:

Cycle	1	2	3	4	5	6	7	8	9
LD	IF	ID	EX	MEM	WB				
DADD 1		IF	S	ID	EX	MEM	WB		
CJP			IF	D	EX	MEM	WB		
DADD 12				IF	D	EX	MEM	WB	
DSUB					IF	D	EX	MEM	WB
BNEZ						IF	D	EX	MEM
NOP							IF	D	EX

6 Instructions
1 Stall
1 delay

6+1+1 = 8 cycles per iteration.