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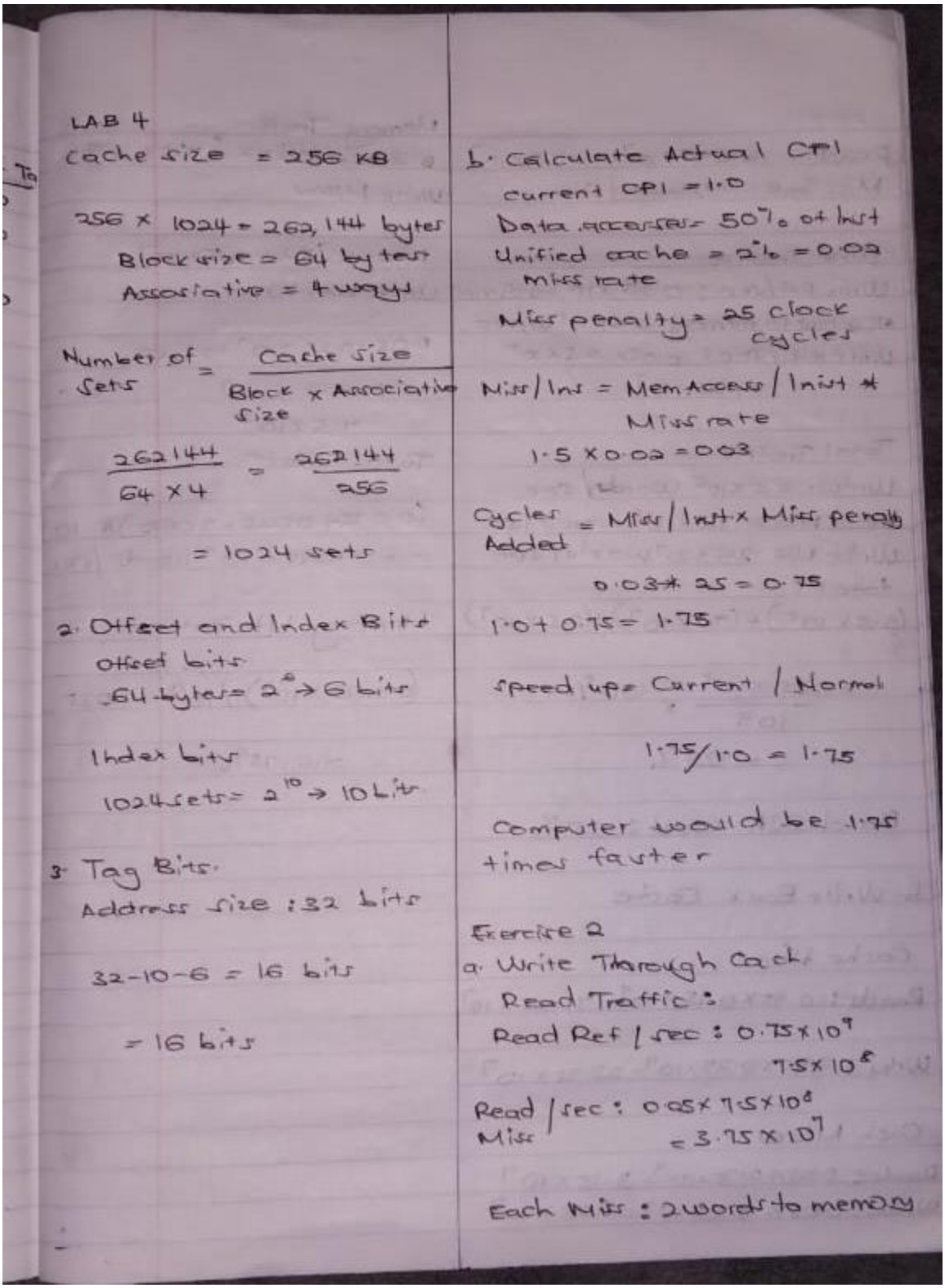
COMPUTER ARCHITECTURE. LAB 4.



LAB 4

Cache size = 256 KB

256 × 1024 = 262,144 bytes

Block size = 64 bytes

Associative = 4 ways

Number of Sets = Cache size / (Block × Associative size)

262144 / (64 × 4) = 262144 / 256

= 1024 sets

2. Offset and Index Bits

offset bits

64 bytes = 2^6 → 6 bits

Index bits

1024 sets = 2^{10} → 10 bits

3. Tag Bits.

Address size : 32 bits

32 − 10 − 6 = 16 bits

= 16 bits

b. Calculate Actual CPI

current CPI = 1.0

Data accesses = 50% of Inst

Unified cache = 2% = 0.02 Miss rate

Miss penalty = 25 clock cycles

Miss/Ins = Mem Access / Inst * Miss rate

1.5 × 0.02 = 0.03

Cycles Added = Miss/Inst × Miss penalty

0.03 * 25 = 0.75

1.0 + 0.75 = 1.75

speed up = Current / Normal

1.75 / 1.0 = 1.75

Computer would be 1.75 times faster

Exercise 2

a. Write Through Cache

Read Traffic :

Read Ref / sec : 0.75×10^9

7.5×10^8

Read / sec Miss : $0.05 \times 7.5 \times 10^8$

$= 3.75 \times 10^7$

Each Miss : 2 words to memory

Read Miss Traffic = $3.75 \times 10^7 \times 2 = 7.5 \times 10^7$ Words / sec

Write Traffic

Write Ref/sec : $0.25 \times 10^9 = 2.5 \times 10^8$

All writes to memory 2.5×10^5 w/sec

Write miss/sec : $0.05 \times 2.5 \times 10^8$

$= 1.25 \times 10^7$

Total Traffic

Writes: 2.5×10^5 words/sec

Read Miss = 7.5×10^7 words/sec

Write Miss 2.5×10^7 words/sec

total :

$(2.5 \times 10^5) + (7.5 \times 10^7) + (2.5 \times 10^7)$

$= \frac{3.5 \times 10^8}{10^9} \times 100\%$

$= 35\%$

Bandwidth used : 35%

b. Write Back Cache

Cache Hits

Reads : $0.95 \times 0.75 \times 10^9 = 71.25 \times 10^7$

Writes : $0.95 \times 0.25 \times 10^9 = 23.75 \times 10^7$

Cach Misses

Reads : $0.05 \times 0.75 \times 10^9 = 3.75 \times 10^7$

Writes : $0.05 \times 0.25 \times 10^9 = 1.25 \times 10^7$

Memory Traffic

$3.75 \times 10^7 \times 2 = 7.5 \times 10^7$

Write Misses

$1.25 \times 10^7 \times 2 = 2.5 \times 10^7$

Write backs

$0.05 \times 0.25 \times 10^9 \times 0.3 \times 2$

$= 0.0075 \times 10^9$

7.5×10^6

Total Traffic

$(0.0754 0025 + 0.0075) * 10^9$

$= 0.1075 \times 10^9$ words / sec

Memory Utilization

$(0.1075 \times 10^9) / 10^9 = 01075$

$= 10.75\%$

Exercise 3:

Write Through

Read Cycles

26% Loads, 74% other

Read cycle / Instructs = 0.74

0.74 cycles / instruction

Miss cycles

(0.005 × 0.74 × 50) + (0.01 × 0.26 × 50) = 0.185 + 0.13

= 0.315 cyc / instruction

Write

2 cycles

2 × 0.09 = 0.18

Total

0.74 + 0.315 + 0.18 = 1.235 cyc / instruc

Write Back

Read:

Read Hits: 1 cyc × 0.74 = 0.74

Read Miss

(0.005 × 0.74 × 0.5) + (0.01 × 0.26 × 50) = 0.185 + 0.13

= 0.315 cyc / instruc

Write

2 cycles: 2 × 0.09 = 0.18

0.18 cycles / inst

Write Miss

Assume dirty block is written back.

0.01 × 0.09 × 50 = 0.045 cyc / in

Total

0.74 + 0.315 + 0.18 + 0.045 = 1.28

= 1.28 cycles / instruction

Compare 1.235 ≯ 1.28

Write Through is better.