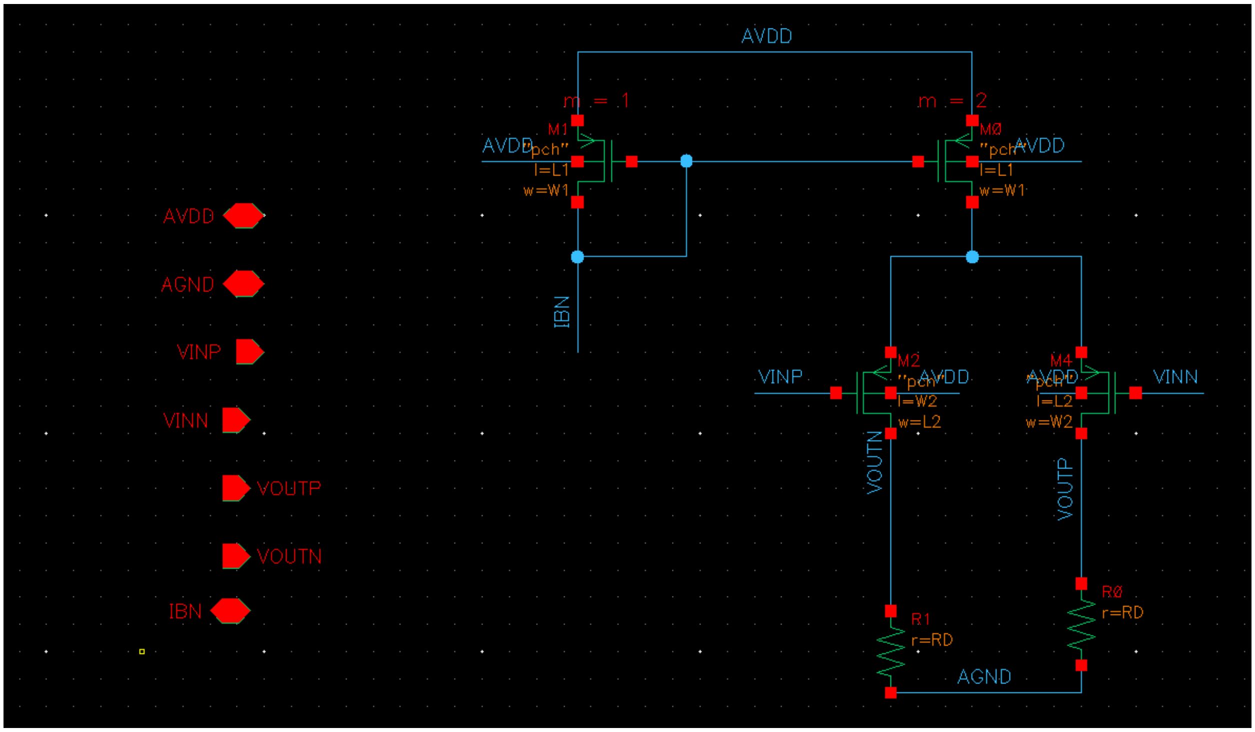
PART 1: Differential Amplifier Design

1 CIRCUIT



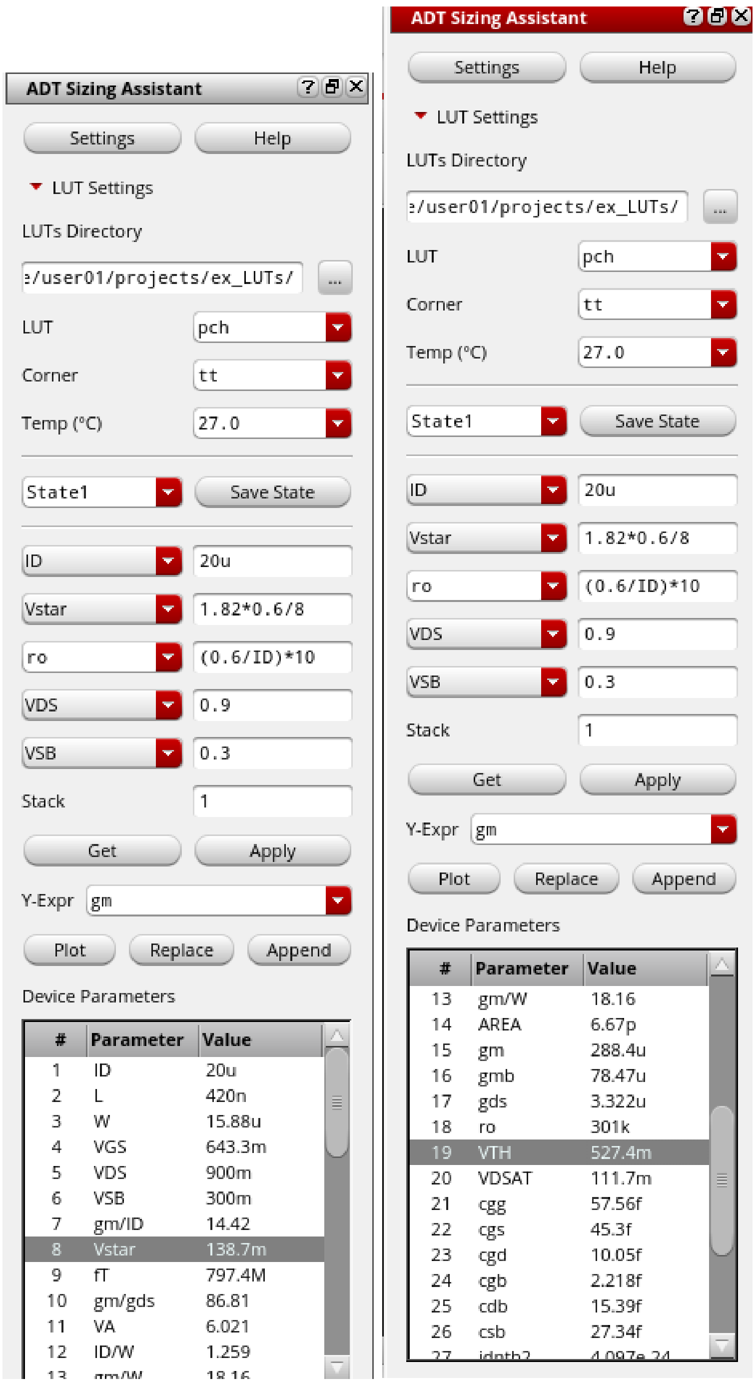
2 CHOOSE $\boldsymbol{RD}$ TO MEET THE CM OUTPUT LEVEL SPEC.

$$RD = \frac{0.6}{20u} = 30k$$

3 CHOOSE $\boldsymbol{V*}$ TO MEET THE DIFFERENTIAL GAIN SPEC.

$$V* = \frac{1.82VRD}{|Av|} = 136.5mv$$

4 Assume we will set VDS of the tail current source to $300mV$ to allow more output swing. Report the input pair sizing using SA.



L2=420n & W2=15.88u & VTH=527.4mv & |VGS|=643.3mv

5 Give the above assumption, calculate the CM input level. Calculate the min and max CM input levels. Is the selected CM input level in the valid range?

Min : VICMmin = IRD – VTH = 0.6-0.5274= 72.6 mV

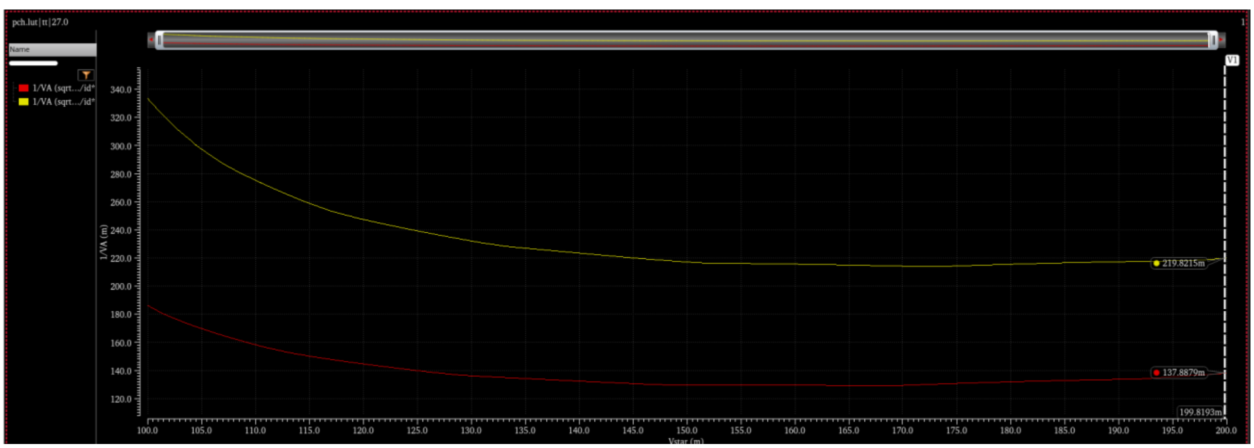
Max: ViCMmax= -VSG+VDS+VDD=-643.3 m -138.7 m+1.8=1.018 V

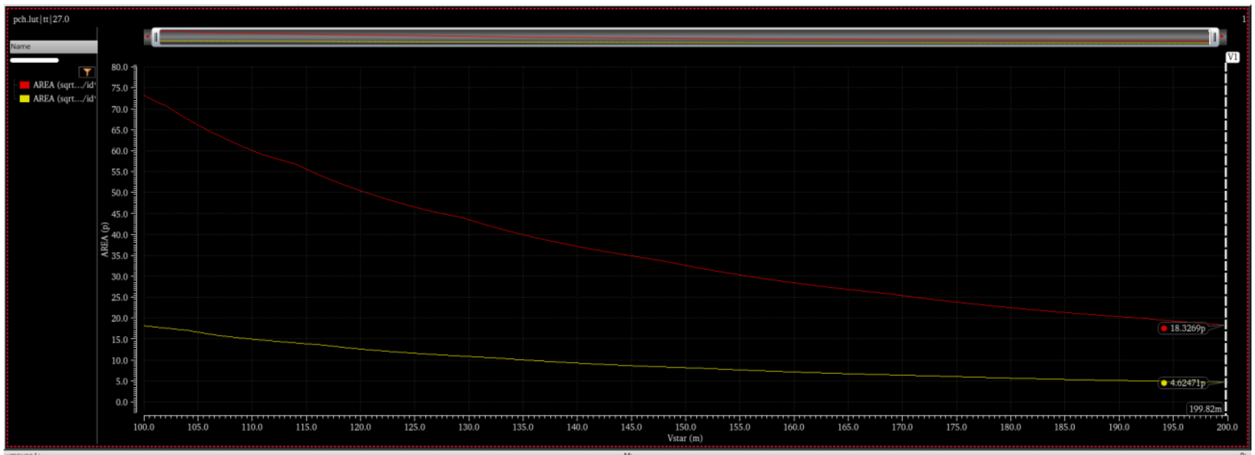
the CM input level: VICM=-643.3 m-300 m+1.8=856.7mv

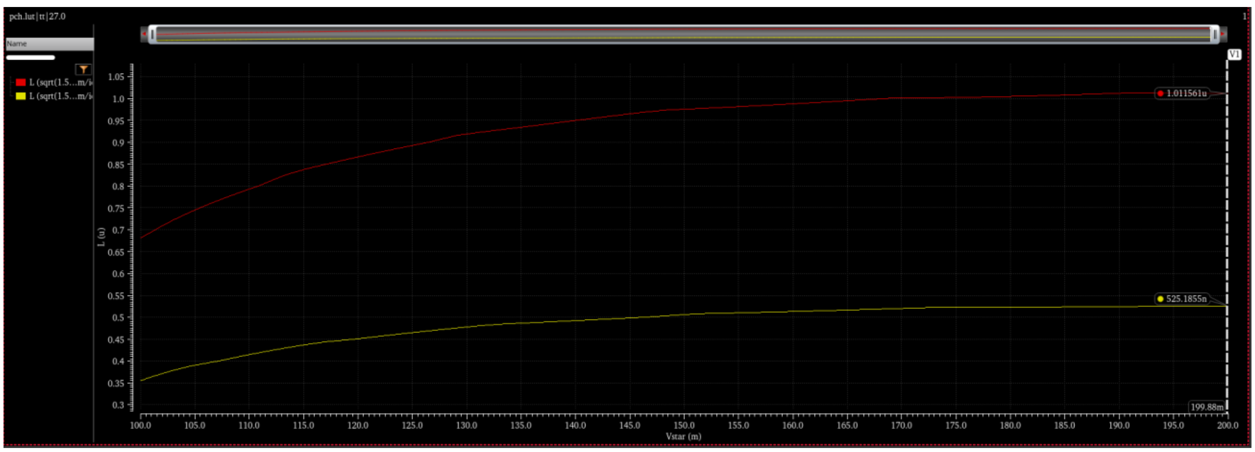
yes, the selected CM input level in the valid range

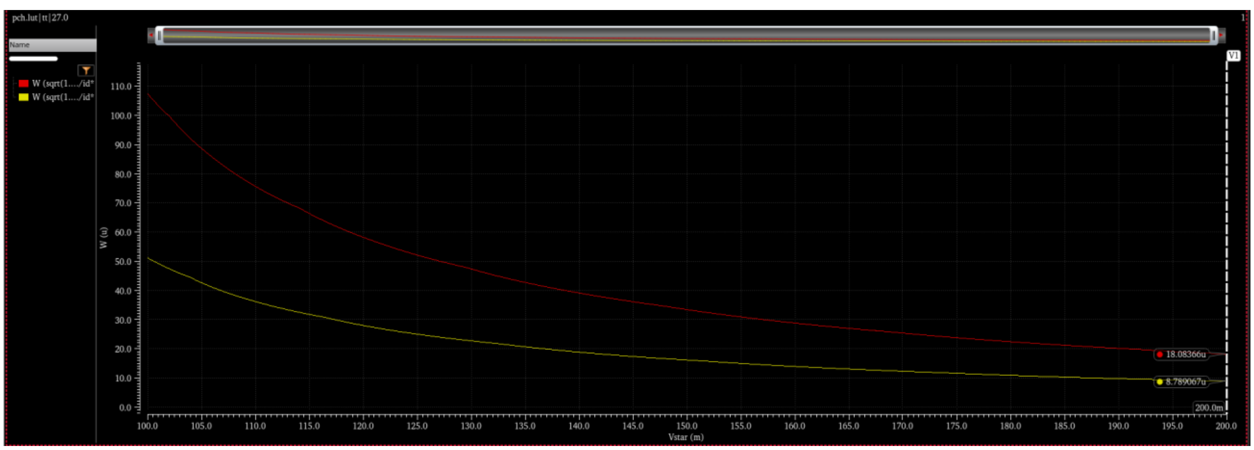
6 Sizing the tail current source

ID	20u
Vstar	100m:200m
sqrt(1.5)*3.5m/sqrt(W*L*1e12)*gm/ID*100	1,2
VDS	0.3
VSB	0









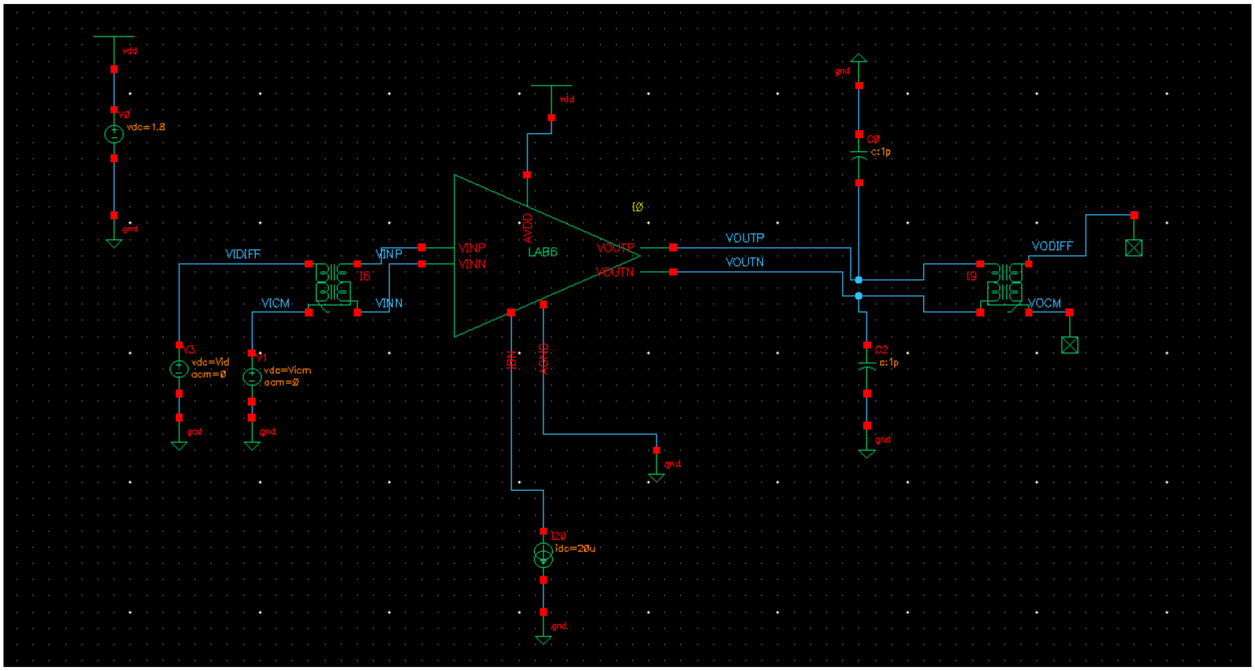
L=525.18n

W=8.8u

At V^* = 200mv (the minimum mismatch is achieved at the max $V*$)

Part 2: Differential Amplifier Simulation

1 SCHEMATIC



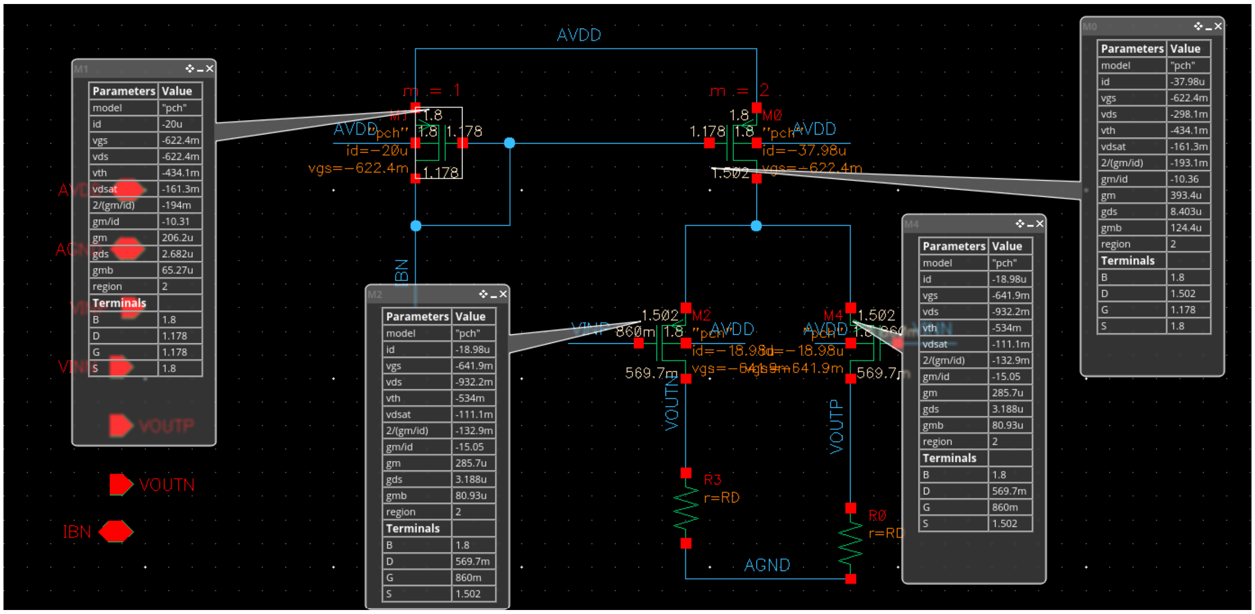
2 SET THE TRANSISTOR SIZING AND VICM AS DESIGNED IN PART 1.

Design Variables

L1	525.17n
L2	420n
RD	30k
Vicm	0.86
Vid	0
W1	8.8u
W2	15.88u

Click to add variable

1 REPORT THE SCHEMATIC OF THE DIFF PAIR WITH DC OP POINT CLEARLY ANNOTATED.

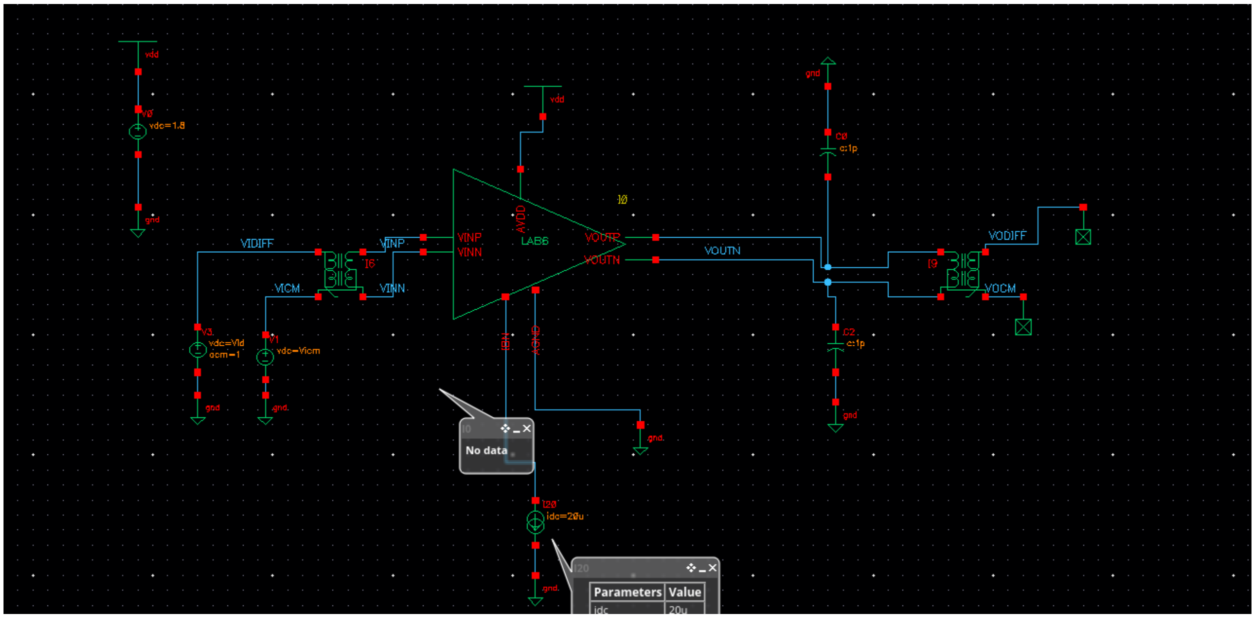


1.1 CHECK THAT ALL TRANSISTORS OPERATE IN SATURATION.

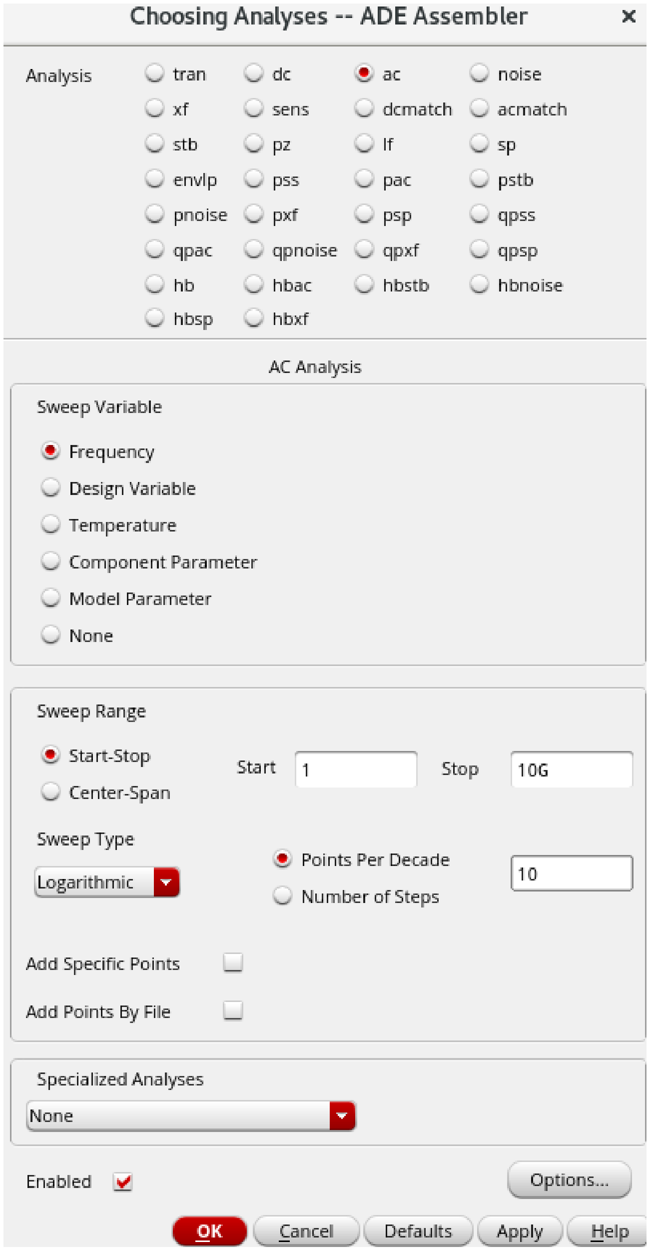
YES, they are all in region(2) saturation.

2 DIFF SMALL SIGNAL CCS:

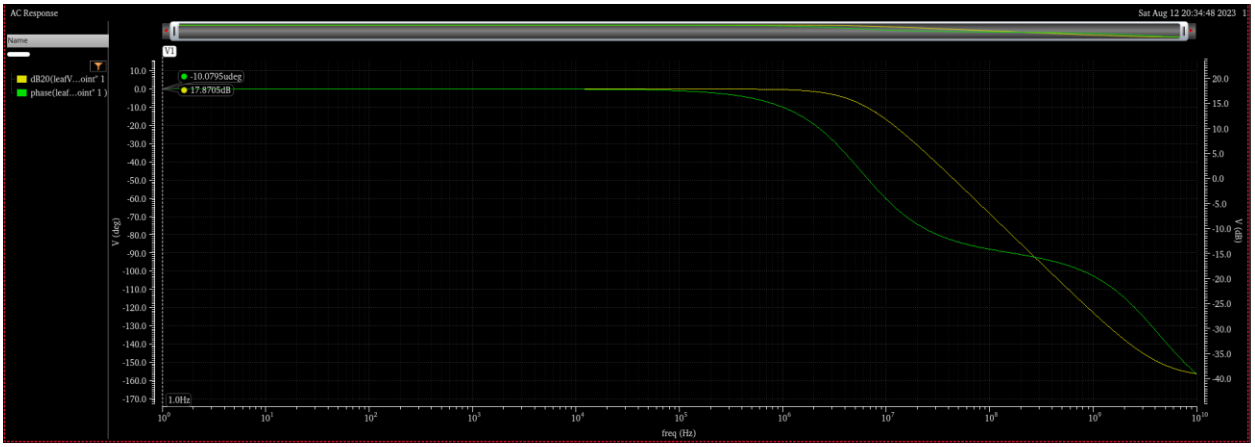
2.1 USE AC MAGNITUDE = 1 FOR THE DIFF SOURCE (AND AC MAGNITUDE = 0 FOR THE CM SOURCE).



2.2 Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).



2.3 Report the Bode plot of small signal diff gain.



lab5_LAB6PART...	ymax(mag(VF("/...	7.826			
lab5_LAB6PART...	bandwidth(VF("/...	5.696M			
lab5_LAB6PART...	ymax(dB20(VF("...	17.87			

Analytically :

Gain=gm2 (RD//ro2)= 285.8u*27.38k =7.82

In db : 20log(7.82)= 17.86 db

Rth= (ro2 (gm+gmb)*r0) // RD = RD

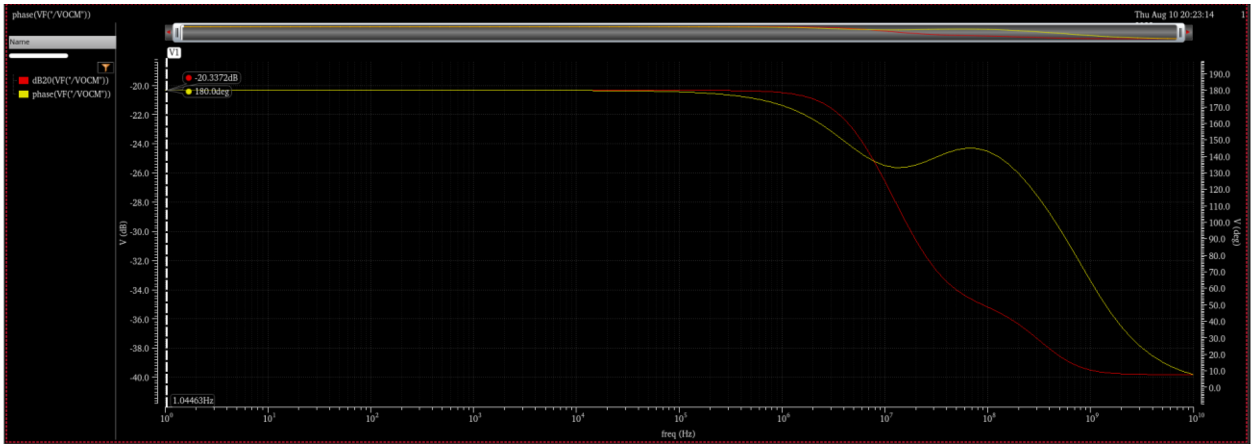
ω=1/RCL=33.4 M

f=ω/2pi=5.3 MHZ

	SIM	ANALYTICAL
DC diff gain	17.87 db	17.86 db
BW	5.7 MHZ	5.3MHZ

3 CM SMALL SIGNAL CCS:

3.1



3.2

lab5_LAB6PART...	ymax(dB20(VF("...	-20.34			

3.3 COMPARE THE DC CM GAIN WITH HAND ANALYSIS IN A TABLE. IS IT SMALLER THAN "1"? WHY?

$$Avcm = \frac{-gm2 * RD}{1 + 2(gm2 + gmb2) * ro0} = \frac{-285.7u * 30K}{2(285.7 + 80.93) * \frac{1}{8.403}} = 0.0982$$

$$= -20.15\ DB$$

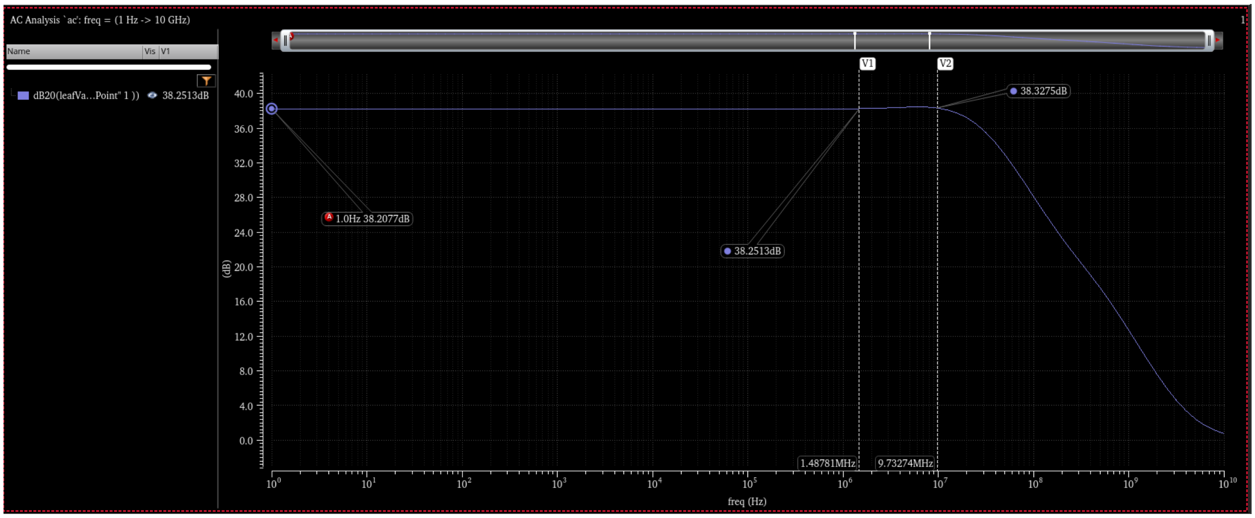
SIM	ANALYTICAL
-20.34 DB	-20.15 DB

YES, it's smaller than 1 (in decimal scale), as cm input is partially rejected and attenuated.

3.4 JUSTIFY THE VARIATION OF AVCM VS FREQUENCY.

the pole at the output causes the Avcm to start dropping at high frequency as CL is large, so it is dominant, but also there is a zero caused by the capacitances at the tail current source causes it to fall at a slower rate, as Cp degrades tail current source impedance at high frequency making bigger gain (if we neglected the changes in output impedance at high frequency).

3.5 Plot Avd/Avcm in dB. Compare Avd/Avcm @ DC with hand analysis in a table.



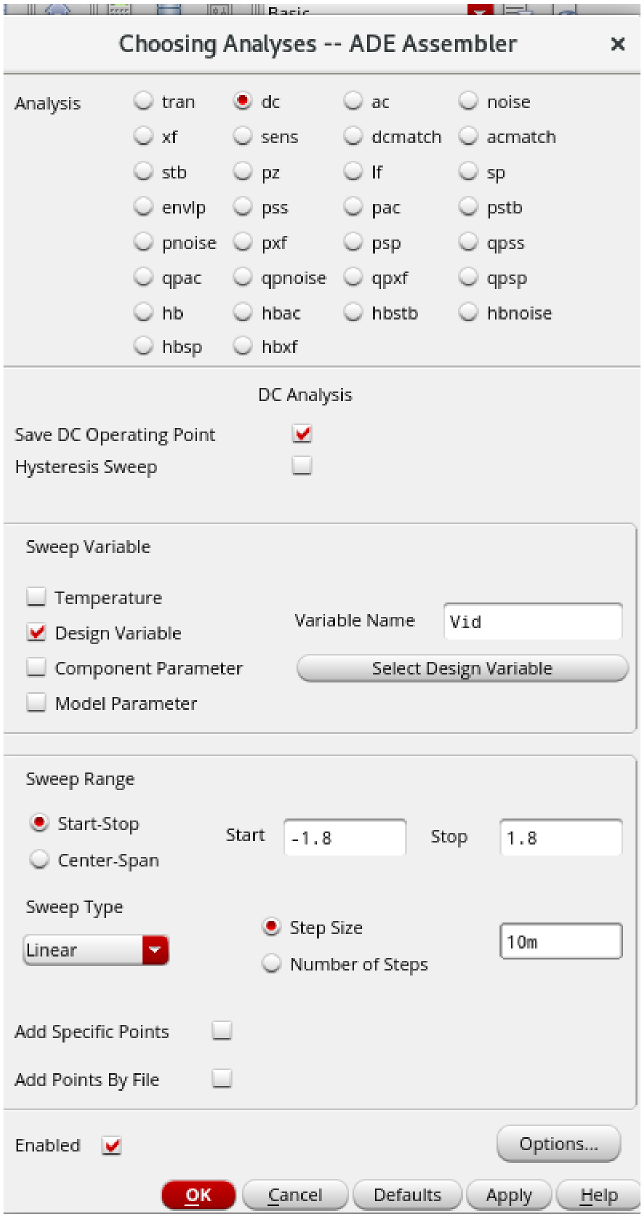
SIM	ANALYITALC
38.2DB	20log($\frac{7.82}{0.0982}$)=38.02 DB

3.6 Justify the variation of Avd/Avcm with frequency

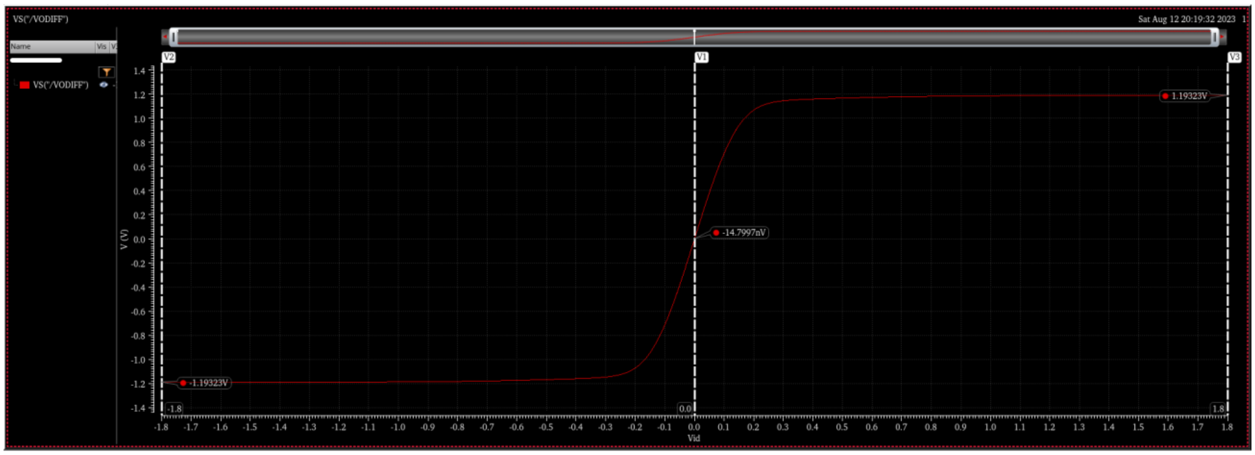
there is a zero made a short increase, as it was a pole caused AVCM to decrease, There is also a pole because of cp degrades tail current source impedance at high frequency making Avcm make more gain so the ratio itself decreases.

4 DIFF LARGE SIGNAL CCS:

4.1 USE DC SWEEP (NOT PARAMETRIC SWEEP) FOR VID = -VDD:10M:VDD.



4.2 REPORT DIFF LARGE SIGNAL CCS (VODIFF VS VIDIFF). COMPARE THE EXTREME VALUES WITH HAND ANALYSIS IN A TABLE.



VOP (@ vid=1.8v)=RD*ISS=30k*40u=1.2v

VON (@ vid=1.8v)=0

VOD(@ vid=1.8v) = 1.2v

VOP (@ vid=-1.8v)=0

VON (@ vid=-1.8v)= 30k*40u=1.2v

VOD(@ vid=-1.8v) =0-1.2v= -1.2v

VOP (@ vid=0v)= 30k*20u=0.6v

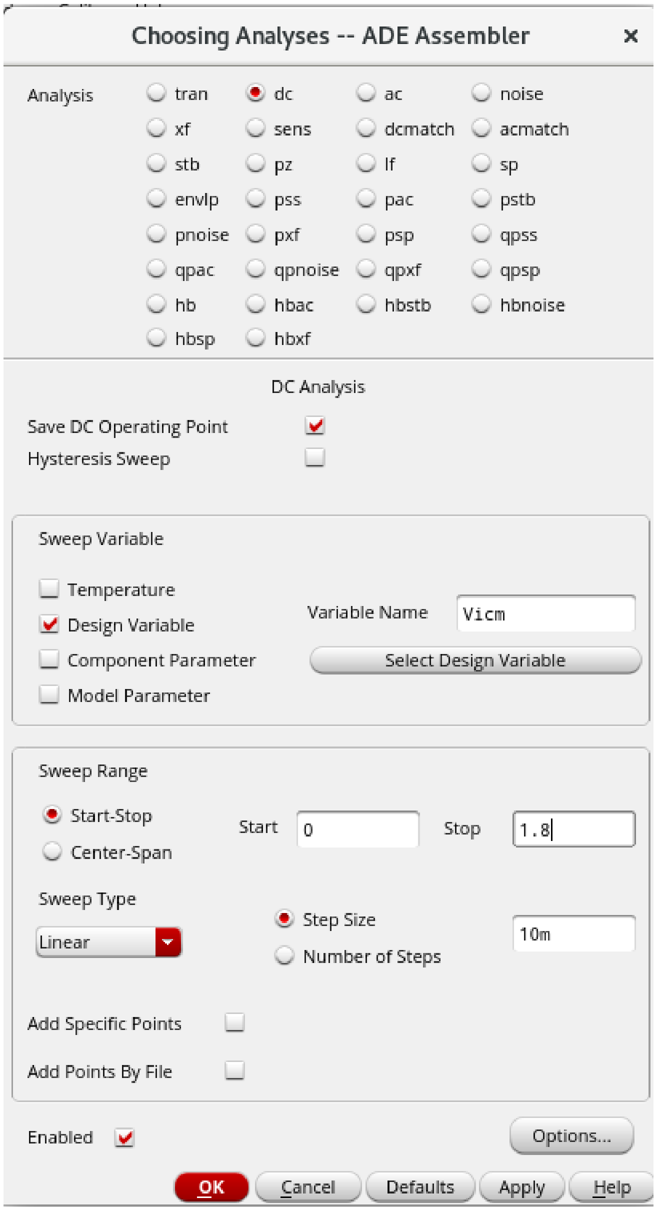
VON (@ vid=0v)= 30k*20u=0.6v

VOD(@ vid=0v) =0.6-0.6v=0v

	Sim	analytical
-1.8	-1.19	-1.2
0	15 n	0
1.8	1.19	1.2

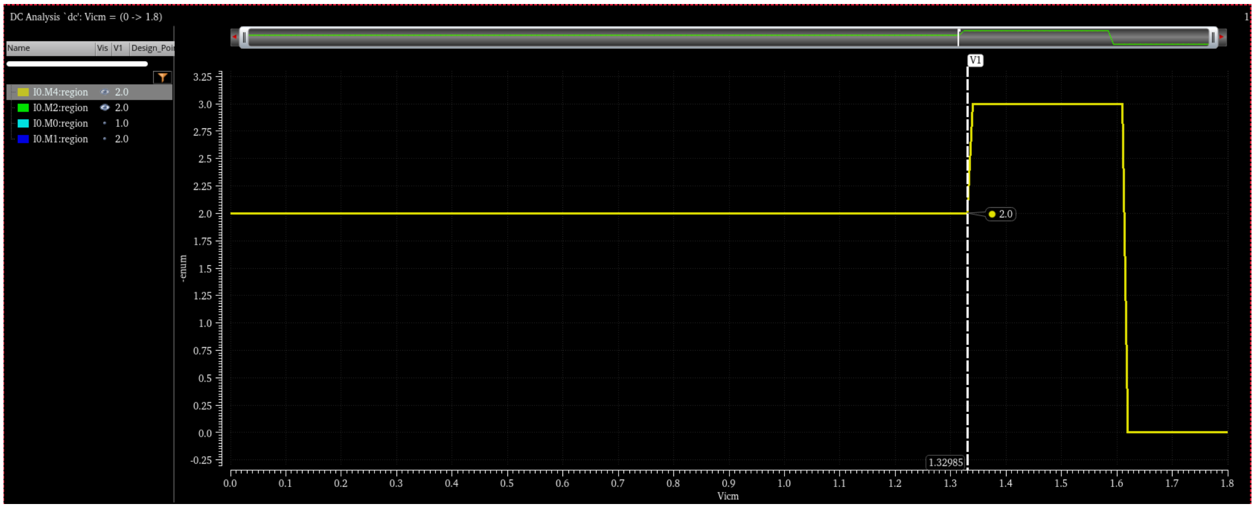
5 CM LARGE SIGNAL CCS (REGION VS VICM):

5.1 USE DC SWEEP (NOT PARAMETRIC SWEEP) FOR VICM = 0:10M:VDD (NO NEED TO RUN AC SIM)

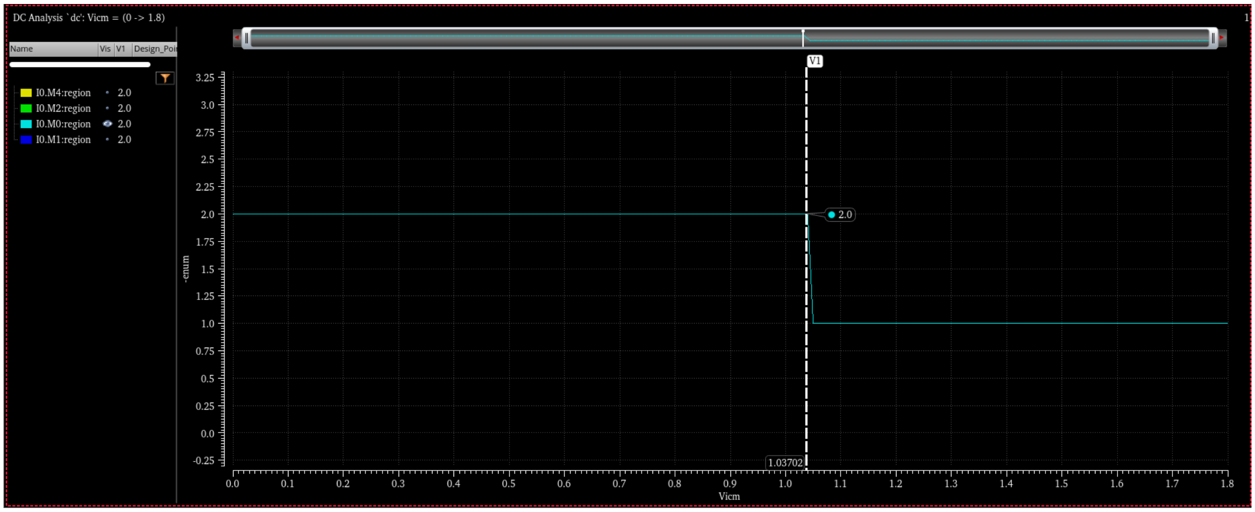


5.2 Plot "region" OP parameter vs Vicm for the input pair and the tail current source.

INPUT PAIR:



TAIL CURRENT:



5.3 Find the CM input range (CMIR). Compare with hand analysis in a table.

To keep the input pair and the tail current source both in saturation (region 2) the range is 0 to 1.037v from the graph.

ANALYTICALLY:

Min : VICMmin = IRD – VTH = 35.4mV

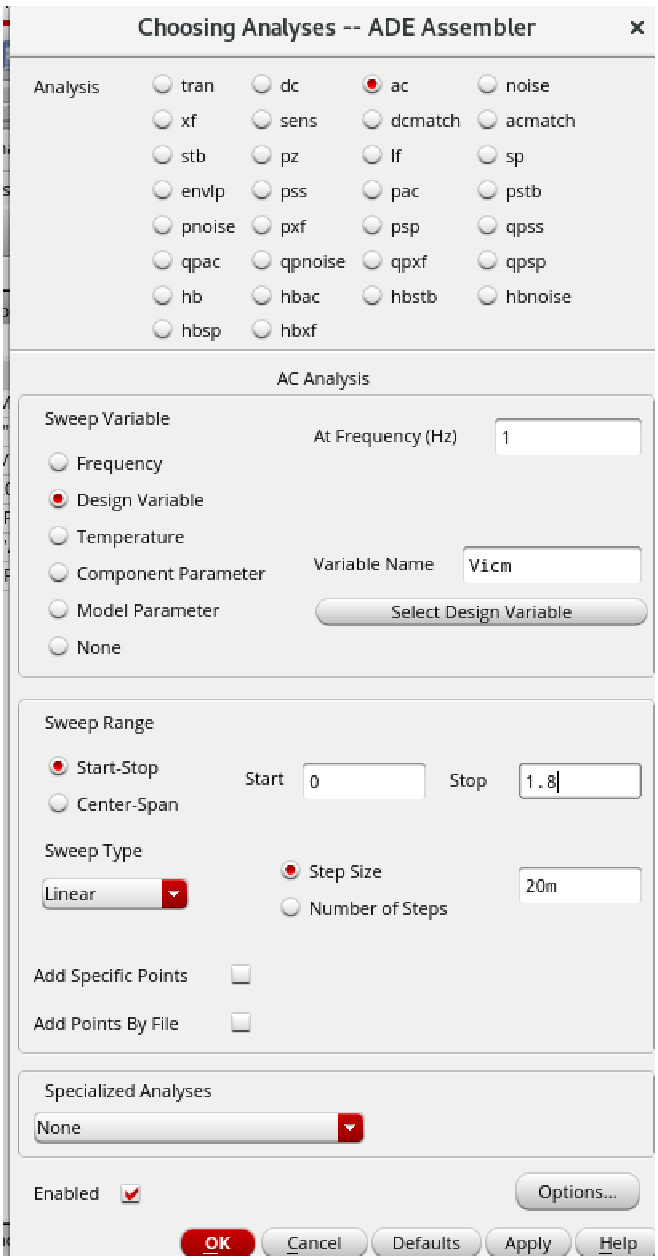
Max: ViCMmax= -VSG2-V*+VDD=-641.9 m -193.1 m +1.8=965m

= 965m-35.4m=929.6mv

SIM	ANALYTICALLY
1.037	929.6mv

6 CM LARGE SIGNAL CCS (GBW VS VICM):

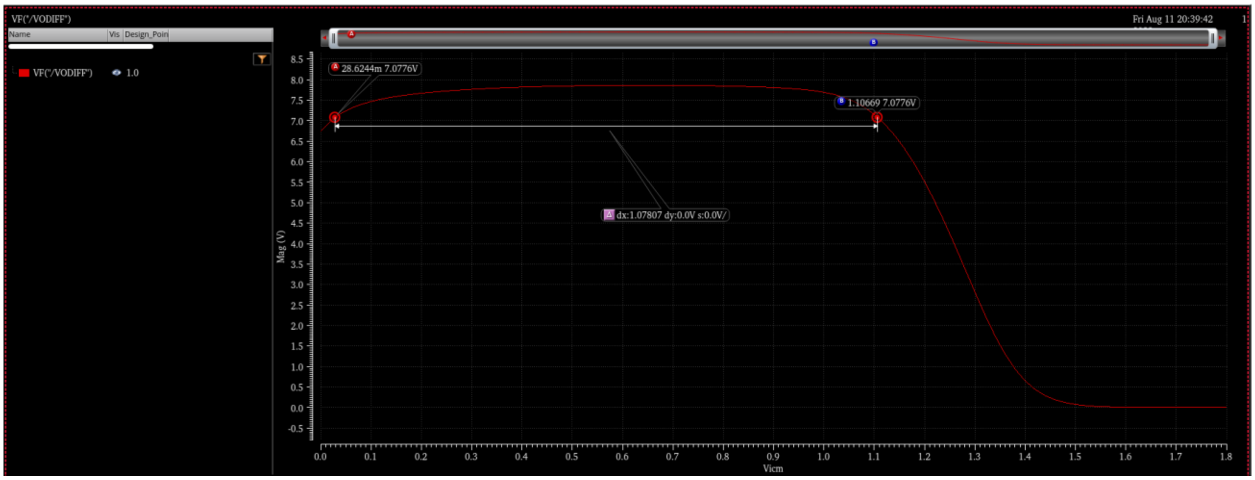
6.1 USE AC ANALYSIS (START = 1, STOP = 1, PTS(LINEAR) = 1) TO GET AVD. USE PARAMETRIC SWEEP (NOT DC SWEEP) FOR VICM = 0:20M:VDD.



lab5_LAB6PART...	ymax(mag(VF("/VODIFF")))	7.864			

Avd(max)=7.864

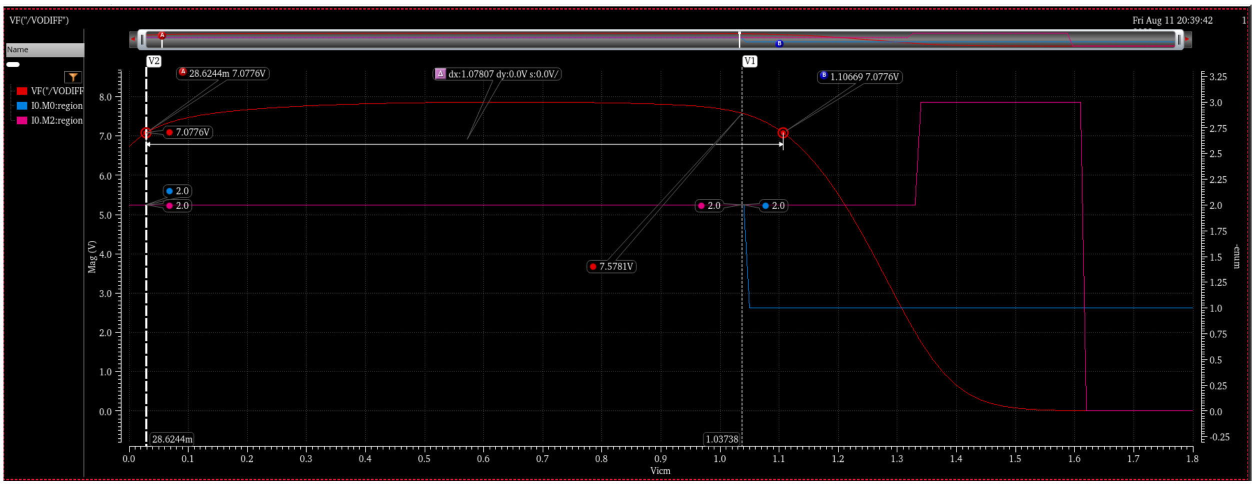
6.2 Report CM large signal CCs (Avd vs Vicm). Assume the valid range for Vicm (CMIR) is defined by the condition that Avd is within 90% of the max gain, i.e., 10% drop in gain.



90% * 7.864= 7.0776

The range is 1.078 v

6.3 PLOT THE RESULTS OVERLAID ON THE RESULTS OF THE PREVIOUS METHOD (REGION PARAMETER). FIND THE CM INPUT RANGE. COMPARE WITH THE PREVIOUS METHOD IN A TABLE



the cm input range is within the 10% drop and the transistors in saturation

Vicm=1.037-28.62m =1.008 V

Above 90% gain	Region only	Both
1.078v	1.037v	1.008v