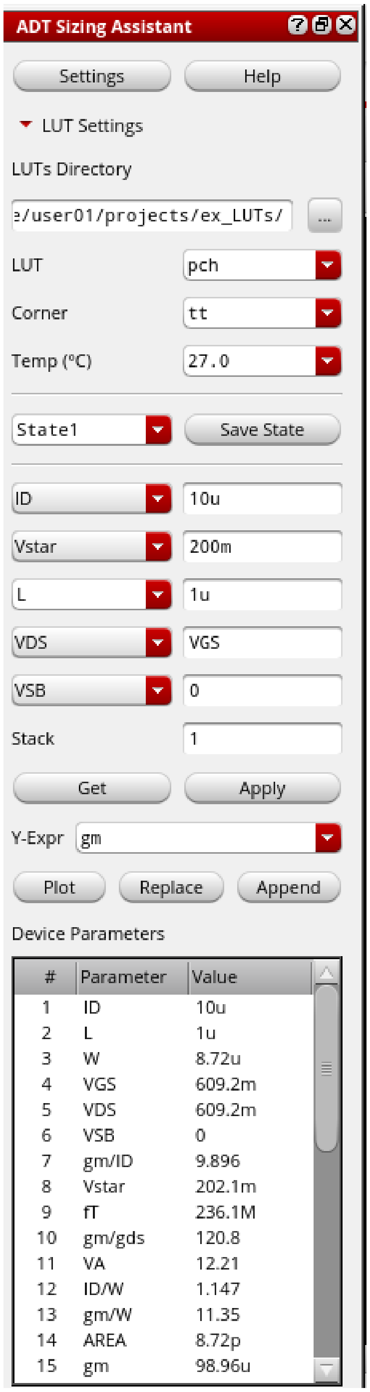
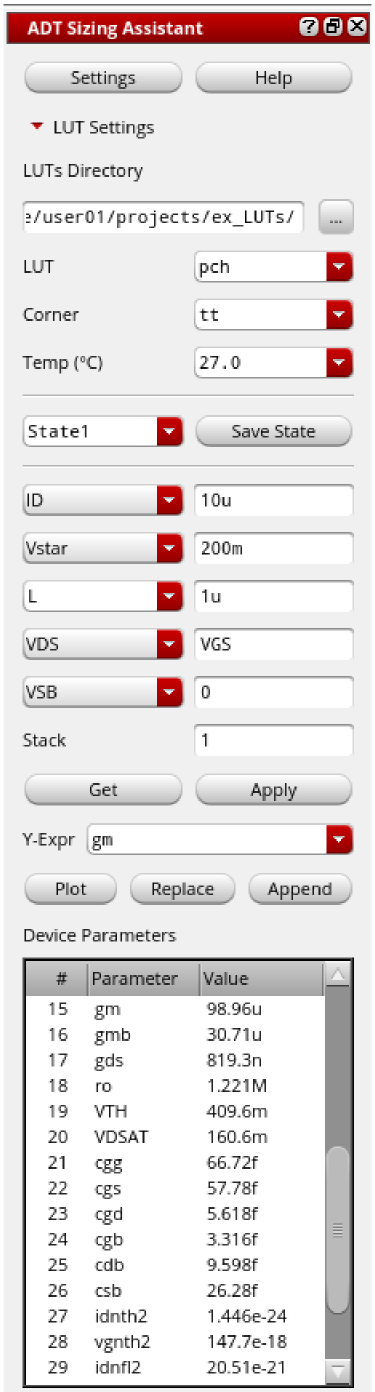
PART 1: Sizing Chart

1 Device Sizing Using SA

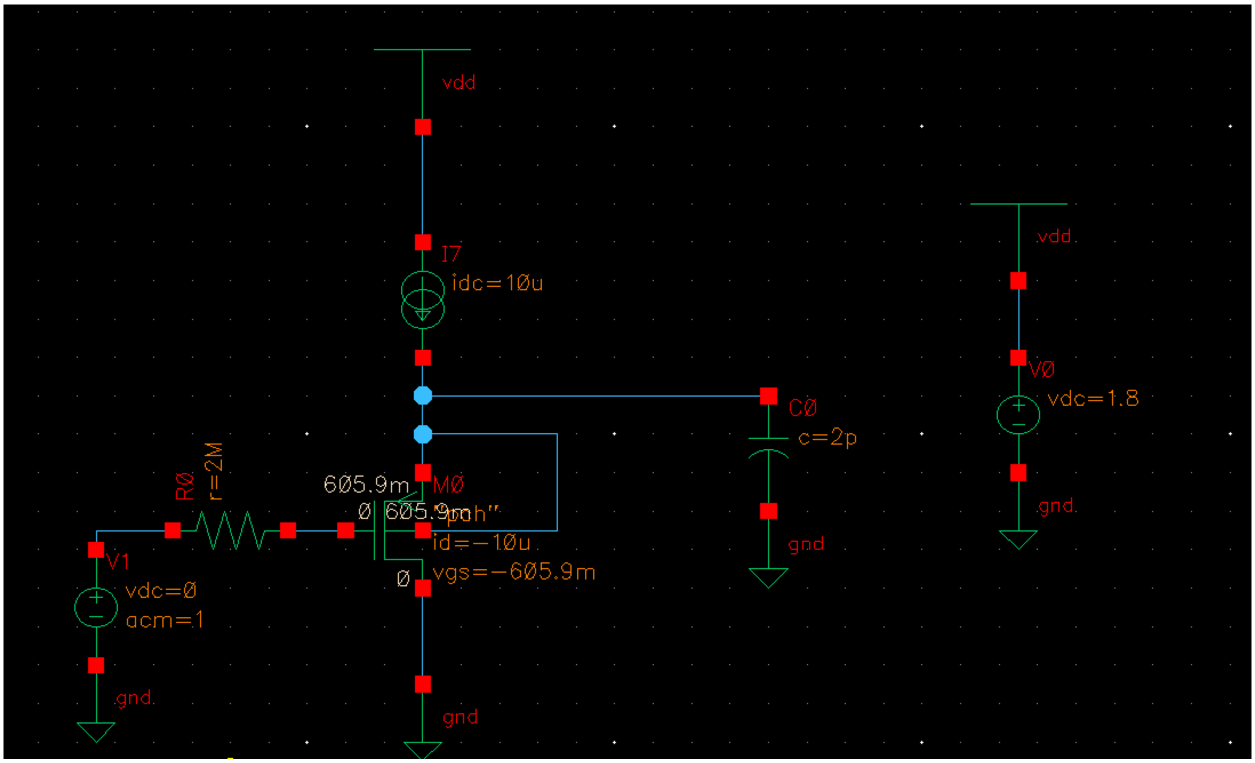



ADT Sizing Assistant
Settings
Help
LUT Settings
LUTs Directory
e/user01/projects/ex_LUTs/
...
LUT
pch
Corner
tt
Temp (°C)
27.0
State1
Save State
ID
10u
Vstar
200m
L
1u
VDS
VGS
VSB
0
Stack
1
Get
Apply
Y-Expr
gm
Plot
Replace
Append
Device Parameters
Parameter Value
15 gm 98.96u
16 gmb 30.71u
17 gds 819.3n
18 ro 1.221M
19 VTH 409.6m
20 VDSAT 160.6m
21 cgg 66.72f
22 cgs 57.78f
23 cgd 5.618f
24 cgb 3.316f
25 cdb 9.598f
26 csb 26.28f
27 idnth2 1.446e-24
28 vgnth2 147.7e-18
29 idnfl2 20.51e-21

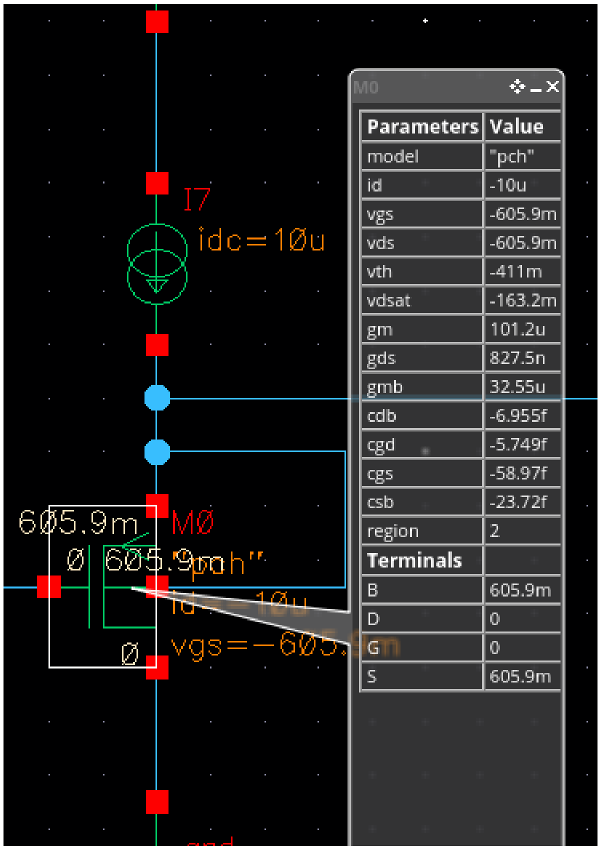
Part 2: CD Amplifier

OP Analysis

1 Create a new schematic for the CD amplifier



2 SIMULATE THE OP POINT. REPORT A SNAPSHOT CLEARLY SHOWING THE FOLLOWING PARAMETERS



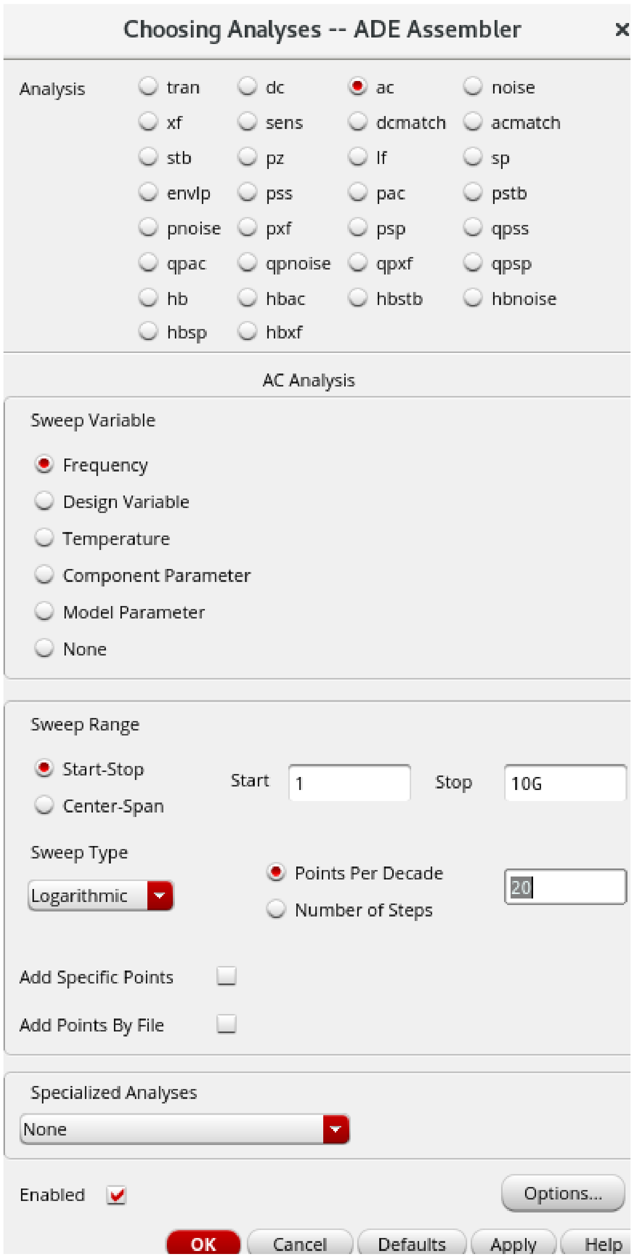
3 CHECK THAT THE TRANSISTOR OPERATES IN SATURATION.

Cadence Hint: The “region” meaning is as follows: (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown).

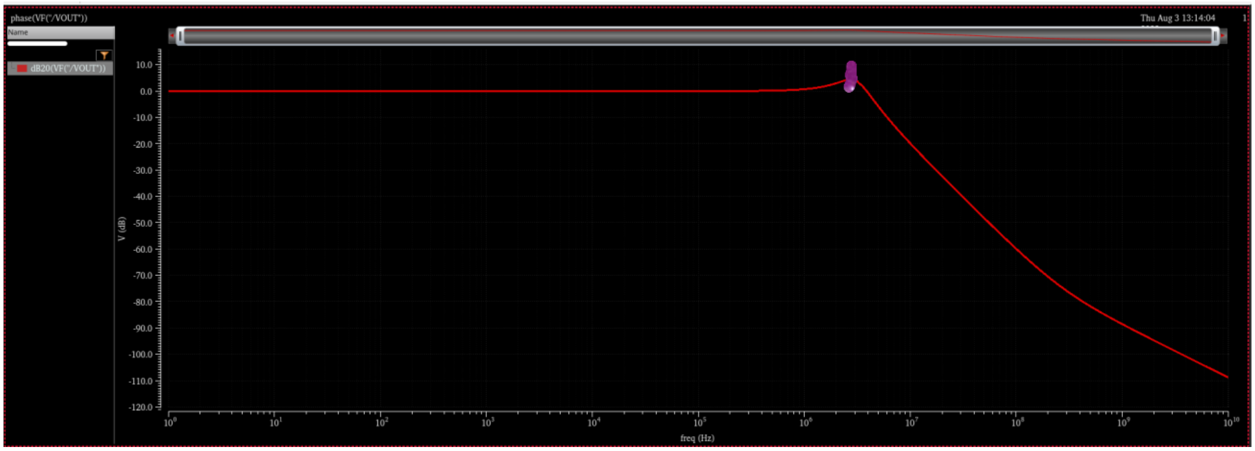
Region is 2, and vgs = vds so it is diode connected transistor.

AC Analysis

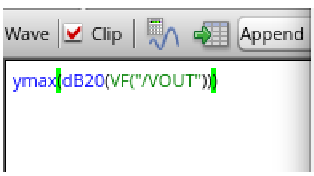
1 Perform AC analysis (1Hz:10GHz, logarithmic, 20points/decade) to investigate the frequency domain peaking.

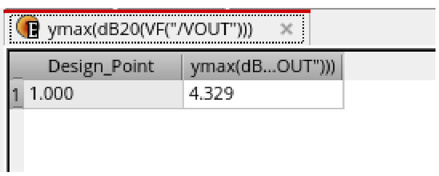


2 REPORT THE BODE PLOT MAGNITUDE



3 DO YOU NOTICE FREQUENCY DOMAIN PEAKING? HOW MUCH IS THE PEAKING?

YES, 



	Design_Point	ymax(dB...OUT"))
1	1.000	4.329

= 4.329 DB above the dc gain

4 ANALYTICALLY CALCULATE THE QUALITY FACTOR (USE APPROXIMATE EXPRESSIONS). IS THE SYSTEM UNDERDAMPED OR OVERDAMPED?

CL=2P, Cgs=59 f, Cgd =5.75 f

Cl >> C (mos)

So we can use approximate expressions Q= $\sqrt{\frac{gm(Cgs+Cgd)Rsig}{CL}}$ = 2.56

But Rsig is so big so

$$Q = \frac{\sqrt{b2}}{b1}$$

$\sqrt{b2}$=($\sqrt{\frac{CL(Cgs+Cgd)+CgsCgd}{gm}}$)Rsig b1=CgdRsig + $\frac{Cgs+Cl}{gm}$

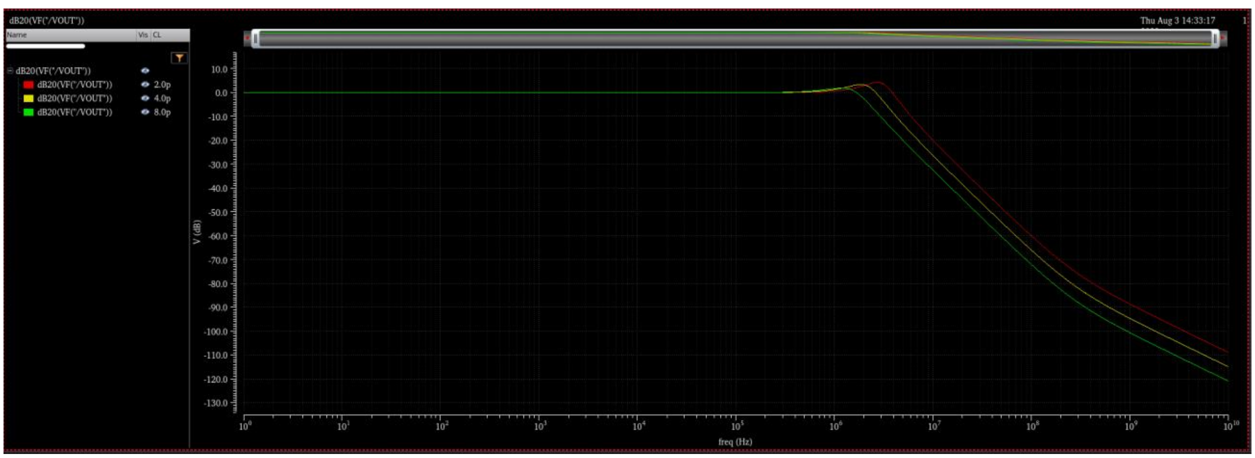
So, Q= 1.59

Q>0.5 SO IT IS underdamped system.

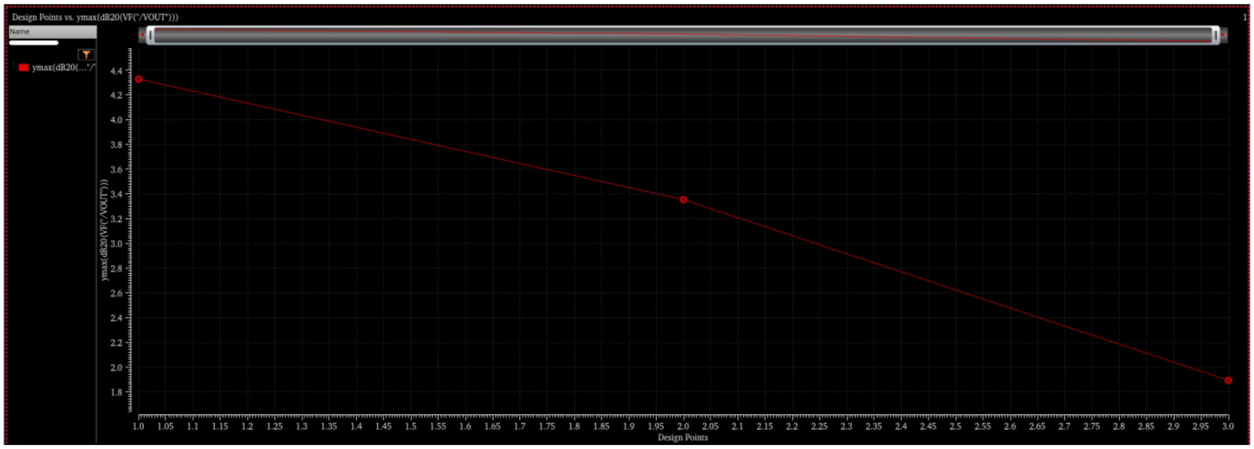
5 [OPTIONAL] PERFORM PARAMETRIC SWEEP: CL = 2P, 4P, 8P.

Parameters: CL=2p						
1	LAB4_lab_1	dB20(VF("/VOUT...				
1	LAB4_lab_1	phase(VF("/VOU...				
1	LAB4_lab_1	ymax(dB20(VF("...	4.329			
Parameters: CL=4p						
2	LAB4_lab_1	dB20(VF("/VOUT...				
2	LAB4_lab_1	phase(VF("/VOU...				
2	LAB4_lab_1	ymax(dB20(VF("...	3.354			
Parameters: CL=8p						
3	LAB4_lab_1	dB20(VF("/VOUT...				
3	LAB4_lab_1	phase(VF("/VOU...				
3	LAB4_lab_1	ymax(dB20(VF("...	1.892			

5.1 REPORT BODE PLOT MAGNITUDE OVERLAID ON SAME PLOT.



5.2 REPORT THE PEAKING VS CL.



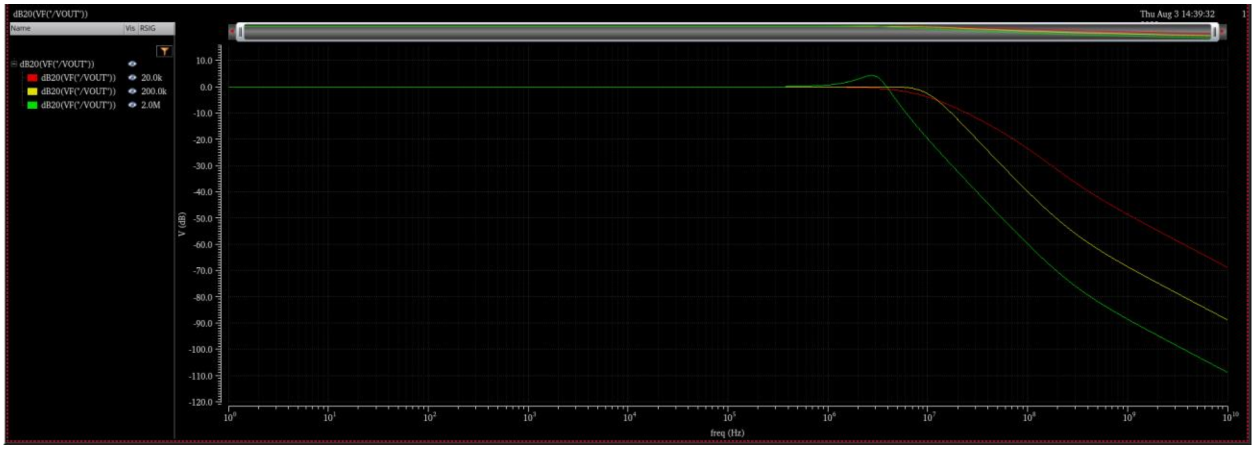
5.3 COMMENT

As we increasing Cl, Q decreases so the peaking decreases as ωout becomes more dominant and also ωo decreases (the frequency at which peaking happens is decreased).

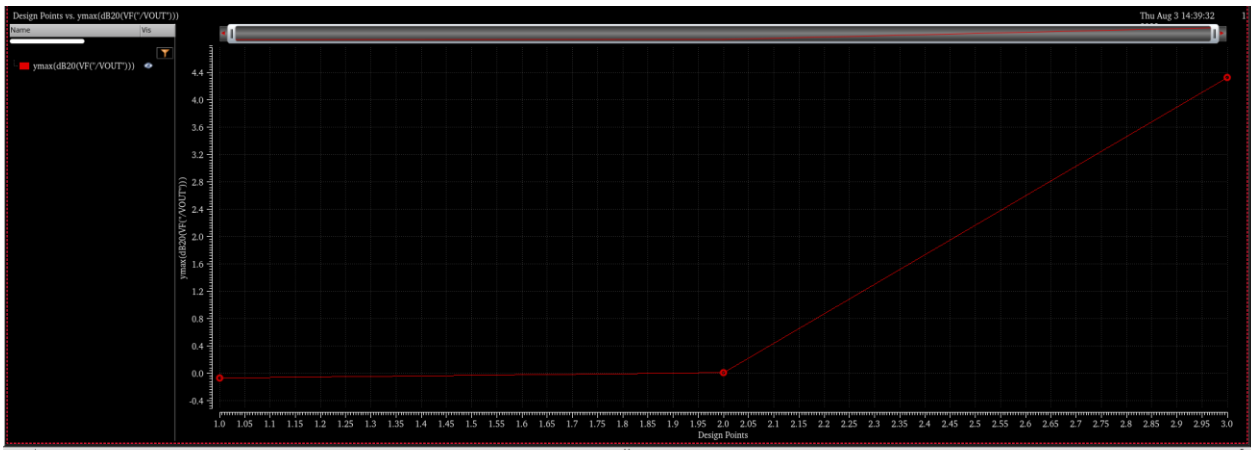
6 [OPTIONAL] PERFORM PARAMETRIC SWEEP: RSIG = 20K, 200K, 2M.

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: RSIG=20K						
1	LAB4_lab_1	dB20(VF("/VOUT...				
1	LAB4_lab_1	phase(VF("/VOU...				
1	LAB4_lab_1	ymax(dB20(VF("...	-70.73m			
Parameters: RSIG=200K						
2	LAB4_lab_1	dB20(VF("/VOUT...				
2	LAB4_lab_1	phase(VF("/VOU...				
2	LAB4_lab_1	ymax(dB20(VF("...	7.88m			
Parameters: RSIG=2M						
3	LAB4_lab_1	dB20(VF("/VOUT...				
3	LAB4_lab_1	phase(VF("/VOU...				
3	LAB4_lab_1	ymax(dB20(VF("...	4.329			

6.1 REPORT BODE PLOT MAGNITUDE OVERLAID ON SAME PLOT



6.2 REPORT THE PEAKING VS RSIG

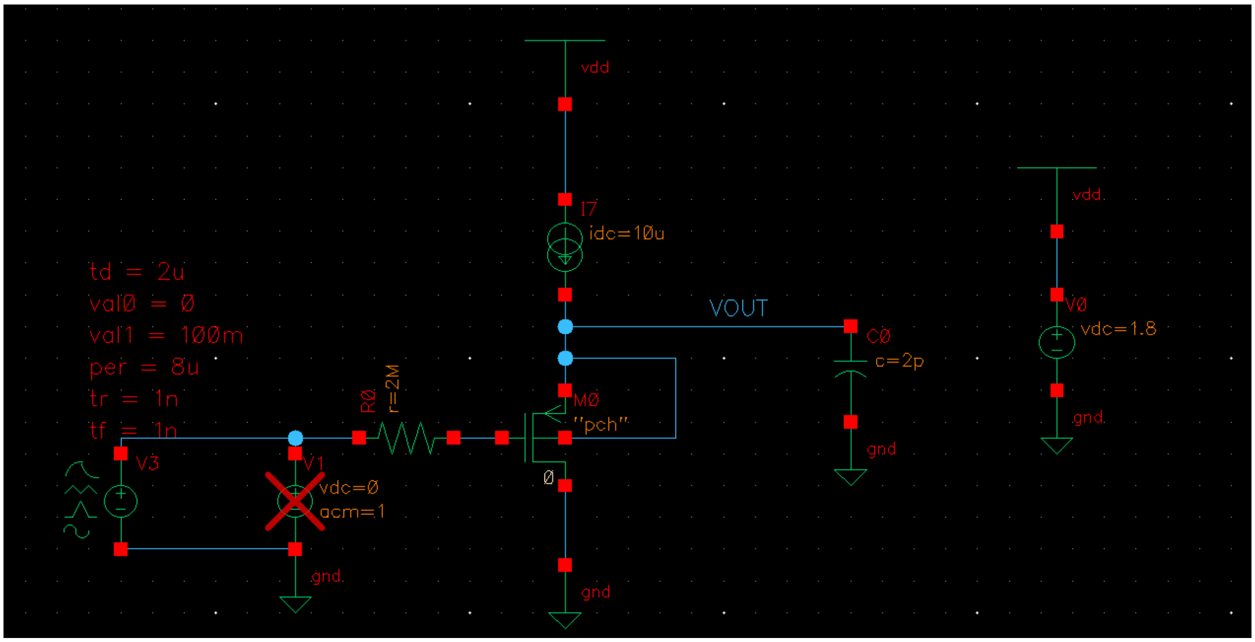


6.3 COMMENT

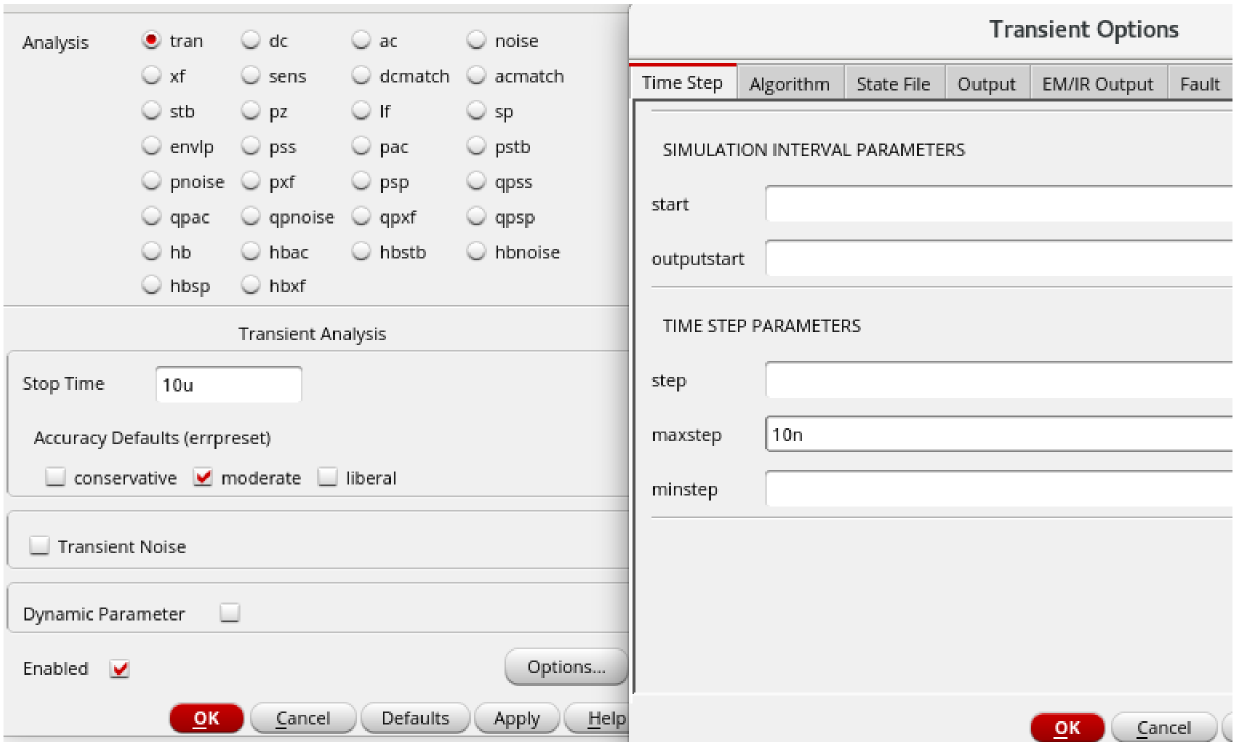
As increasing Rsig, Q increased so the peaking increased but the natural frequency decreased, so if we decreased Rsig we will see less peaking and higher ωo (flatter response) .

Transient Analysis

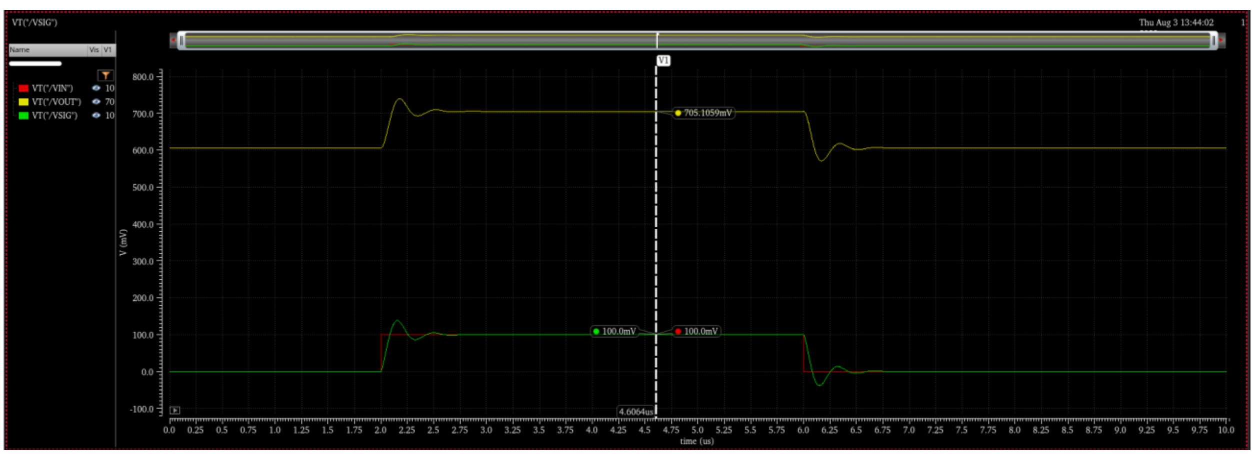
1 USE A PULSE SOURCE AS YOUR TRANSIENT STIMULUS AND SET IT AS FOLLOWS: DELAY TIME = 2US, INITIAL (ZERO VALUE) = 0V, PERIOD = 8US, PULSE (ONE VALUE) = 100MV, FALL TIME = 1NS, RISE TIME = 1NS, PULSE WIDTH = 4US.



2 RUN TRANSIENT ANALYSIS FOR 10US TO INVESTIGATE THE TIME DOMAIN RINGING



3 REPORT VIN AND VOUT OVERLAID VS TIME.



4 Calculate the DC voltage difference (DC shift) between Vin and Vout.

4.1 What is the relation between the DC shift and VGS of the transistor?

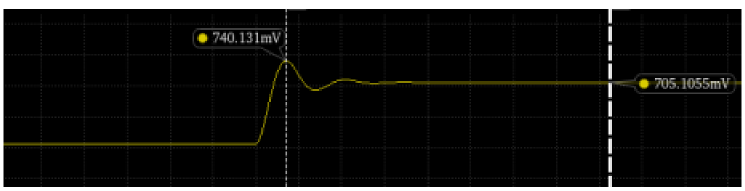
the DC shift = VGS of the transistor=605mv

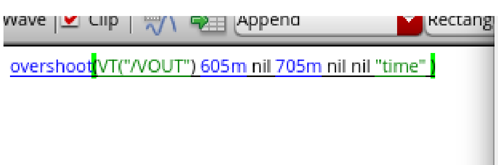
4.2 How to shift the signal down instead of shifting it up?

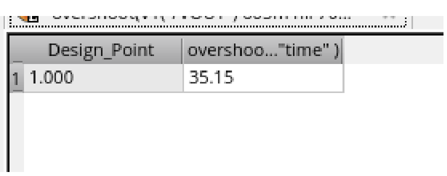
By using NMOS.

5 Do you notice time domain ringing? How much is the overshoot?

YES, $overshoot = e^{\frac{-\pi}{\sqrt{4*(Q)^2-1}}}$= 35.3 (if we didn't use the approximated Q)



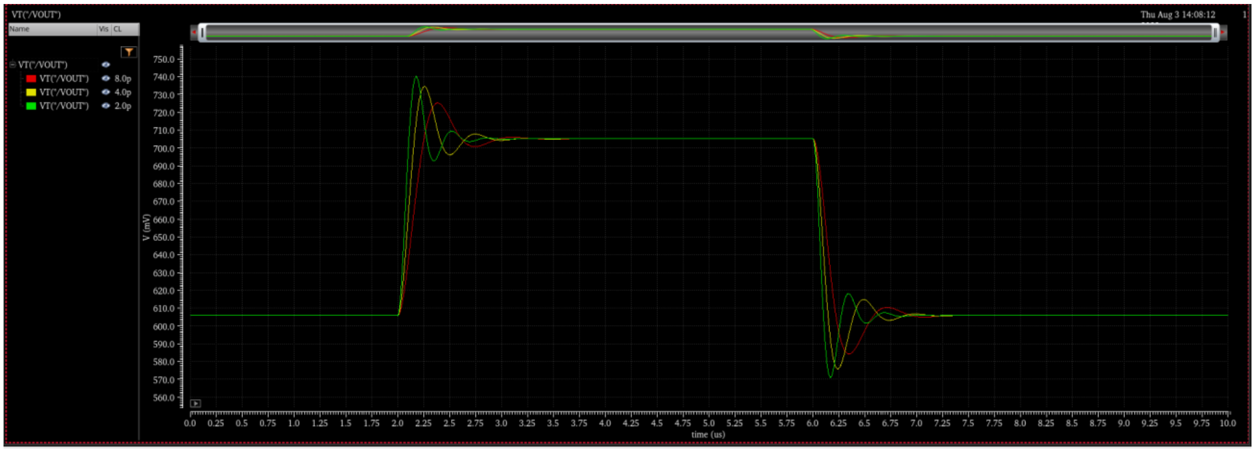




	Design_Point	overshoo..."time")
1	1.000	35.15

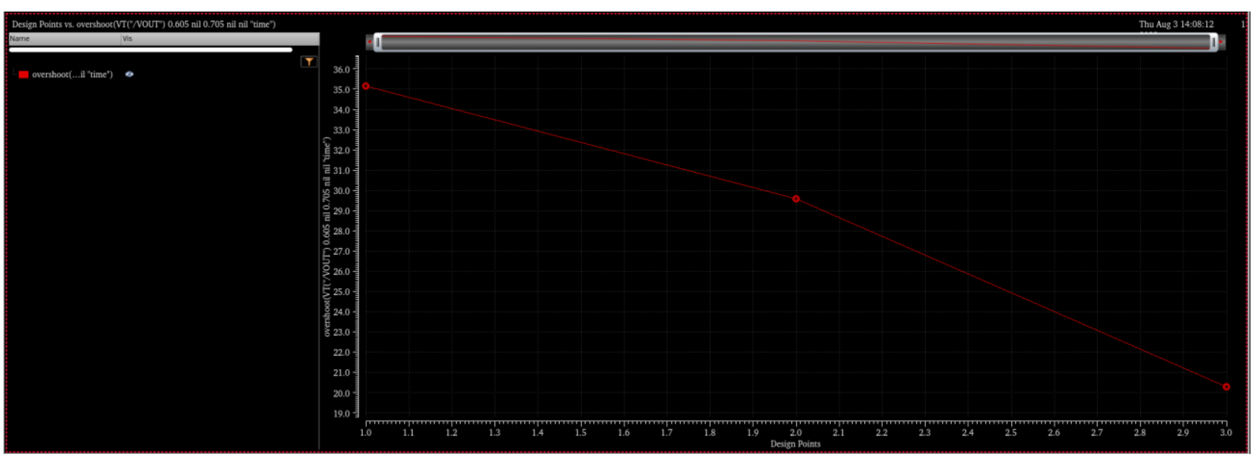
6 [Optional] Perform parametric sweep: CL = 2p, 4p, 8p.

6.1 Report Vout vs time overlaid on same plot.



6.2 Report the overshoot vs CL.

Parameters: CL=2p						
1	LAB4_lab_1	VT("/VOUT")				
1	LAB4_lab_1	VT("/VIN")				
1	LAB4_lab_1	VT("/VSIG")				
1	LAB4_lab_1	overshoot(VT("/...	35.15			
Parameters: CL=4p						
2	LAB4_lab_1	VT("/VOUT")				
2	LAB4_lab_1	VT("/VIN")				
2	LAB4_lab_1	VT("/VSIG")				
2	LAB4_lab_1	overshoot(VT("/...	29.58			
Parameters: CL=8p						
3	LAB4_lab_1	VT("/VOUT")				
3	LAB4_lab_1	VT("/VIN")				
3	LAB4_lab_1	VT("/VSIG")				
3	LAB4_lab_1	overshoot(VT("/...	20.29			

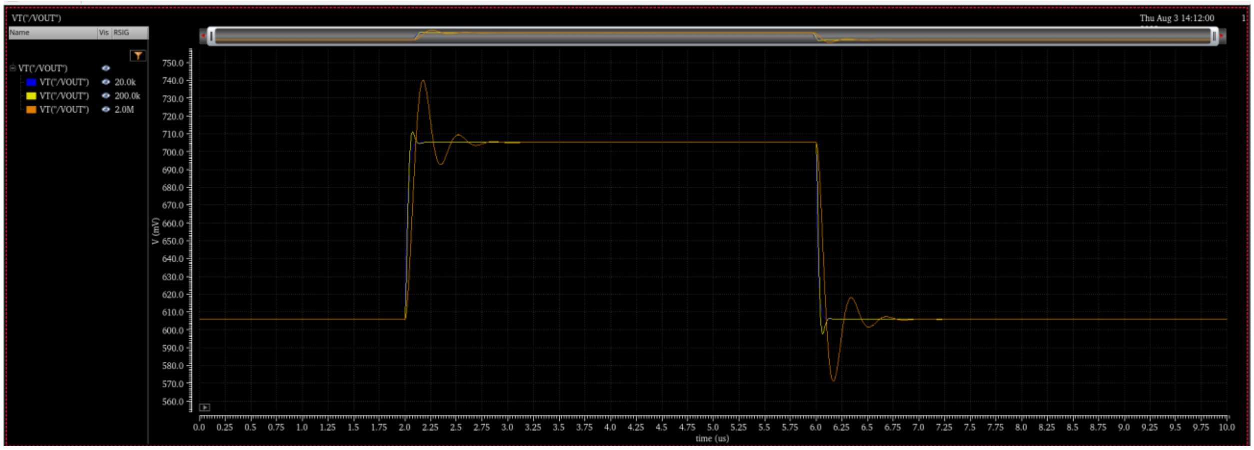


6.3 COMMENT

AS CL increases, the overshot decreases

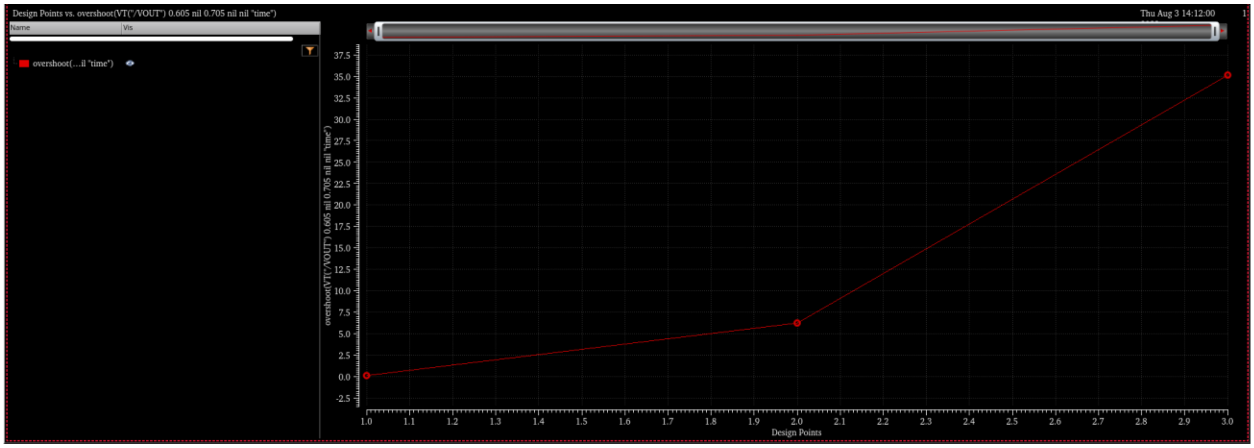
7 [OPTIONAL] PERFORM PARAMETRIC SWEEP: RSIG = 20K, 200K, 2M

7.1 REPORT VOUT VS TIME OVERLAID ON SAME PLOT.



7.2 REPORT THE OVERSHOOT VS RSIG

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: RSIG=20K						
1	LAB4_lab_1	VT("/VOUT")				
1	LAB4_lab_1	VT("/VIN")				
1	LAB4_lab_1	VT("/VSIG")				
1	LAB4_lab_1	overshoot(VT("/...	106.2m			
Parameters: RSIG=200K						
2	LAB4_lab_1	VT("/VOUT")				
2	LAB4_lab_1	VT("/VIN")				
2	LAB4_lab_1	VT("/VSIG")				
2	LAB4_lab_1	overshoot(VT("/...	6.235			
Parameters: RSIG=2M						
3	LAB4_lab_1	VT("/VOUT")				
3	LAB4_lab_1	VT("/VIN")				
3	LAB4_lab_1	VT("/VSIG")				
3	LAB4_lab_1	overshoot(VT("/...	35.15			

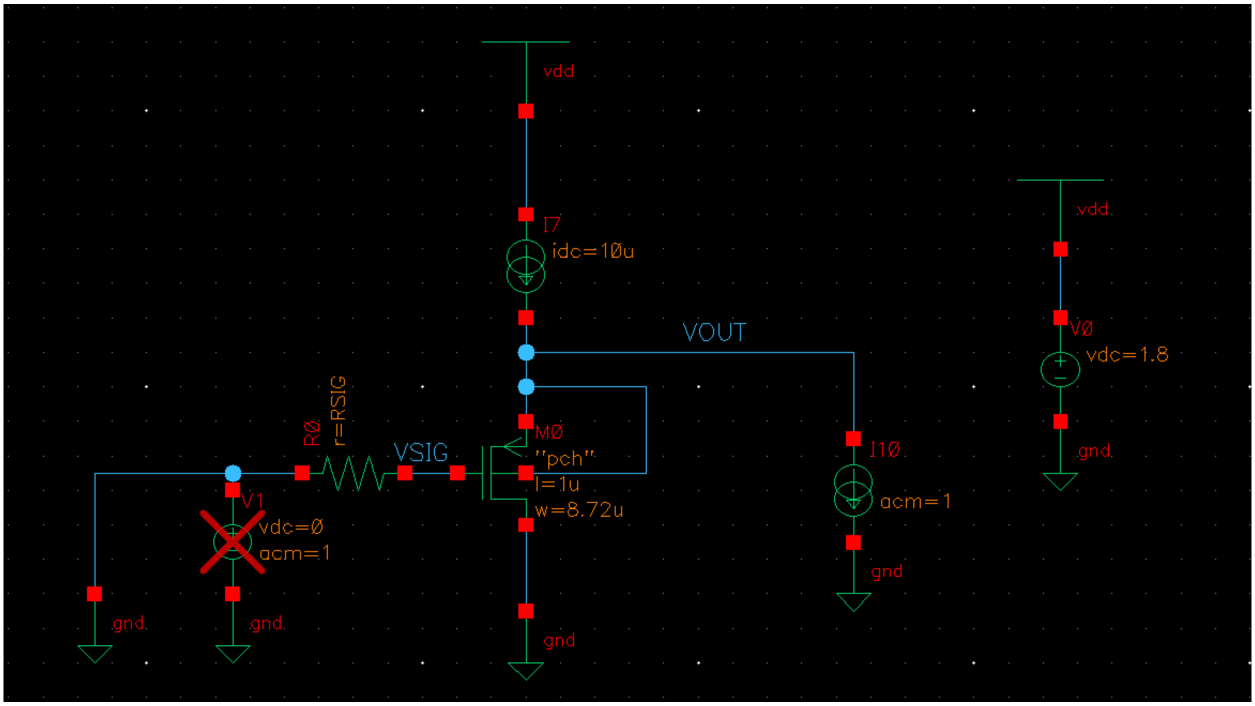


7.3 COMMENT

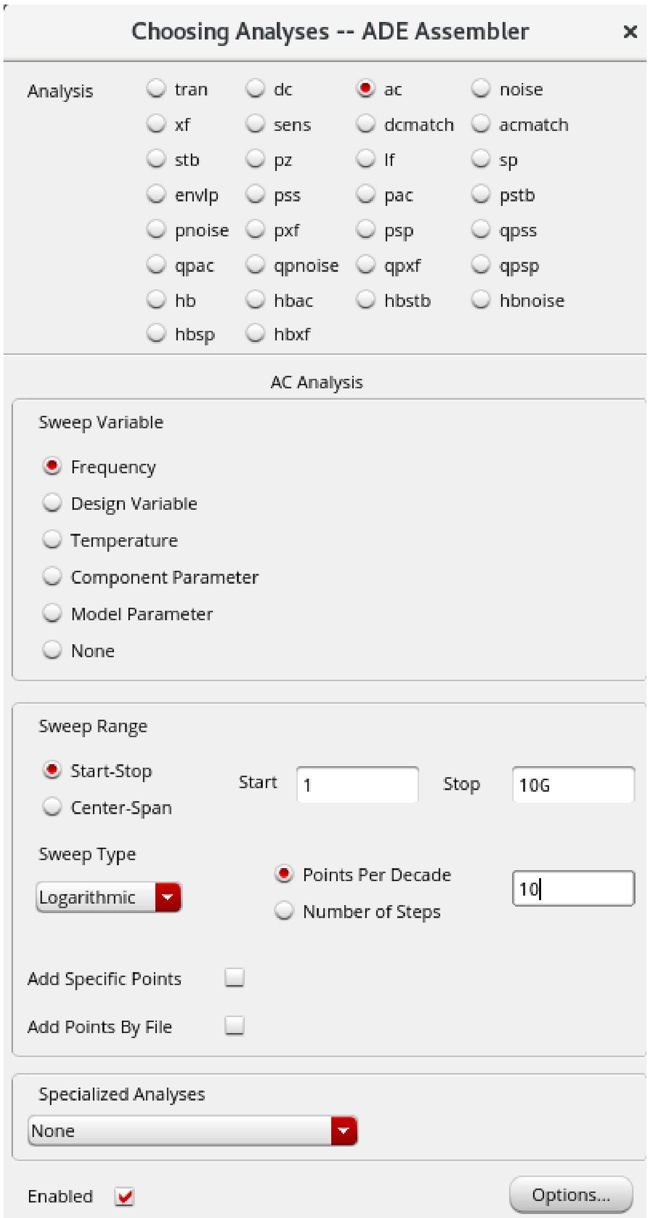
AS Rsig increases, the overshot increases and at low impedance we can see there is almost no overshoot.

$Zout$ (Inductive Rise)

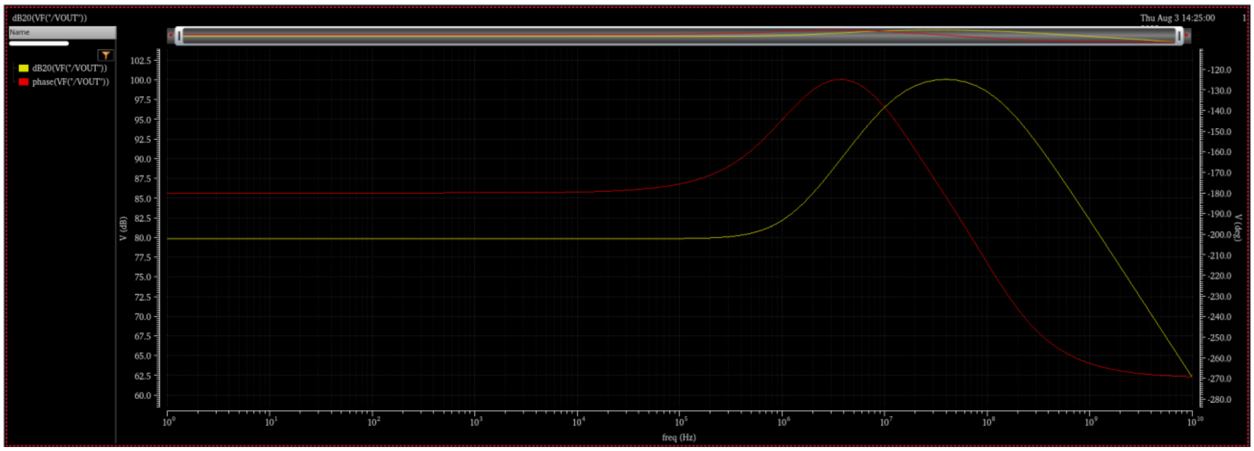
1 WE WANT TO SIMULATE THE CD AMPLIFIER OUTPUT IMPEDANCE. REPLACE CL WITH AN AC CURRENT SOURCE WITH MAGNITUDE = 1. REMOVE THE AC INPUT SIGNAL.



2 Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade). The voltage across the AC current source is itself the output impedance.



3 PLOT THE OUTPUT IMPEDANCE (MAGNITUDE AND PHASE) VS FREQUENCY. DO YOU NOTICE AN INDUCTIVE RISE? WHY?



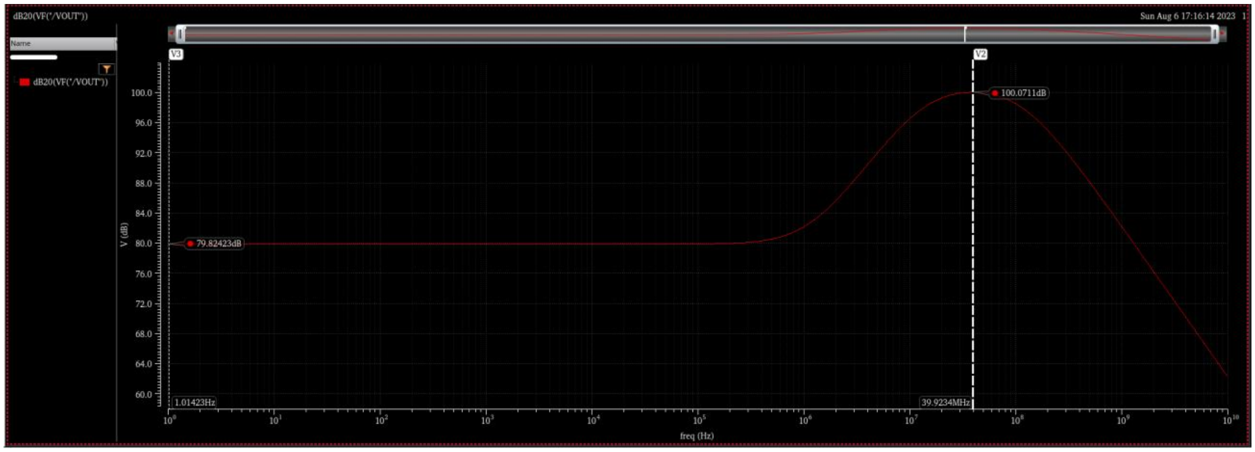
Yes, as $\omega z < \omega p$, because 1/gm < Rsig, so the zero causes a 20dB/dec rise like inductor (with increasing frequency the impedance increases).

4 DOES $Zout$ FALL AT HIGH FREQUENCY? WHY?

Yes, AS at high frequency a pole with Cgs appears after the pole with cgd and because of these two poles after the zero we have a fall with -20 db/dec at high frequency.

5 ANALYTICALLY CALCULATE THE ZEROS, POLES, AND MAGNITUDE AT LOW/HIGH FREQUENCY FOR $Zout$. COMPARE WITH SIMULATION RESULTS IN A TABLE.

```
                Poles (Hz)

        Real                  Imaginary            Qfactor

  1   -1.34828e+07           0.00000e+00          5.00000e-01
  2   -1.15850e+08           0.00000e+00          5.00000e-01

                Zeros (Hz)
                at V(VOUT,0)/I12

        Real                  Imaginary            Qfactor

  1   -1.17422e+06           0.00000e+00          5.00000e-01
```


dB20(VF("/VOUT"))
Sun Aug 6 17:16:14 2023 1
Name
dB20(VF("/VOUT"))
V3
V2
100.0711dB
79.82423dB
1.01423Hz
39.9234MHz
V (dB)
freq (Hz)

Subject موضوع الدرس Date التاريخ

$$S_Z = \frac{-1}{R_{sig}\, C_{gs}} = -8,47\ M\,rad/s$$

$$\Rightarrow \boxed{f_Z = 1,34\ MHz}$$

$$S_{P1} = -\frac{(g_m + g_{ds})}{R_{sig}\, g_{ds}\, C_{gs} + C_{gs}} = -651,6\ M\,rad/s$$

$$\Rightarrow \boxed{f_{P1} = 103,7\ MHz}$$

$$S_{P2} = \frac{-1}{R_{sig}\ C_{gd}} = -86,97\ M\,rad/s$$

$$\Rightarrow \boxed{f_{P2} = 13,8\ MHz}$$

At low freq: $Z_{out_{LF}} = \frac{1}{g_m} \,//\, r_o$

So $Z_{out_{LF}} = 9,8\ k\Omega$

$20 \log (9,8K) = 79,8\ Db$

At High freq $Z_{out} = R_{sig} \,//\, r_o = 753,2K\Omega$

$20 \log (753,2K) = 117,54\ Db$

Elsalam

	Analytical	Sim
Zero	1.34 MHZ	1.17 MHZ
Pole1	13.8 MHZ	13.48 MHZ
Pole2	103.7 MHZ	115.85 MHZ
Zout LF	79.8 DB	79.8 DB
Zout Hf	117.54 DB	100.07 DB