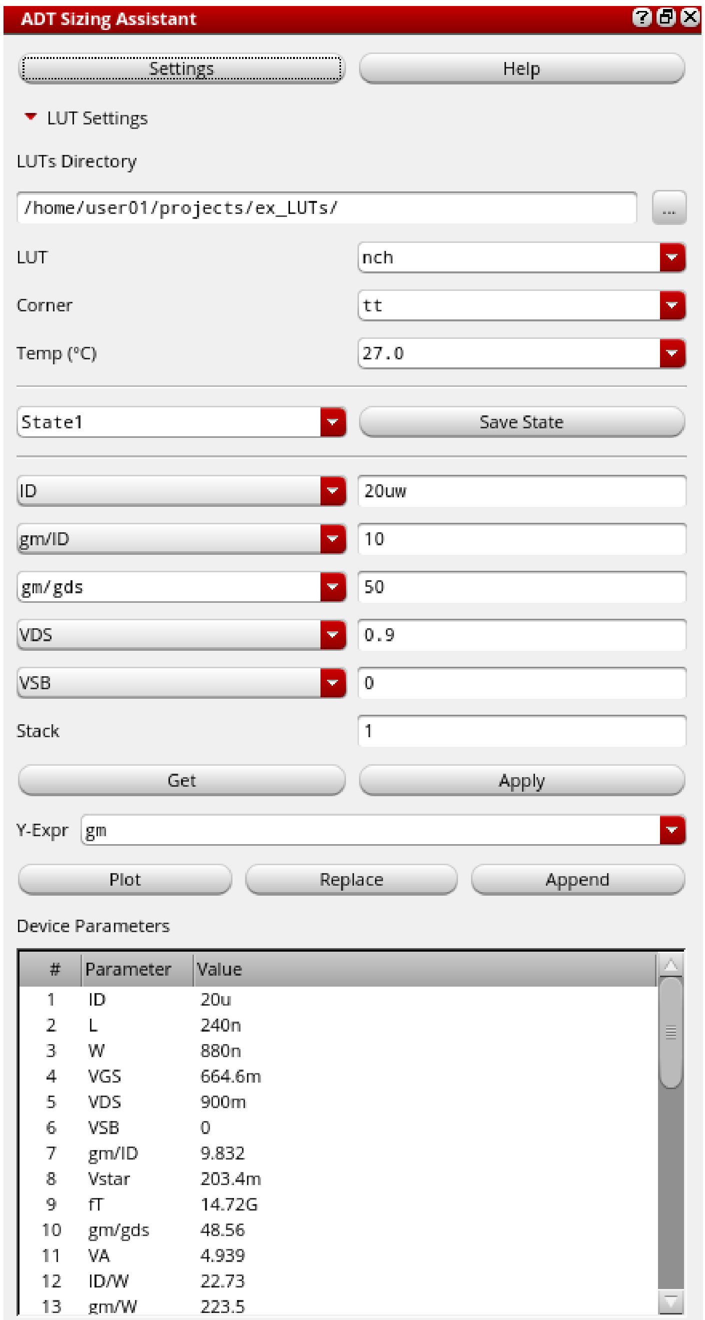
PART 1: Sizing Chart

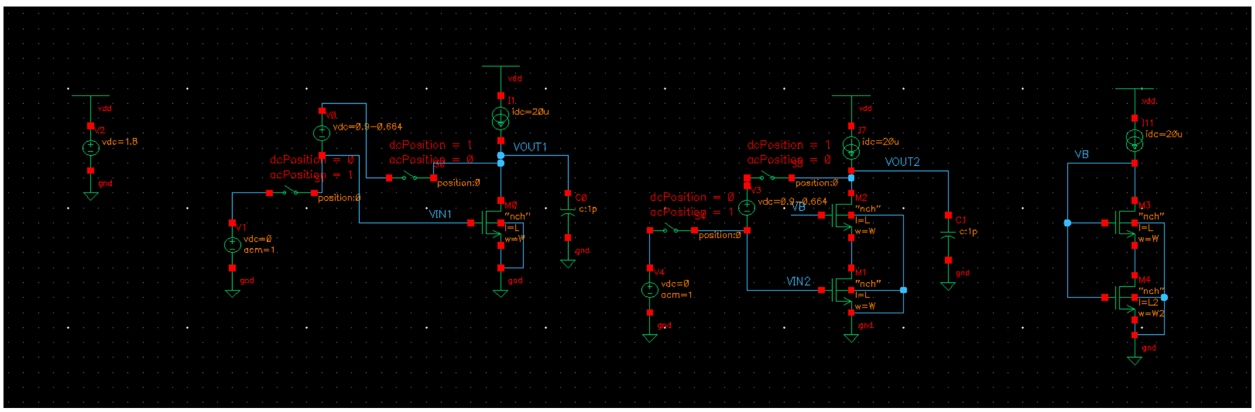
1 We want to design a common source (CS) amplifier that has ideal current source load with the following parameters.



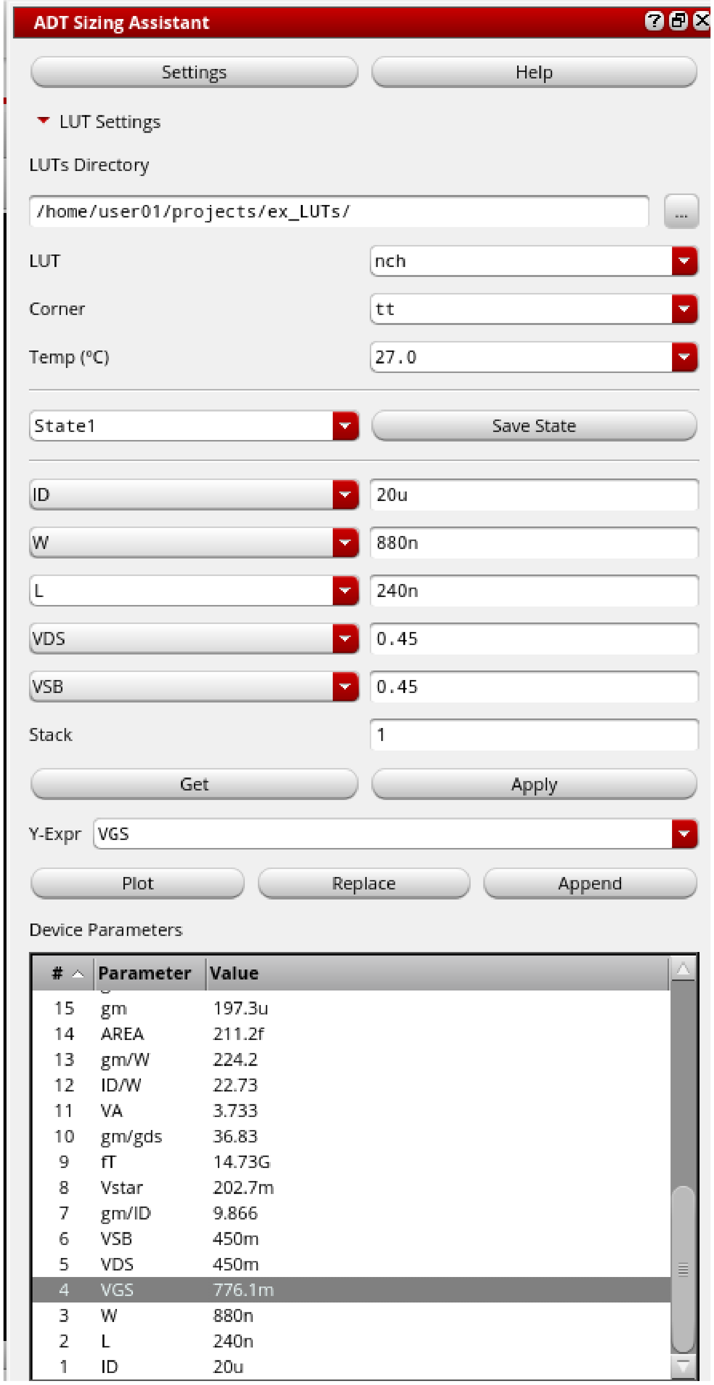
PART 2: Cascode for Gain

OP ANALYSIS

1 CREATE A NEW SCHEMATIC. CONSTRUCT THE CIRCUIT SHOWN BELOW. USE $IB = 20\mu A$. USE L AND W AS SELECTED IN PART 1 FOR M0, M1, M2, AND M4. USE THE SAME W FOR M3 BUT IT WILL HAVE DIFFERENT L AS WILL BE SHOWN LATER. USE $CL = 1pF$.

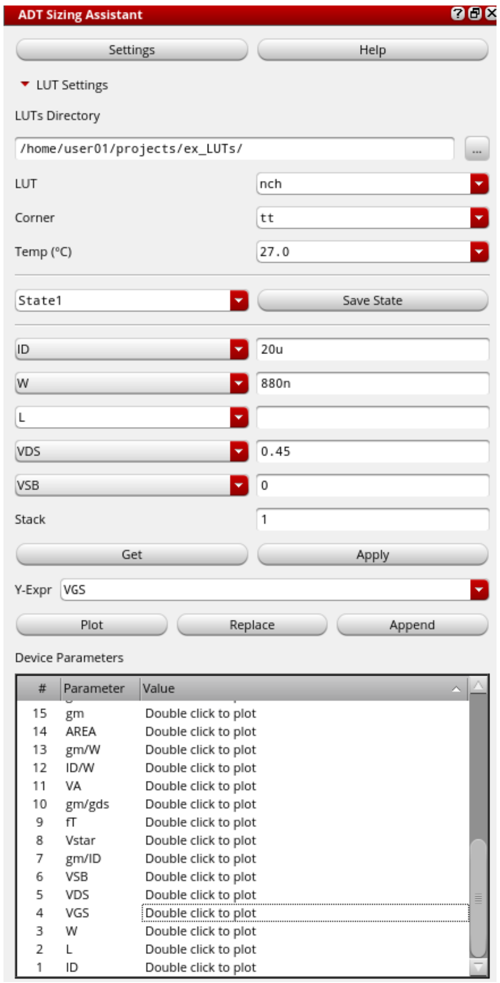


2 To calculate VB we need to find $VGS2$ because $VB = VGS2 + VDS1$. Note that M2 experiences body effect, so its VGS will be higher than M0 and M1.

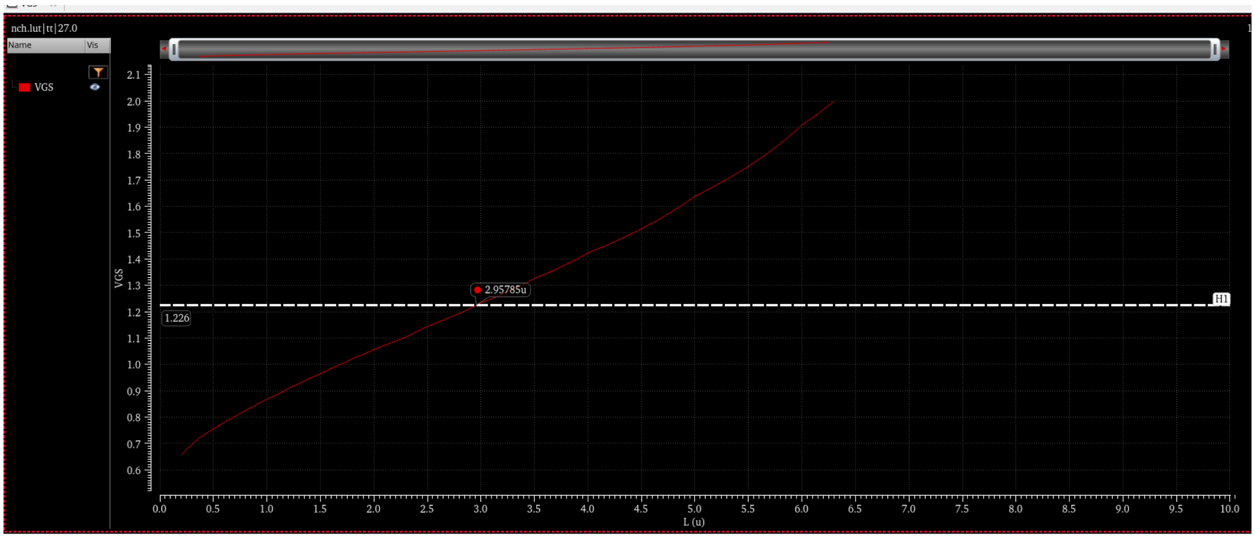


3 M3 AND M4 ARE USED TO GENERATE THE CASCODE BIAS VOLTAGE. NOTE THAT M4 IS ALWAYS IN SATURATION AND M3 IS ALWAYS IN TRIODE (WHY?). WE NEED TO FIND THE L OF M3, SO WE SET A SWEEP FOR M3 AS SHOWN BELOW

M4 (M3 in my schematic) is always in saturation as it diode connected, if we assumed that M3(M4 in my schematic) is working in saturation we will find that vds= 0v as whole VD drops on the upper saturated transistor, so the down one would be in triode.

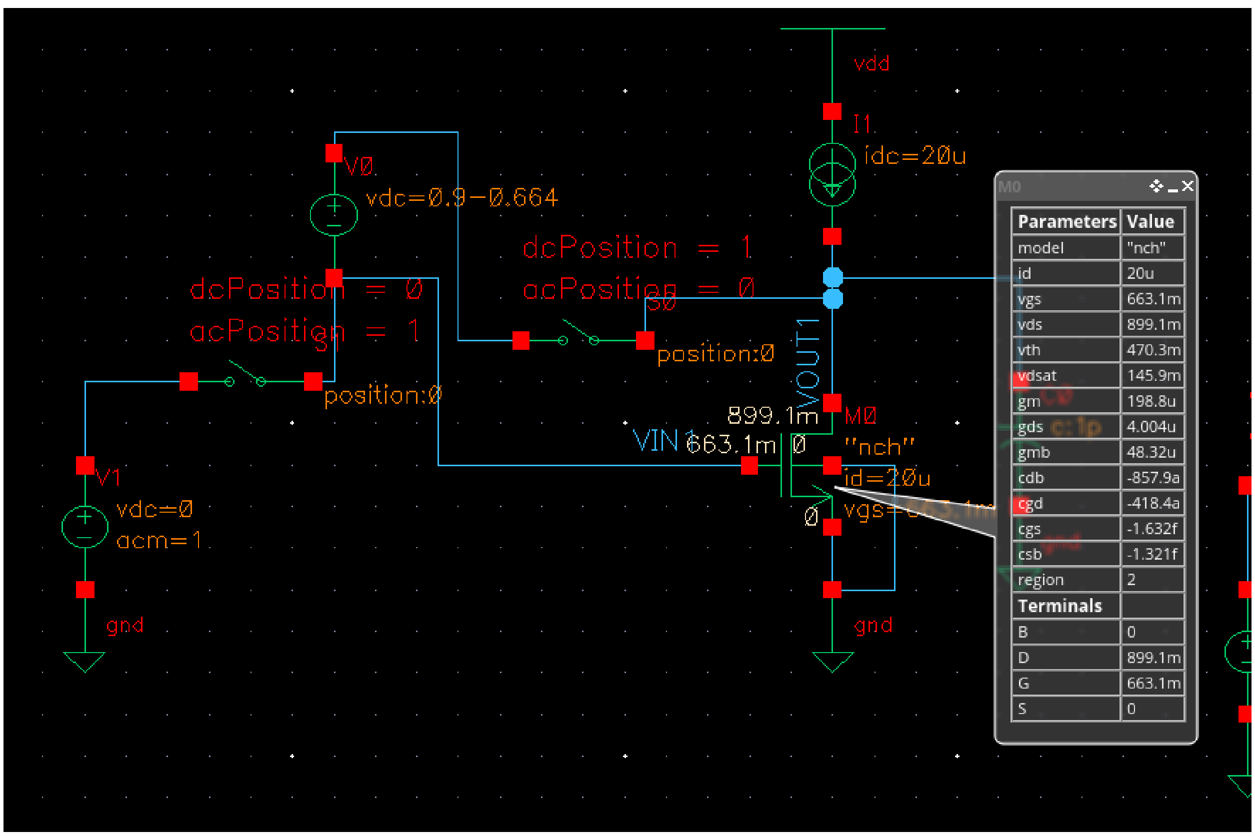


VGS+VDS=0.776+0.45=1.226

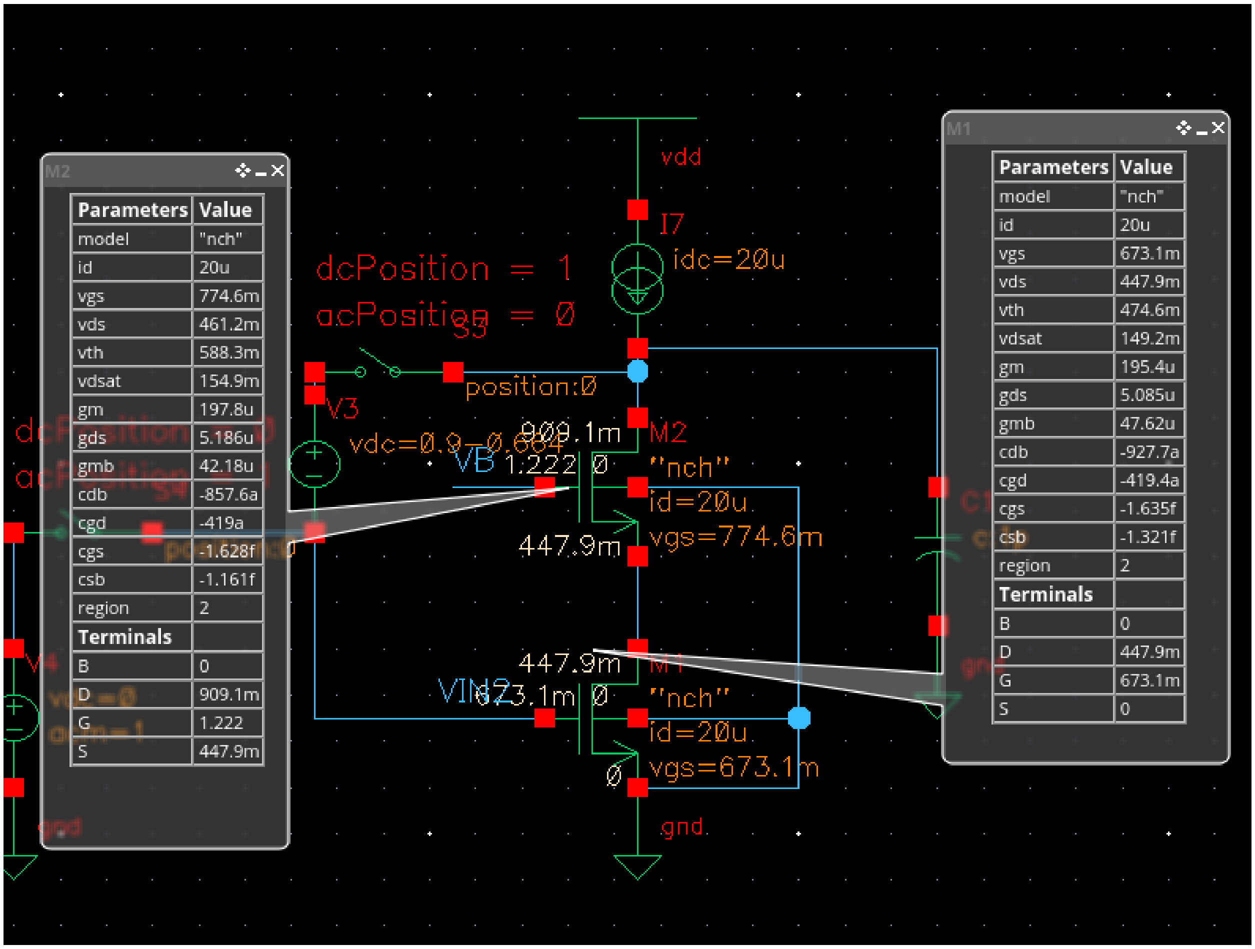


4 Simulate the DC OP point of the above CS and cascode amplifiers.

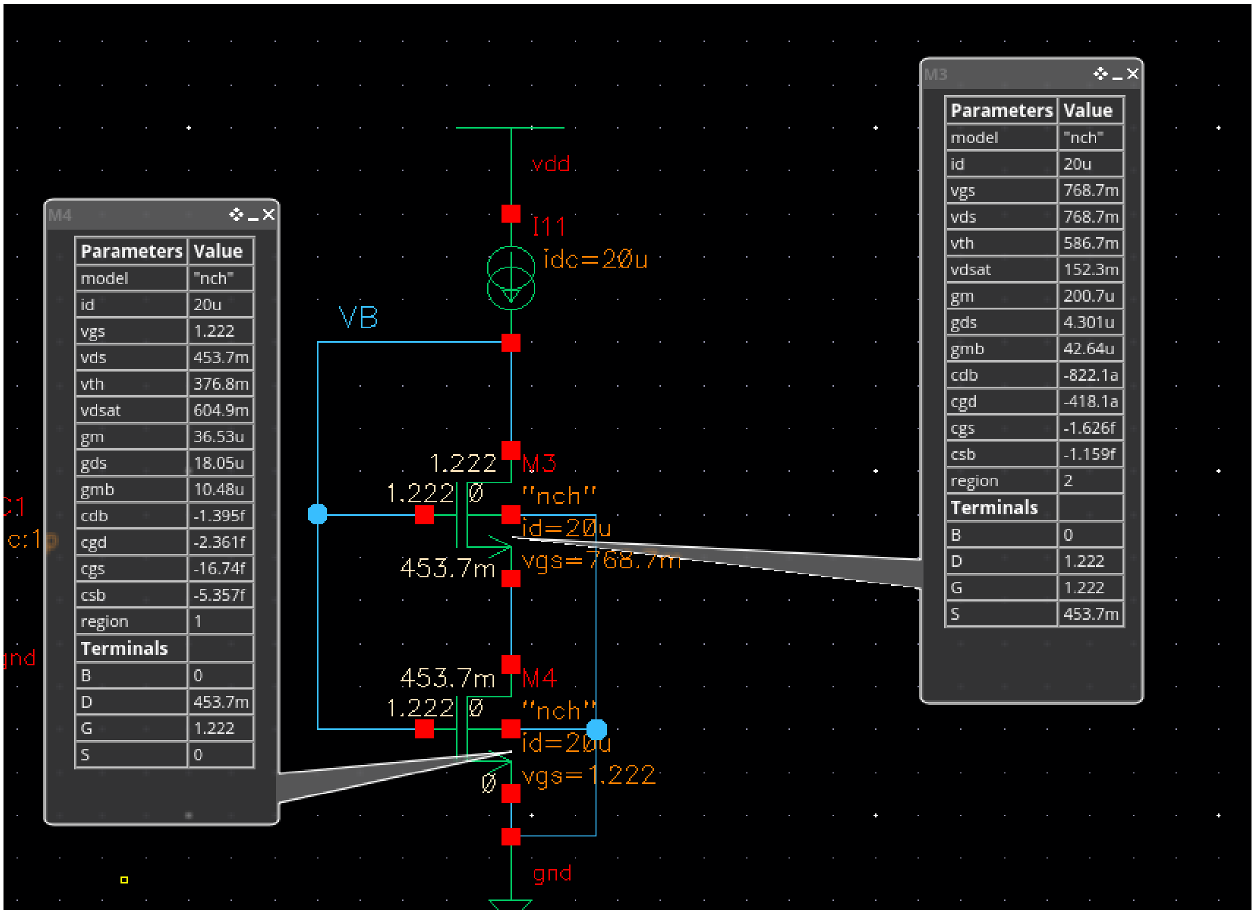
M0:



M1&M2:


M2
Parameters Value
model "nch"
id 20u
vgs 774.6m
vds 461.2m
vth 588.3m
vdsat 154.9m
gm 197.8u
gds 5.186u
gmb 42.18u
cdb -857.6a
cgd -419a
cgs -1.628f
csb -1.161f
region 2
Terminals
B 0
D 909.1m
G 1.222
S 447.9m
vdd
I7
idc=20u
dcPosition = 1
acPosition = 0
S3
position:0
V3
vdc=0.9-0.664
VB
909.1m
1.222
M2
"nch"
id=20u
447.9m
vgs=774.6m
447.9m
VIN2
673.1m
M1
"nch"
id=20u
vgs=673.1m
gnd
M1
Parameters Value
model "nch"
id 20u
vgs 673.1m
vds 447.9m
vth 474.6m
vdsat 149.2m
gm 195.4u
gds 5.085u
gmb 47.62u
cdb -927.7a
cgd -419.4a
cgs -1.635f
csb -1.321f
region 2
Terminals
B 0
D 447.9m
G 673.1m
S 0

M3&M4:



5 CHECK THAT ALL TRANSISTORS OPERATE IN SATURATION.

Cadence Hint: The "region" meaning is as follows: (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown).

All Transistors are in saturation except m4(m3 in doctor schematic) is in triode.

m0 : vds=899.1m vdsat=145.9m

m1 : vds=447.9m vdsat=149.2m

m2 : vds=461.2m vdsat=154.9m

m3 : vds=768.7m vdsat=152.3m

vds > vdsat so they are in saturation

m4 : vds=453.7m vdsat=604.9m

vds<vdsat so it is in triode

explanation : M3 is in saturation because it is diode connected, VGS(m3)=VGD(m4), and since VGS(m3) = VTH+Vov, then VGD(m4)>VTH then M4 is always in triode

6 DO ALL TRANSISTORS HAVE THE SAME VTH? WHY?

No, they don't have the same threshold voltage, because of body effect as they don't have the same V_{SB} .

7 WHAT IS THE RELATION (≪, <, =, >, ≫) BETWEEN GM AND GDS?

gm >> gds only in saturation transistors

in M4 only, just gm > gds

8 WHAT IS THE RELATION (≪, <, =, >, ≫) BETWEEN GM AND GMB?

gm > gmb

9 WHAT IS THE RELATION (≪, <, =, >, ≫) BETWEEN CGS AND CGD?

CGS > CGD

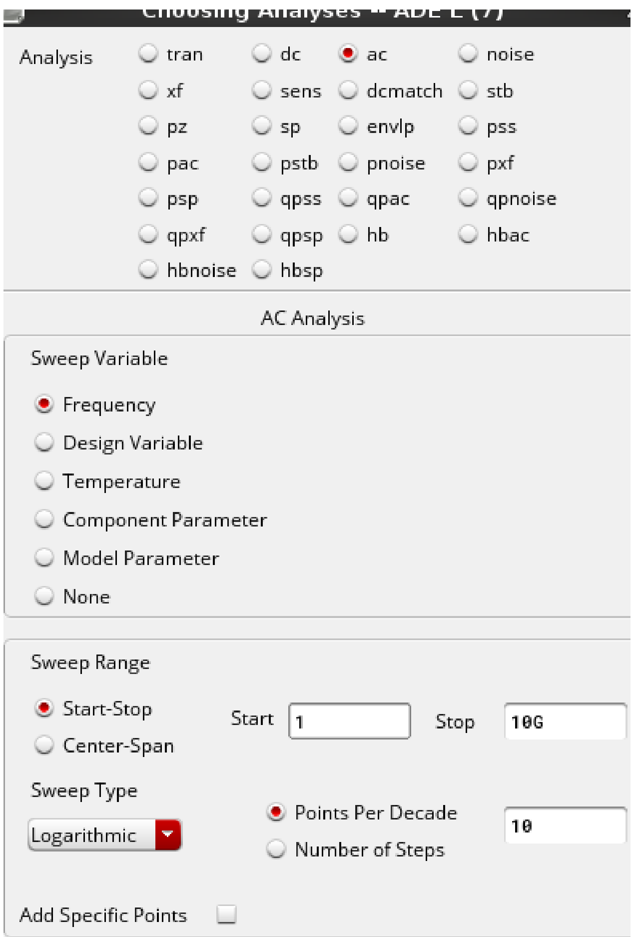
10 WHAT IS THE RELATION (≪, <, =, >, ≫) BETWEEN CSB AND CDB?

CSB > CDB

WE TOOK ABSLUITE VALUES

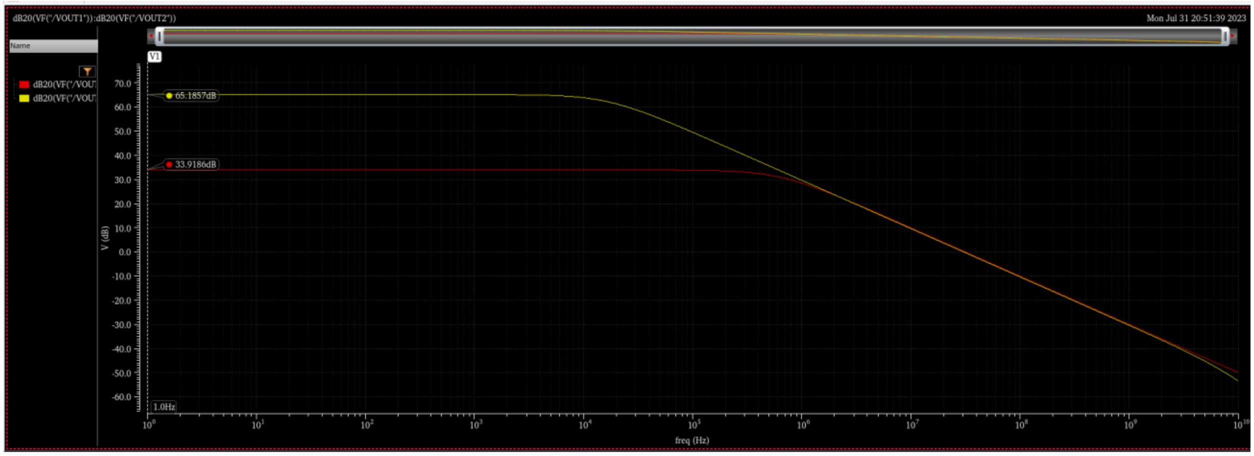
AC Analysis

1 Create a new simulation configuration. Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.



2 USE CALCULATOR TO CREATE EXPRESSIONS FOR CIRCUIT PARAMETERS (DC GAIN, BW, GBW, AND UGF) AND EXPORT THEM TO ADEXL.

Name	Type	Details	Value	Plot	Save	Spec
	expr	dB20(VF("/VOUT1"))		✓		
	expr	ymax(dB20(VF("/VOUT1")))	33.92	✓		
	expr	ymax(mag(VF("/VOUT1")))	49.65	✓		
	expr	bandwidth(VF("/VOUT1") 3 "low")	635.1K	✓		
	expr	gainBwProd(VF("/VOUT1"))	31.62M	✓		
	expr	dB20(VF("/VOUT2"))		✓		
	expr	ymax(dB20(VF("/VOUT2")))	65.19	✓		
	expr	ymax(mag(VF("/VOUT2")))	1.817K	✓		
	expr	bandwidth(VF("/VOUT2") 3 "low")	16.75K	✓		
	expr	gainBwProd(VF("/VOUT2"))	30.5M	✓		
	expr	unityGainFreq(VF("/VOUT1"))	31.6M	✓		
	expr	unityGainFreq(VF("/VOUT2"))	30.63M	✓		



3 PERFORM HAND ANALYSIS TO CALCULATE DC GAIN, BW, AND GBW

CS :

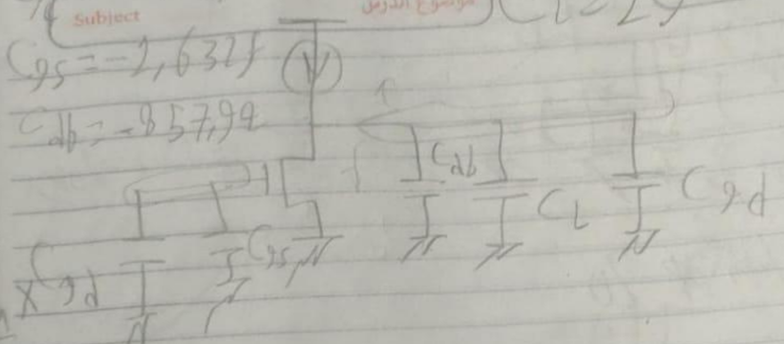
Subject موضوع الدرس Date التاريخ

$C_{gd} = 429,4\,a$

$C_{gs} = 2,632\,f$

$C_{db} = 857,9\,a$

$C_L = 1p$



$$|DC\ gain| = G_m R_{out} = g_m r_o = \frac{g_m}{g_{ds}}$$

$$= \frac{198,8}{4} = 49,7$$

$\omega_{p_{out}} < \omega_{p_{in}}$ $\quad$ C_L is so large

$$\omega_{in} = \frac{1}{\frac{1}{g_{ds}}\left[C_{gd} + C_L + C_{db}\right]} = 4\,M$$

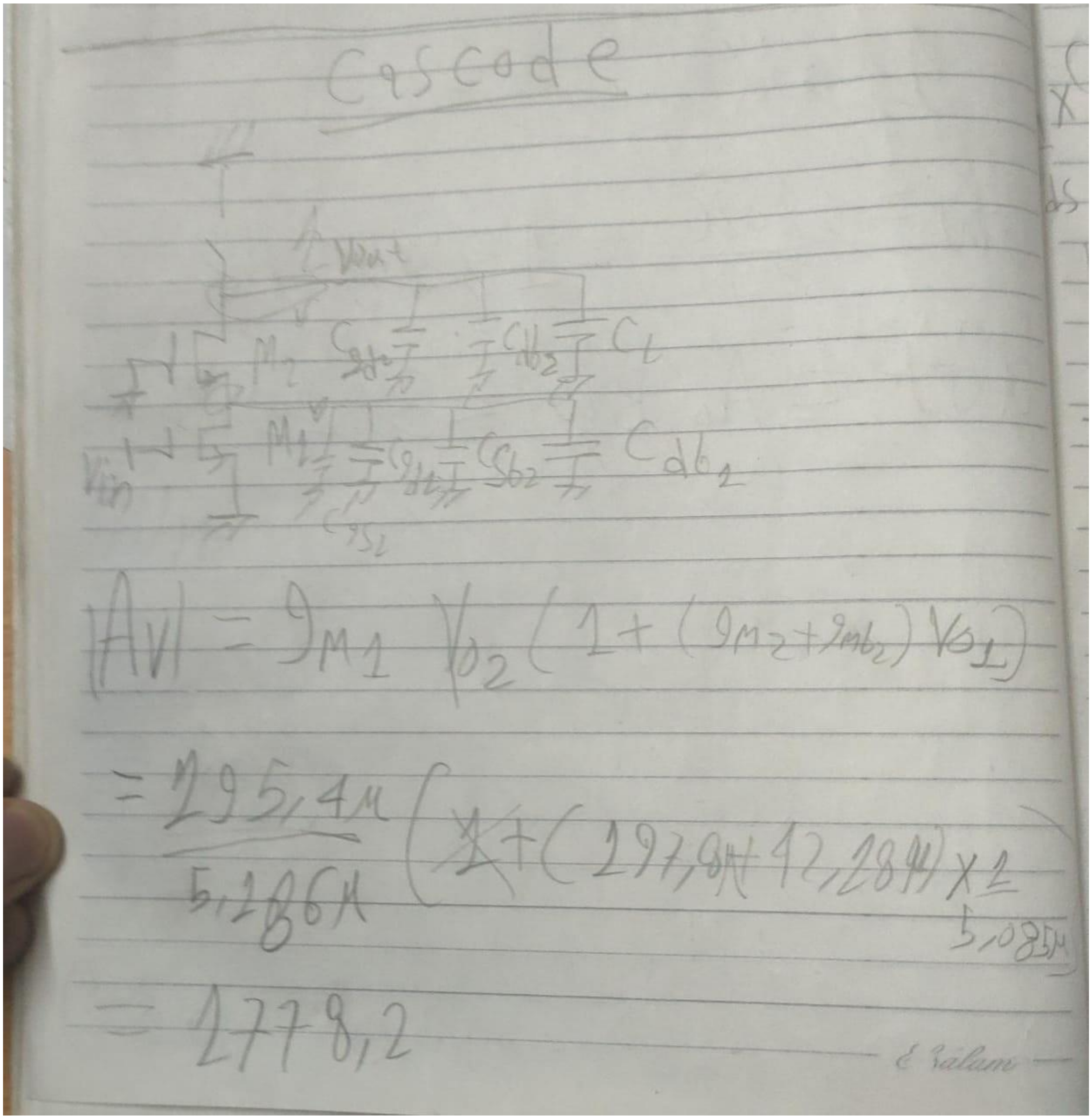
$$f = \frac{\omega}{2\pi} = 636,6\,K$$

Subject موضوع الدرس Date التاريخ

$$UGF = f\,A = 49,7 \times 636,6\,k$$

$$= 31,6M$$

Cascode:


Cascode
Vout
M2
M1
Vin
CL
Cdb2
Csb2
|Av| = gm1 ro2 (1 + (gm2 + gmb2) ro1)
= 295,4µ / 5,286µ (1 + (297,9µ + 42,28µ) × 1 / 5,085µ)
= 1778,2

Subject موضوع الدرس

Date التاريخ

$$W_{m1} = \frac{1}{(1pF + 857,69 + 1,199)\left(\frac{197,8 + 42,29}{5,196 + 5,083}\right)}$$

$$= 110 K$$

$$BW = \frac{110K}{2\pi} = 17,5 \; K \; Hz$$

$$UGF = A_0 \; BW = 31,13 \; M$$

Analytically in cs and cascode cases we can consider GBW=UGF

4 REPORT A TABLE COMPARING THE DC GAIN, BW, UGF, AND GBW OF BOTH CIRCUITS FROM SIMULATION AND HAND ANALYSIS.

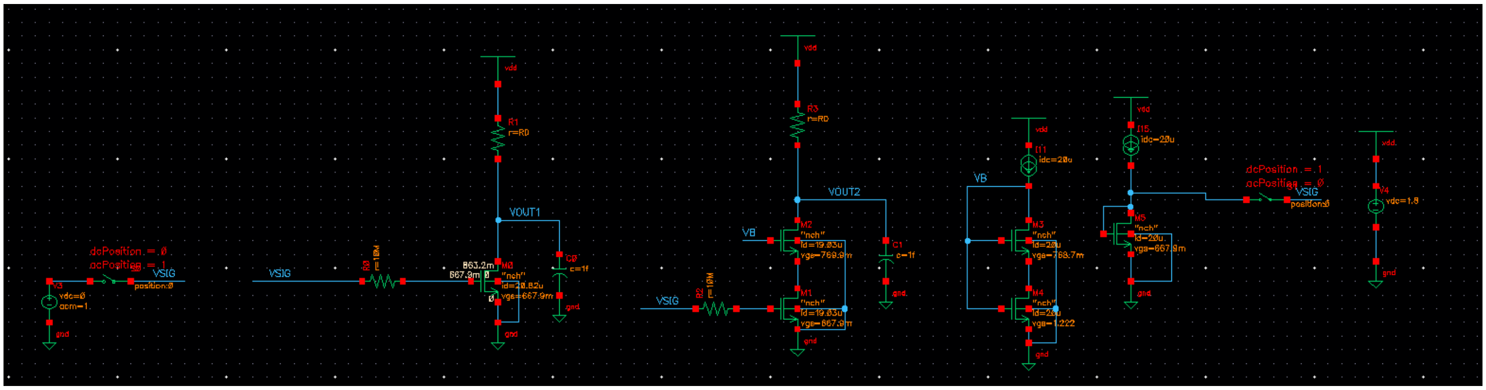
	Simulation		hand analysis	
	CS	Cascode	CS	Cascode
DC GAIN	49.65	1.817k	49.7	1.78k
BW	635.1k	16.75k	636.6k	17.5k
GBW	31.62M	30.5M	31.6M	31.13M
UGF	31.6M	30.63M	31.6M	31.13M

5 COMMENT ON THE RESULTS.

Dc gain in Cascode is much bigger than the gain in CS as it boosts Rout (Gm isn't boosted), and if we compared the hand analysis with the simulation results, we will see they are almost the same , and the increase in Rout causes the output pole to be the dominant pole and decreases the bandwidth, While keeping GBW almost unchanged because it is not dependent on Rout in cascode for gain.

PART 3 [Optional]: Cascode for BW

1 Create a new schematic. Copy the old schematic instances to the new one. Make the following modifications

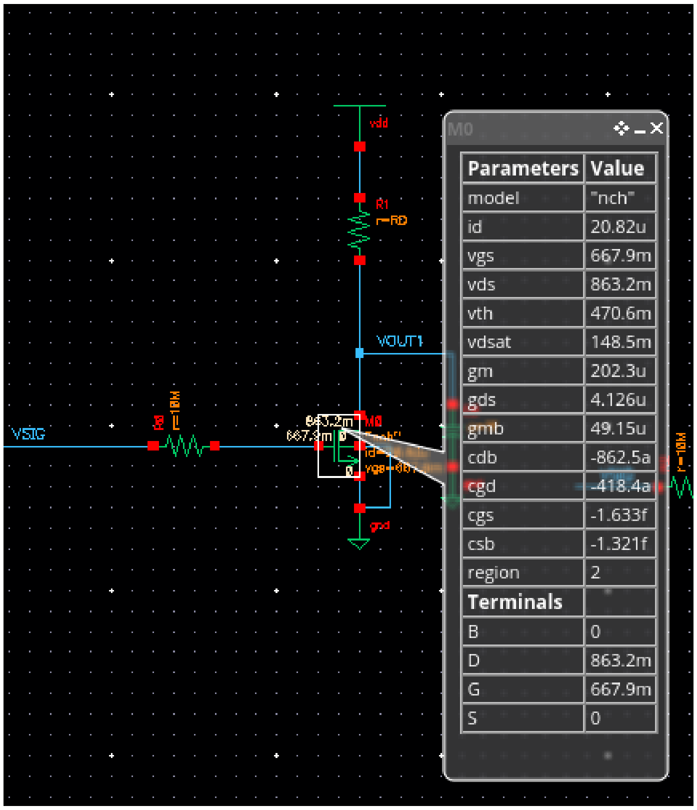


2 Calculate RD analytically such that the voltage drop on it is ≈ $VDD/2$

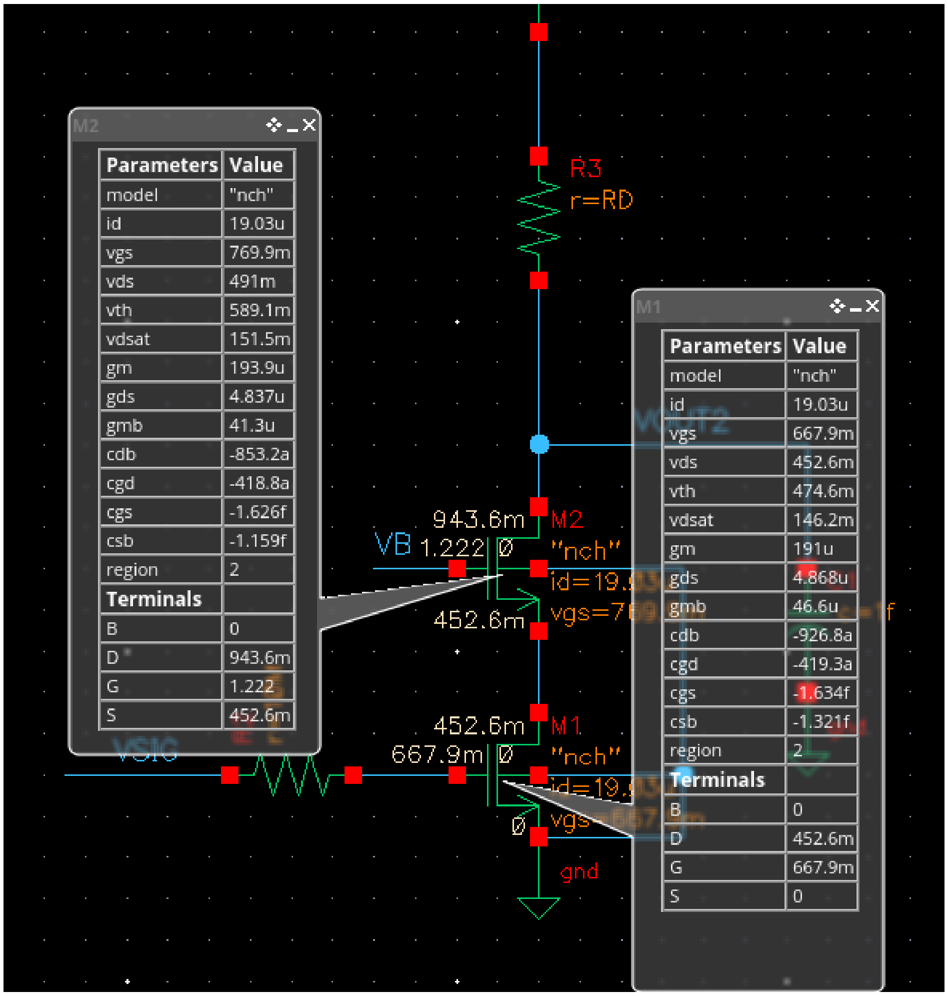
RD = $\frac{1.8/2}{20uA}$ =45k ohm

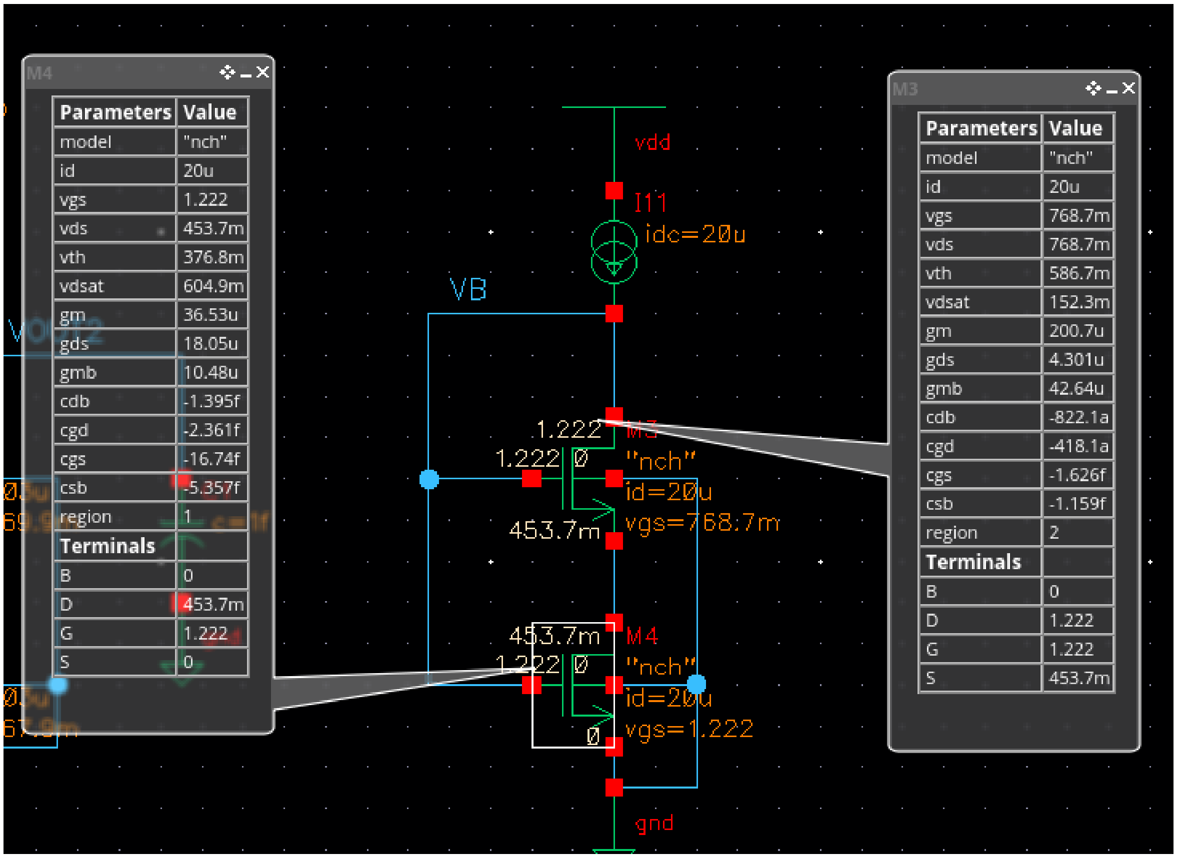
3 Simulate the DC OP of the new CS and cascode amplifiers

M0 (new cs)

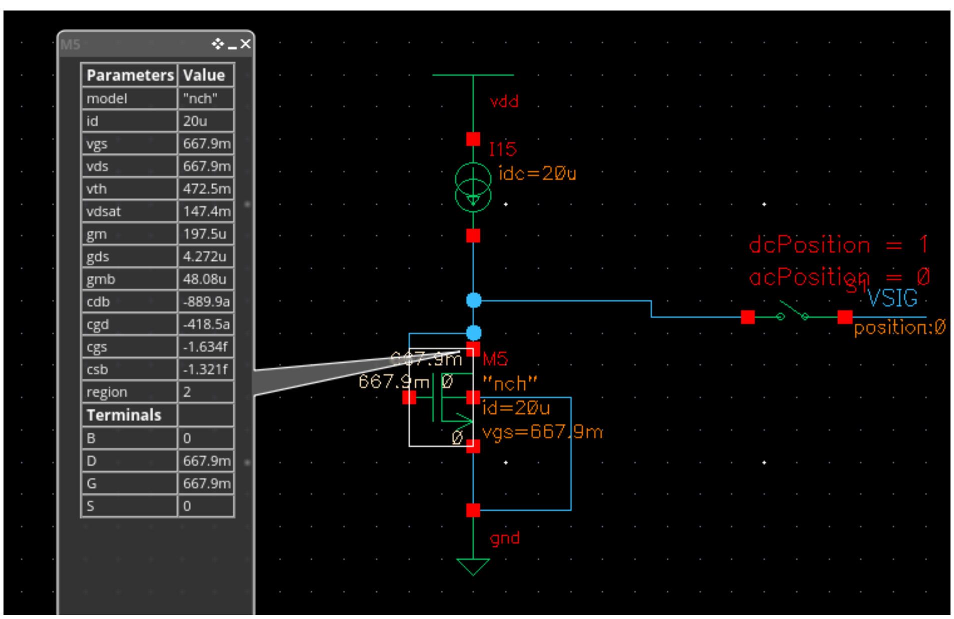


M1 & M2 cascode amplifiers :





M4
Parameters | Value
model | "nch"
id | 20u
vgs | 1.222
vds | 453.7m
vth | 376.8m
vdsat | 604.9m
gm | 36.53u
gds | 18.05u
gmb | 10.48u
cdb | -1.395f
cgd | -2.361f
cgs | -16.74f
csb | -5.357f
region | 1
Terminals
B | 0
D | 453.7m
G | 1.222
S | 0
vdd
I11
idc=20u
VB
1.222
1.222 0
"nch"
id=20u
vgs=768.7m
453.7m
453.7m
M4
1.222 0
"nch"
id=20u
vgs=1.222
0
gnd
M3
Parameters | Value
model | "nch"
id | 20u
vgs | 768.7m
vds | 768.7m
vth | 586.7m
vdsat | 152.3m
gm | 200.7u
gds | 4.301u
gmb | 42.64u
cdb | -822.1a
cgd | -418.1a
cgs | -1.626f
csb | -1.159f
region | 2
Terminals
B | 0
D | 1.222
G | 1.222
S | 453.7m



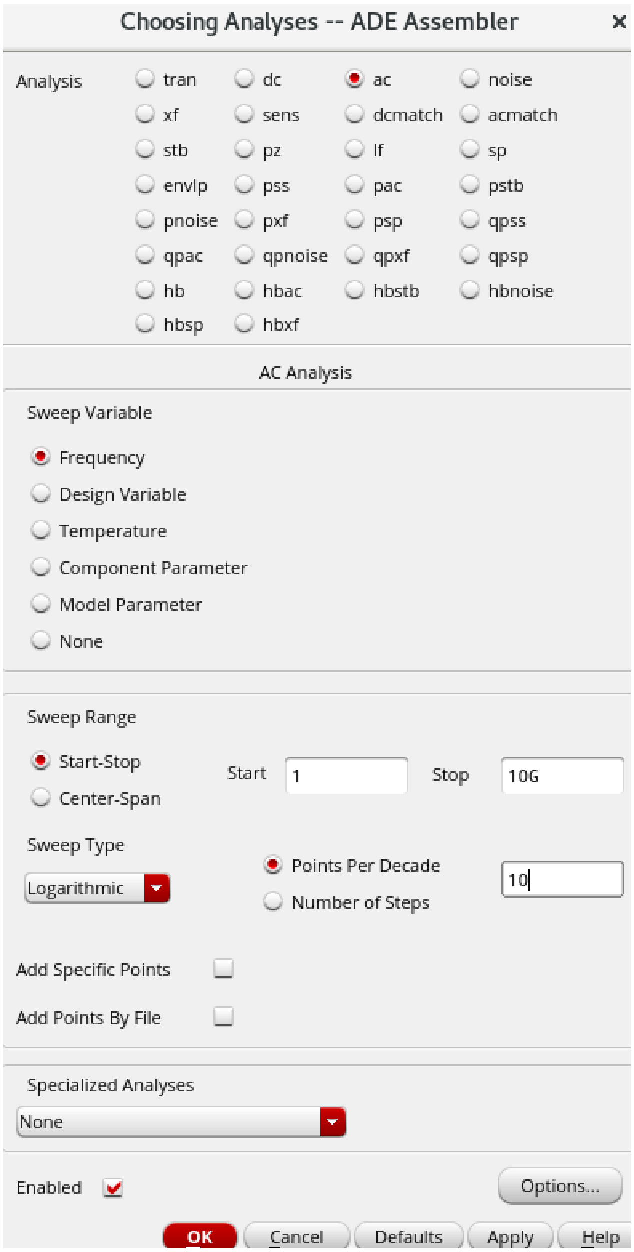
M5
Parameters | Value
model | "nch"
id | 20u
vgs | 667.9m
vds | 667.9m
vth | 472.5m
vdsat | 147.4m
gm | 197.5u
gds | 4.272u
gmb | 48.08u
cdb | -889.9a
cgd | -418.5a
cgs | -1.634f
csb | -1.321f
region | 2
Terminals
B | 0
D | 667.9m
G | 667.9m
S | 0
vdd
I15
idc=20u
dcPosition = 1
acPosition = 0
VSIG
position:0
667.9m
667.9m 0
M5
"nch"
id=20u
0
vgs=667.9m
gnd

4 CHECK THAT ALL TRANSISTORS OPERATE IN SATURATION.

All transistors are in saturation as they have vds>vdsat. But only M4 (bottom transistor in VB circuit) is in triode.

AC Analysis

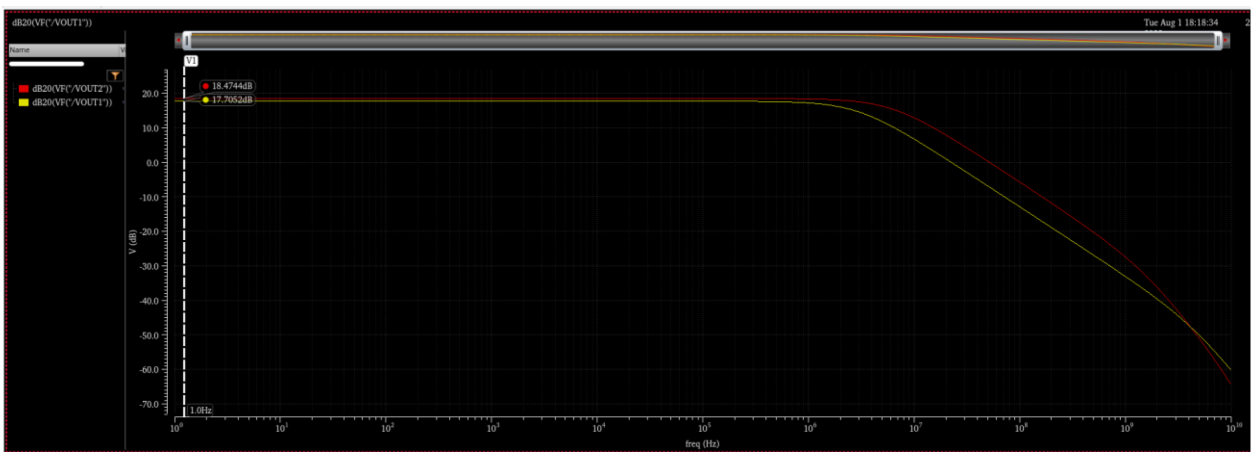
1 Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.



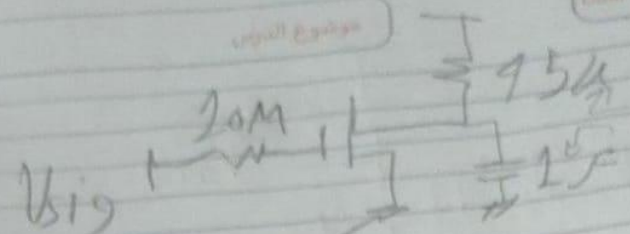
2 USE CALCULATOR TO CREATE EXPRESSIONS FOR CIRCUIT PARAMETERS (DC GAIN, BW, GBW, AND UGF) AND EXPORT THEM TO ADEXL AS IN PART 2

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab3_lab3part3_1	dB20(VF("/VOUT1"))				
lab3_lab3part3_1	ymax(dB20(VF("/VOUT1")))	17.71			
lab3_lab3part3_1	ymax(mag(VF("/VOUT1")))	7.678			
lab3_lab3part3_1	bandwidth(VF("/VOUT1") 3 "low")	2.962M			
lab3_lab3part3_1	gainBwProd(VF("/VOUT1"))	22.79M			
lab3_lab3part3_1	dB20(VF("/VOUT2"))				
lab3_lab3part3_1	ymax(dB20(VF("/VOUT2")))	18.47			
lab3_lab3part3_1	ymax(mag(VF("/VOUT2")))	8.389			
lab3_lab3part3_1	bandwidth(VF("/VOUT2") 3 "low")	6.222M			
lab3_lab3part3_1	gainBwProd(VF("/VOUT2"))	52.32M			
lab3_lab3part3_1	unityGainFreq(VF("/VOUT1"))	22.83M			
lab3_lab3part3_1	unityGainFreq(VF("/VOUT2"))	52.21M			

3 REPORT THE BODE PLOT (MAGNITUDE) OF CS AND CASCODE APPENDED ON THE SAME PLOT.



4 CALCULATE DC GAIN, BW, AND GBW OF BOTH CIRCUIT



$$|A_0| = g_m (R_D // r_o) = g_m \frac{R_D r_o}{R_D + r_o}$$

$$= 7,67$$

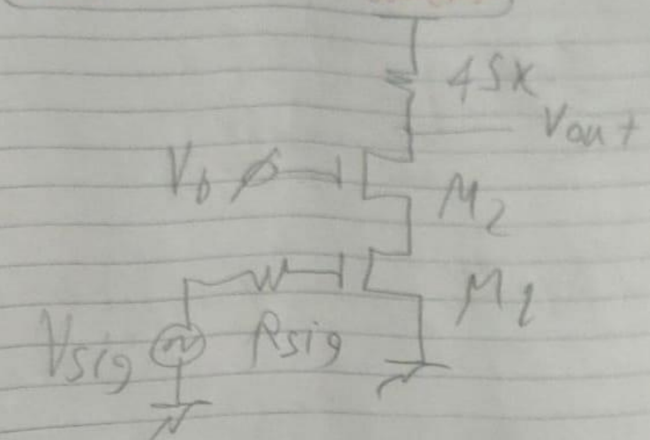
BW: $C_L \downarrow\downarrow$ and $R_{out} \downarrow\downarrow$, $R_{sig} \uparrow$

$$\omega_H = \frac{1}{R_{sig}\left(C_{gs} + C_{gd}(1 + A_0)\right)}$$

$$= 19,02\,M$$

$$BW = 3,02\,MHz$$

$$GBW = A_0 f_H = 23,16\,M$$



$$A_0 = g_{m2}\{V_{o2}[(g_{m2}+g_{mb2})V_{o2} \,//\, R_D]\}$$

$$\simeq g_{m2} R_D = 8{,}6$$

BW↓ R_D↓ R_{sig}↑ I/P pole dom

$$\omega = \frac{1}{R_{sig}(C_{gs1}+2C_{gd1})} = 40{,}4M$$

$$f_H \simeq 6{,}3\,M$$

$$GBW = A_0 f_H = 54{,}2\,M$$

5 Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis. Comment on the results.

	Simulation		hand analysis	
	CS	Cascode	CS	Cascode
DC GAIN	7.678	8.389	7.67	8.6
BW	2.962M	6.22M	3.02M	6.3M
GBW	22.79M	52.32M	23.16M	54.2M
UGF	22.83M	52.21M	23.16M	54.2M

When Rsig is increased and Rout is decreased, we notice that In CS the gain is decreased, but the bandwidth is increased compared to using an ideal load(IDC), because this made the input pole dominant, In cascode the gain is decreased as the output impedance is decreased and input is increased this made the input pole the dominant pole. But the input pole is larger than the common source input pole, which means that the bandwidth was extended, this is due to the Miller effect being decreased, And the gain bandwidth product is no longer the same as in CS but it is higher.