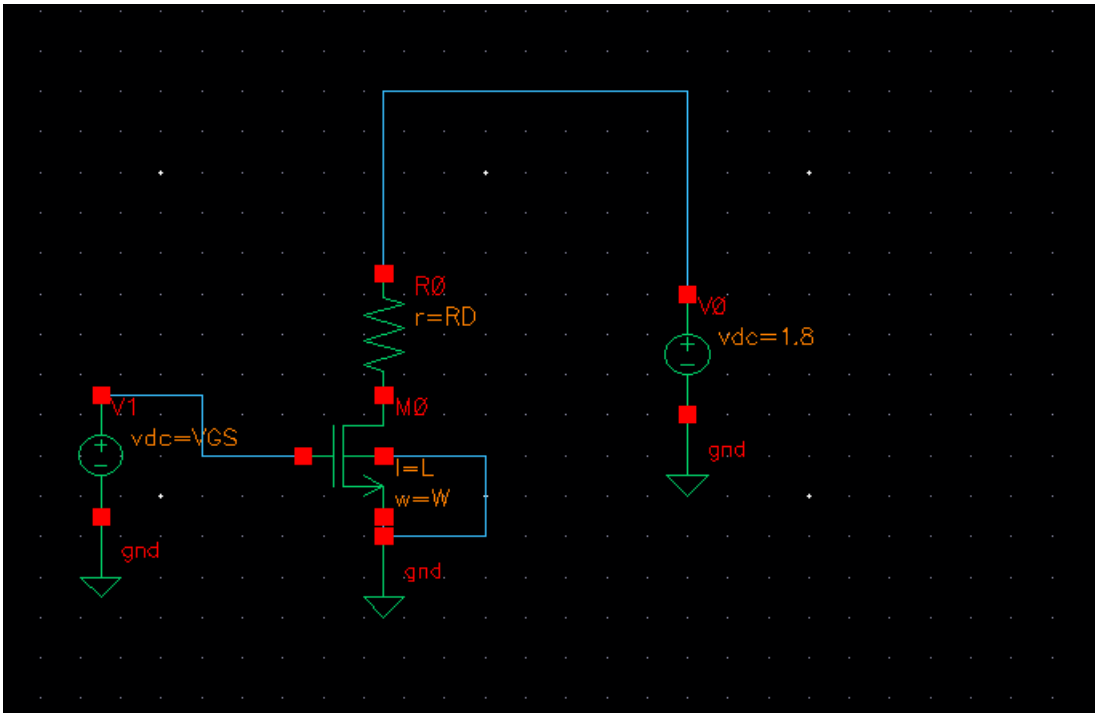
Lab 02 Common Source Amplifier

PART 1: Sizing Chart

1 ASSUMING CM OUTPUT = $VRD = VDD/2$ AND GIVEN THE DC BIAS CURRENT, DETERMINE THE VALUE OF RD.



$$RD = \frac{1.8 - 0.9}{150\mu} = 9K\ \Omega$$

Vrd=0.9 V

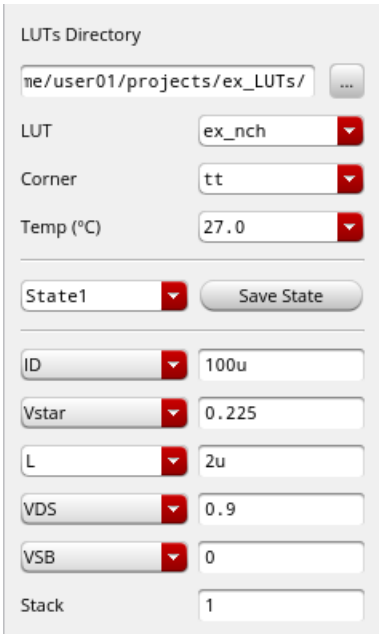
2 GIVEN Av AND VRD , CALCULATE THE REQUIRED $V*$ (AGAIN NOTE THAT $V* \neq Vov$ FOR A REAL MOSFET). LET'S NAME THIS VALUE $VQ*$.

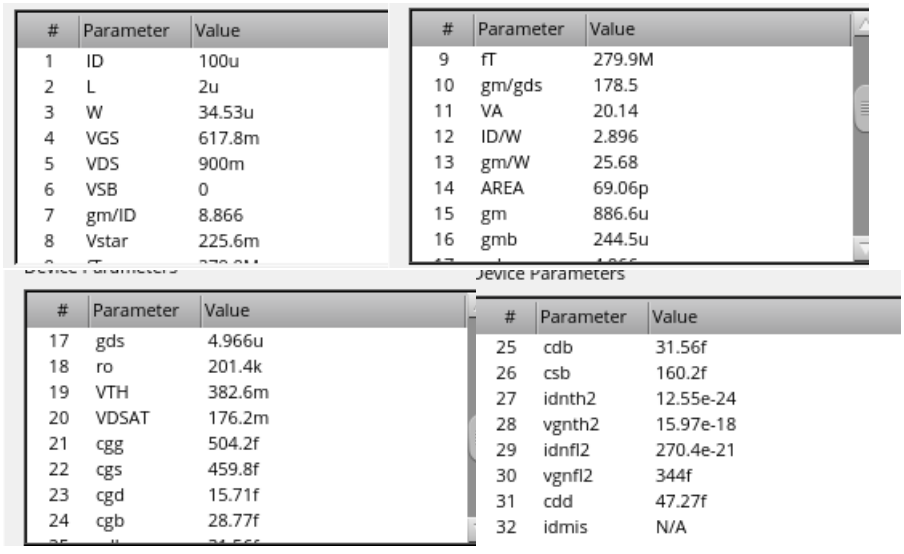
$$|Av| = \frac{2Vrd}{V*}\ , V* = \frac{2Vrd}{|Av|}$$

$$V* = \frac{2 * 0.9}{6} = 0.225\ V$$

3 CALCULATE **W**

NMOS :





#	Parameter	Value
1	ID	100u
2	L	2u
3	W	34.53u
4	VGS	617.8m
5	VDS	900m
6	VSB	0
7	gm/ID	8.866
8	Vstar	225.6m

#	Parameter	Value
9	fT	279.9M
10	gm/gds	178.5
11	VA	20.14
12	ID/W	2.896
13	gm/W	25.68
14	AREA	69.06p
15	gm	886.6u
16	gmb	244.5u

Device Parameters

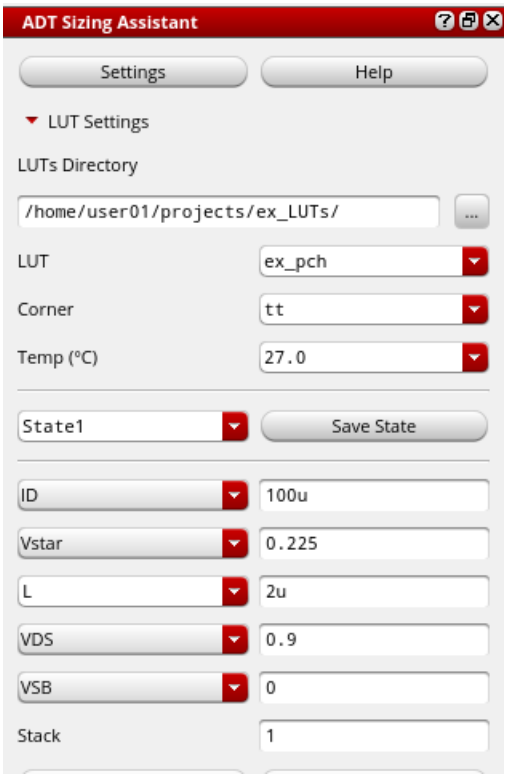
#	Parameter	Value
17	gds	4.966u
18	ro	201.4k
19	VTH	382.6m
20	VDSAT	176.2m
21	cgg	504.2f
22	cgs	459.8f
23	cgd	15.71f
24	cgb	28.77f

#	Parameter	Value
25	cdb	31.56f
26	csb	160.2f
27	idnth2	12.55e-24
28	vgnth2	15.97e-18
29	idnfl2	270.4e-21
30	vgnfl2	344f
31	cdd	47.27f
32	idmis	N/A

W	Gm	Gds	R0	Av
34.53u	886.6u	4.966u	201.4k	$\lvert Av(nmos)\rvert = 886.6u * \frac{9k * 201.4K}{9k + 201.4K} = 7.63 \sim 7.6$

Meet the specs

PMOS



#	Parameter	Value
1	ID	100u
2	L	2u
3	W	139.2u
4	VGS	616.9m
5	VDS	900m
6	VSB	0
7	gm/ID	8.859
8	Vstar	225.8m
9	fT	70.14M
10	gm/gds	208.4
11	VA	23.52
12	ID/W	718.5m
13	gm/W	6.365
14	AREA	278.3p
15	gm	885.9u

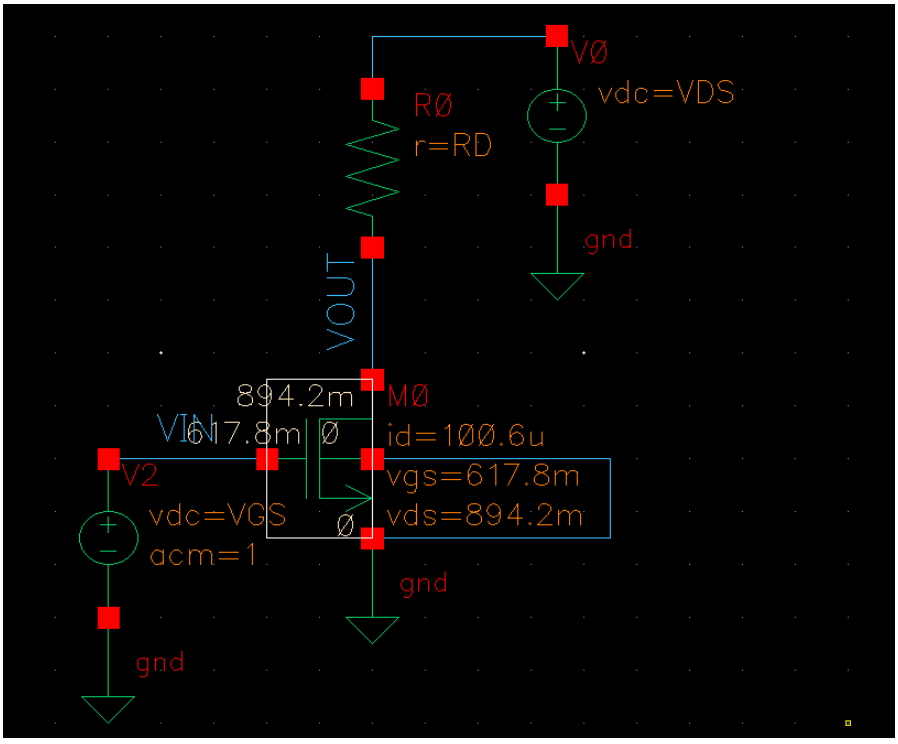
#	Parameter	Value
16	gmb	287.6u
17	gds	4.252u
18	ro	235.2k
19	VTH	393.4m
20	VDSAT	182.9m
21	cgg	2.01p
22	cgs	1.817p
23	cgd	91.24f
24	cgb	102.4f
25	cdb	123.4f
26	csb	664.2f
27	idnth2	13.01e-24
28	vgnth2	16.58e-18
29	idnfl2	54.6e-21
30	vgnfl2	69.58f

W	Gm	Gds	R0	Av
139.2u	885.9u	4.252u	235.2k	$\lvert Av(nmos)\rvert = 885.9u * \frac{9k * 235.2K}{9k + 235.2K} = 7.68 \sim 7.7$

The results meet the specs.

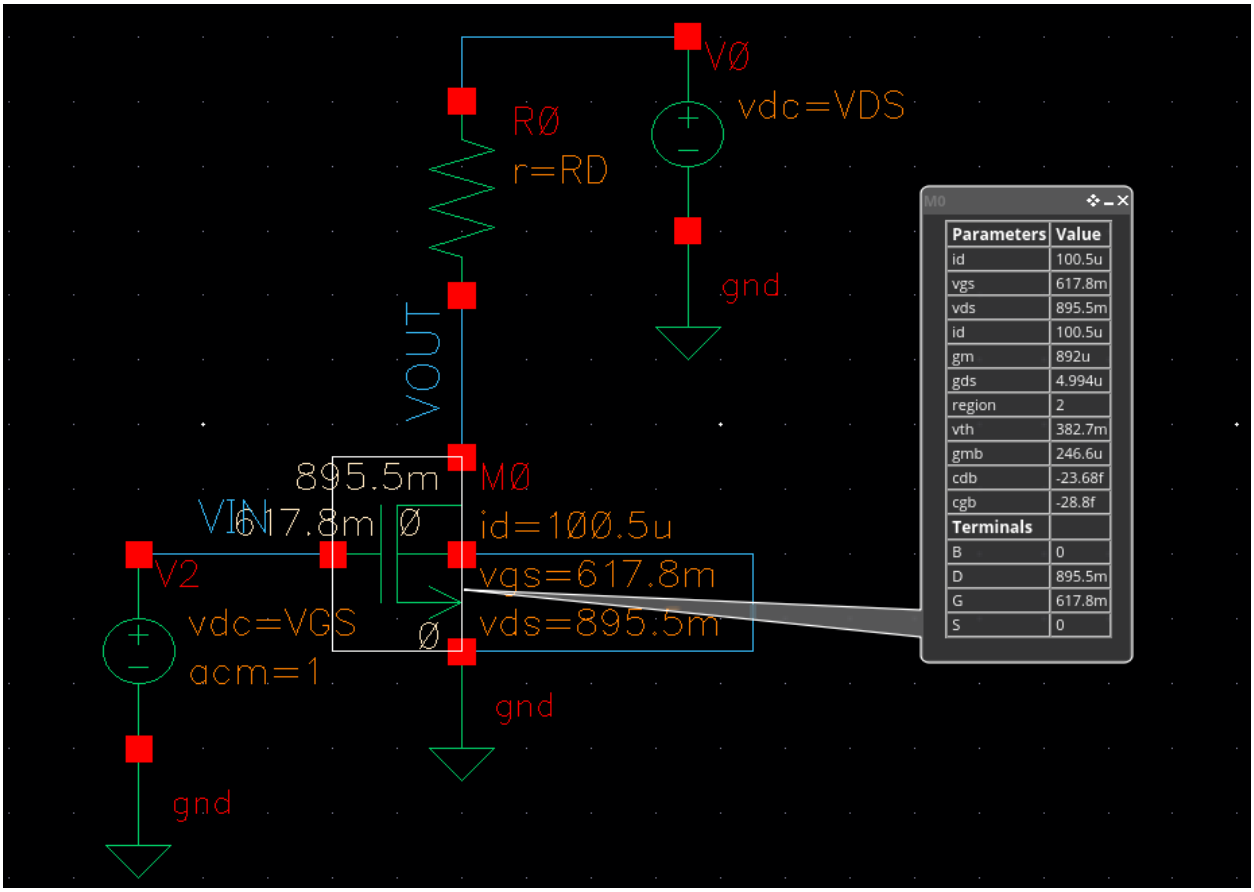
PART 2: CS Amplifier

1 CREATE A TESTBENCH FOR THE RESISTIVE LOADED CS AMPLIFIER USING THE $VGSQ, RD, L,$ AND W THAT YOU GOT FROM THE PREVIOUS PART



Assume ac small signal 1 m to find the gain in required 6 .

2 SIMULATE THE DC OP. REPORT A SNAPSHOT FOR THE KEY OPERATING POINT (OP) PARAMETERS. COMPARE THE RESULTS WITH THE RESULTS YOU OBTAINED IN PART 1. SINCE WE USED CHART-BASED DESIGN, THE RESULTS SHOULD AGREE WELL



	Gm	ID	Gds
Part 2	892u	100.5u	4.994u
Part 1	$886.6u$	100u	$4.966u$

the results agree well.

Region is 2 which means it works in saturation.

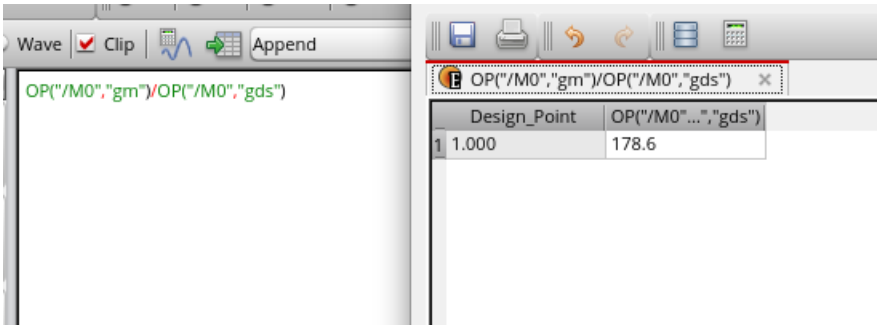
3 COMPARE ro AND RD. IS THE ASSUMPTION OF IGNORING ro JUSTIFIED IN THIS CASE? DO YOU EXPECT THE ERROR TO REMAIN THE SAME IF WE USE MIN L?

r0= 1/gds = 200.24K , RD= 9K , r0 >>RD, Req=$\frac{6*168.55}{6+168.55} k = 8.99k$,
yes the error is so small so it is justified to ignore r0.

the error expected to be larger because of short channel effects (channel length modulation) as early voltage (VA) will decrease so r0 would be smaller .

4 CA LCULATE THE INTRINSIC GAIN OF THE TRANSISTOR.

|Av|=gm*r0=gm/gds=178.6



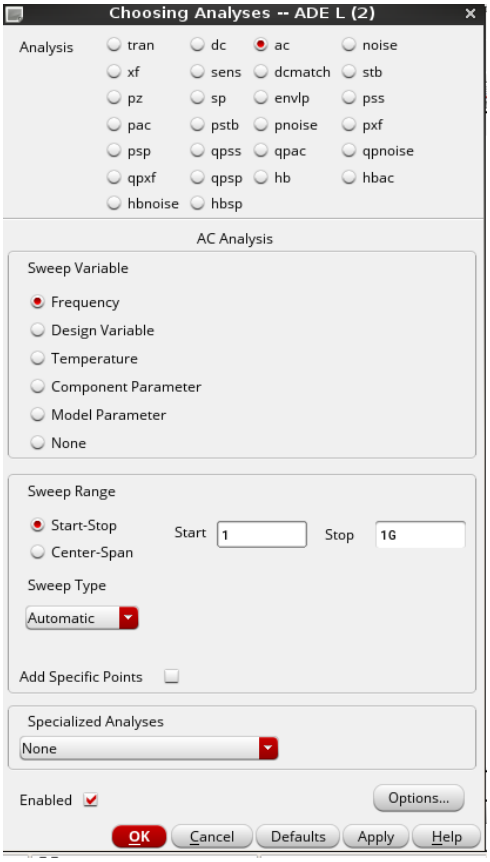
5 CALCULATE THE AMPLIFIER GAIN ANALYTICALLY. WHAT IS THE RELATION (≪,<,= ,>, ≫) BETWEEN THE AMPLIFIER GAIN AND THE INTRINSIC GAIN?

GM=-gm , RS=0,vgs=0 && Rout=RD||r0

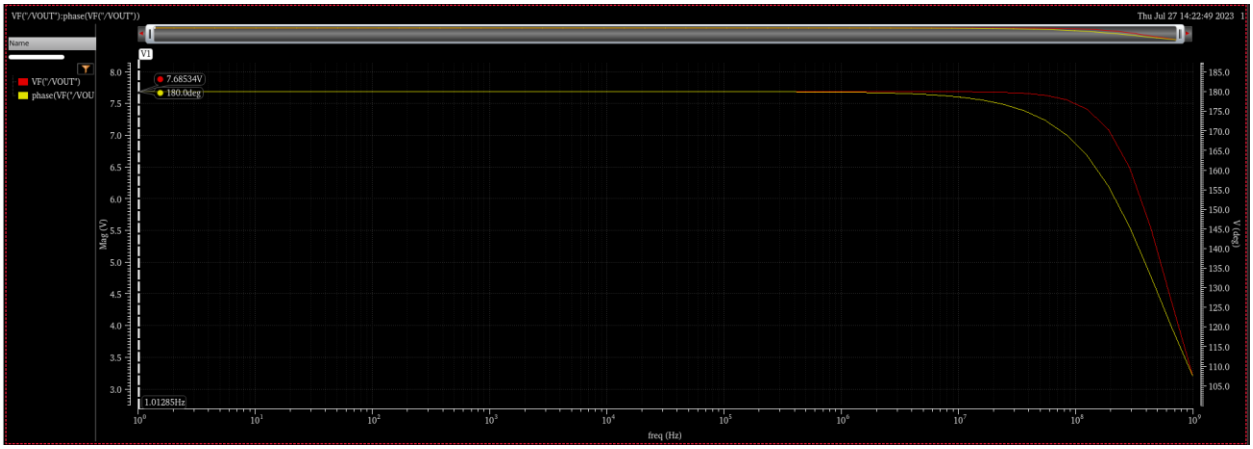
|Av|=gm * RD||r0 = $892 * 10^{-3} * \frac{9*10^3*200.24*10^3}{9*10^3+200.24*10^3}$ = 7.68 ~7.7

the amplifier gain << the intrinsic gain , because Rd is much less than r0 so it dominates .

6 CREATE A NEW SIMULATION CONFIGURATION AND RUN AC ANALYSIS (FROM 1HZ TO 1GHZ). REPORT THE GAIN VS FREQUENCY. ANNOTATE THE DC GAIN AND MAKE SURE IT MEETS THE SPEC .



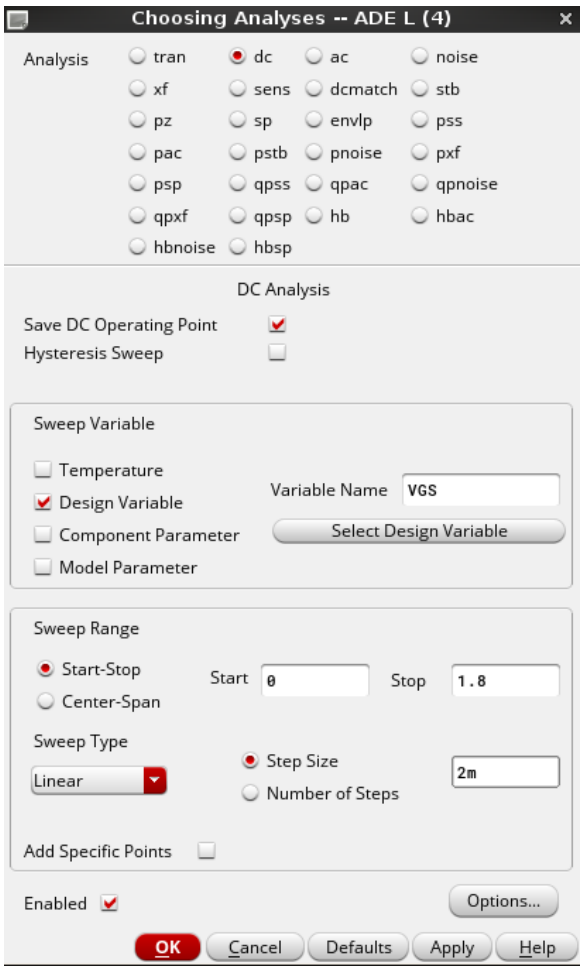
	expr	(VF("/Vout") / VF("/vin"))
	expr	phase((VF("/Vout") / VF("/vin")))



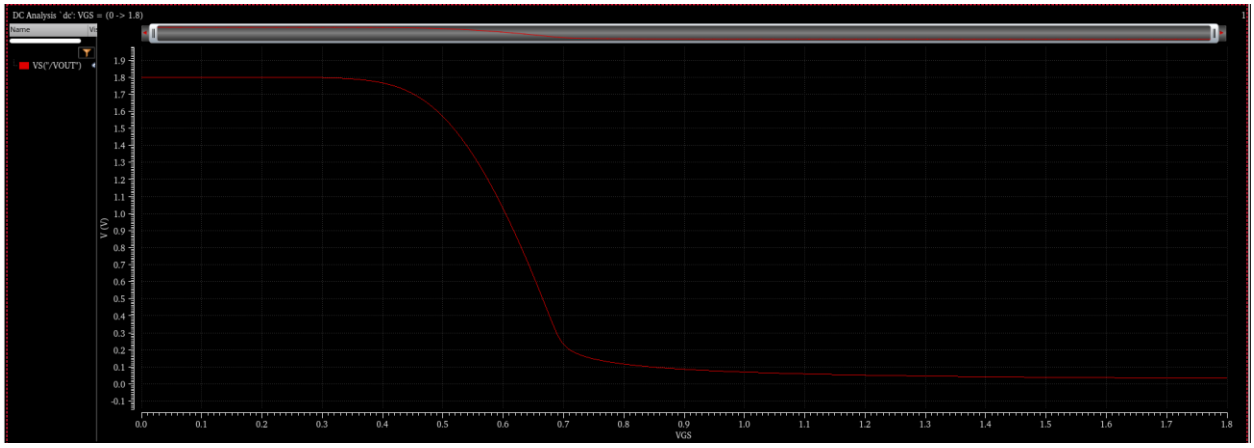
DC gain (when frequency is 1hz) is 7.68 and also there is a 180-degree phase shift, which meets the specs, we note that when the frequency is too high (more than 10^7) the gain drops.

Gain Non-Linearity

1 CREATE A NEW SIMULATION CONFIGURATION. PERFORM A DC SWEEP FOR THE INPUT VOLTAGE FROM 0 TO VDD WITH 2MV STEP.

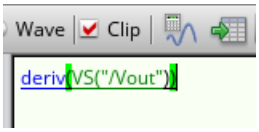


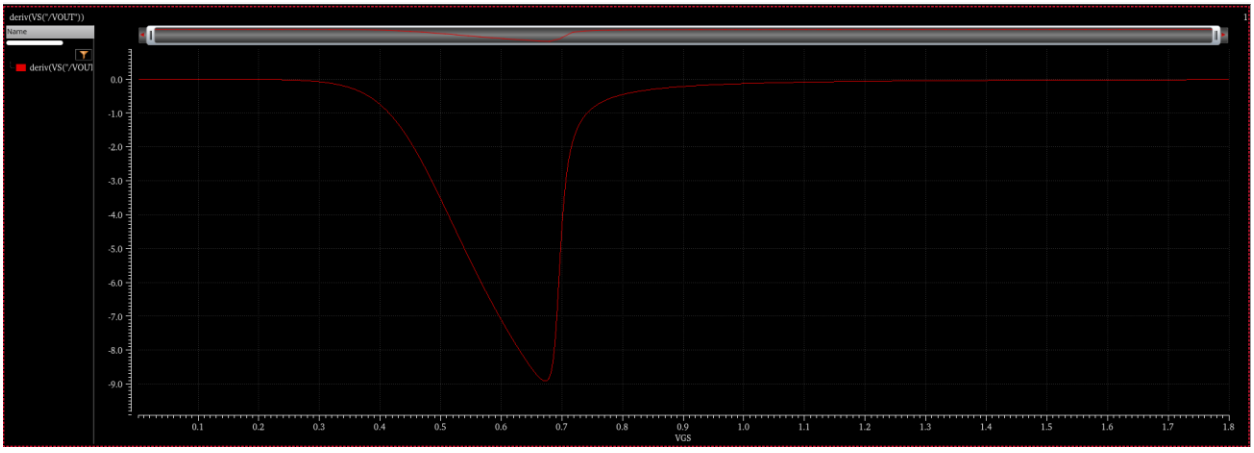
2 Report VOUT vs VIN. Is the relation linear? Why?



The relation is not linear, because VOUT depends on ID (VOUT = VDD – ID * RD), and ID depends on VGS(input) which approximately has quadratic relation with VGS(input) in saturation, and actually Vout variation depends on Vin variation with the slope of this plot which is the gain which is a function of VGS(input), and gain is not linear as it is a function of gm,r0 which are by the way functions of Vin.

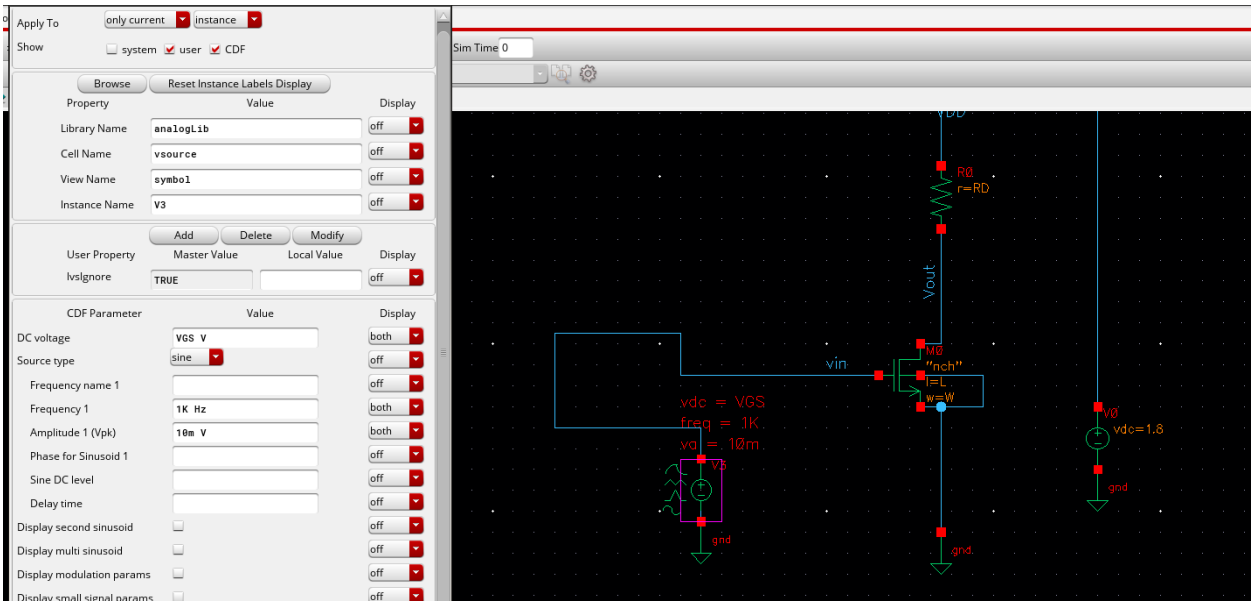
3 Calculate the derivative of VOUT using calculator. Plot the derivative vs VIN. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?



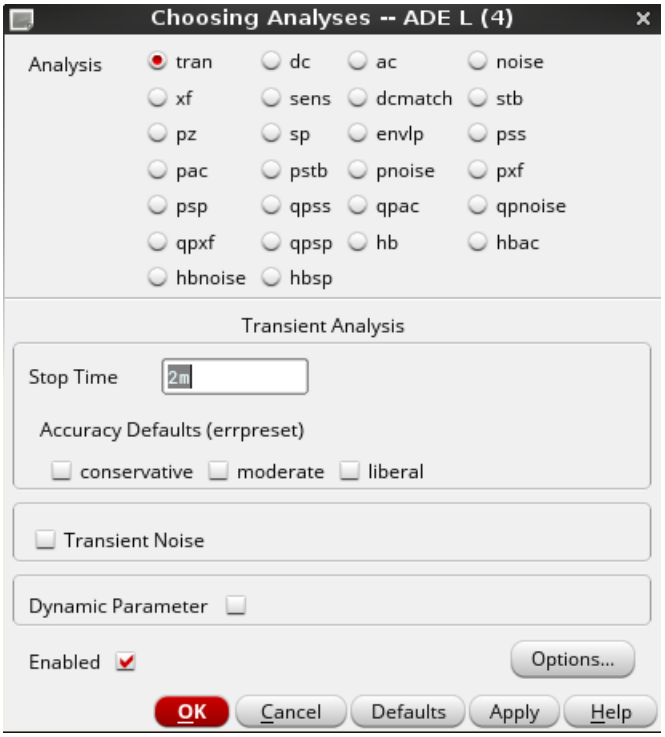


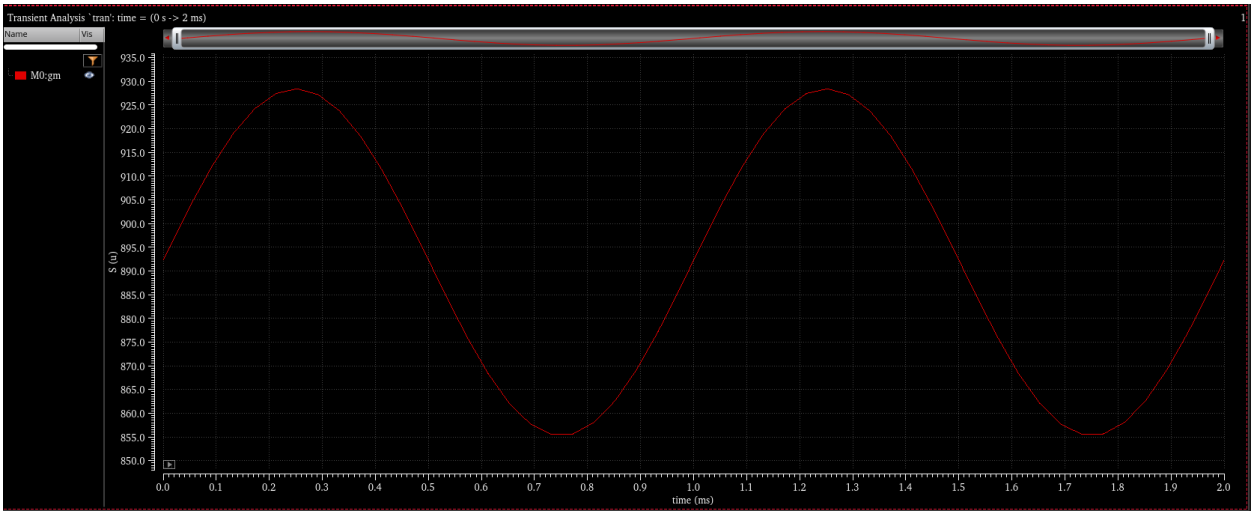
No, gain is not linear because it is a function of gm, r0 (|Av|=gm(RD||r0)) which are actually functions of VGS(Vin) (in case of r0 changing Vin changes Id with it, r0 is the slope of id vs Vout(Vds), so r0 also depends on the change of Vin) then the gain depends on Vin (the input) which make it non linear.

4 SET THE PROPERTIES OF THE VOLTAGE SOURCE TO APPLY A TRANSIENT STIMULUS (SINE WAVE OF 1KHZ FREQUENCY AND 10MV AMPLITUDE SUPERIMPOSED ON THE DC INPUT VOLTAGE).

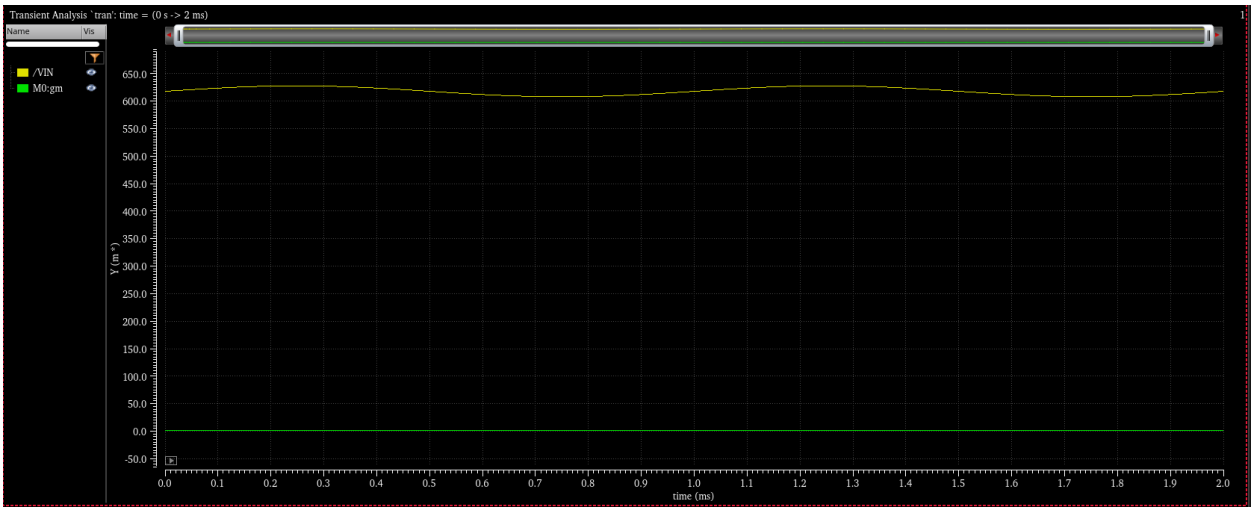


5 CREATE A NEW SIMULATION CONFIGURATION. RUN TRANSIENT SIMULATION FOR 2MS. PLOT GM VS TIME. DOES GM VARY WITH THE INPUT SIGNAL? WHAT DOES THAT MEAN?





gm vs time



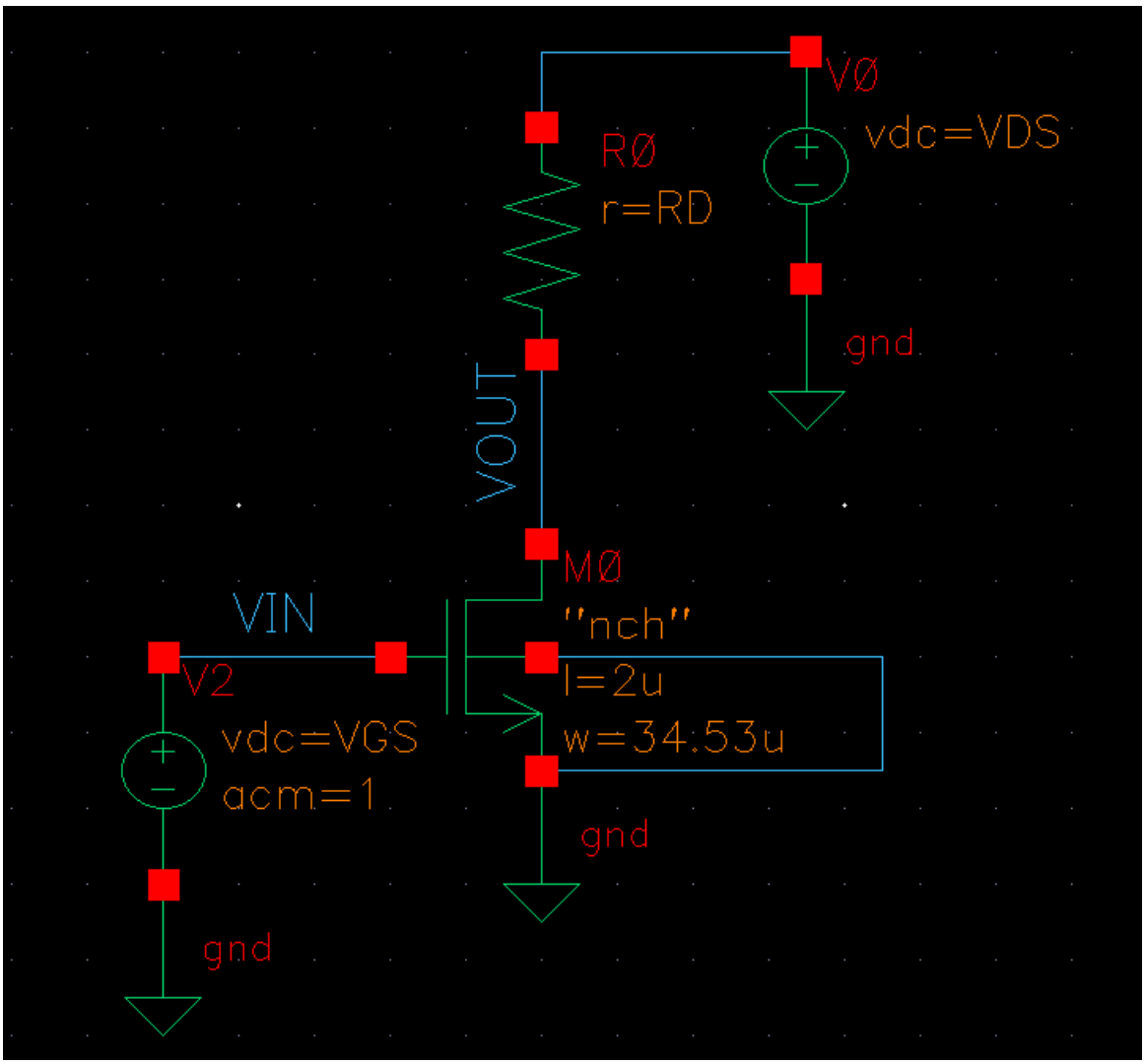
Yes, gm varies with the input signal, as it is the slope of id vs Vgs (vin) , so when the input signal oscillates it changes gm with it, **so the gain is not constant as gain = gm *Rout** , so the small signal linearization model is just an approximation as we consider gm a constant, but that small error is actually acceptable as gm change is very small and could be neglected.

6 IS THIS AMPLIFIER LINEAR? COMMENT.

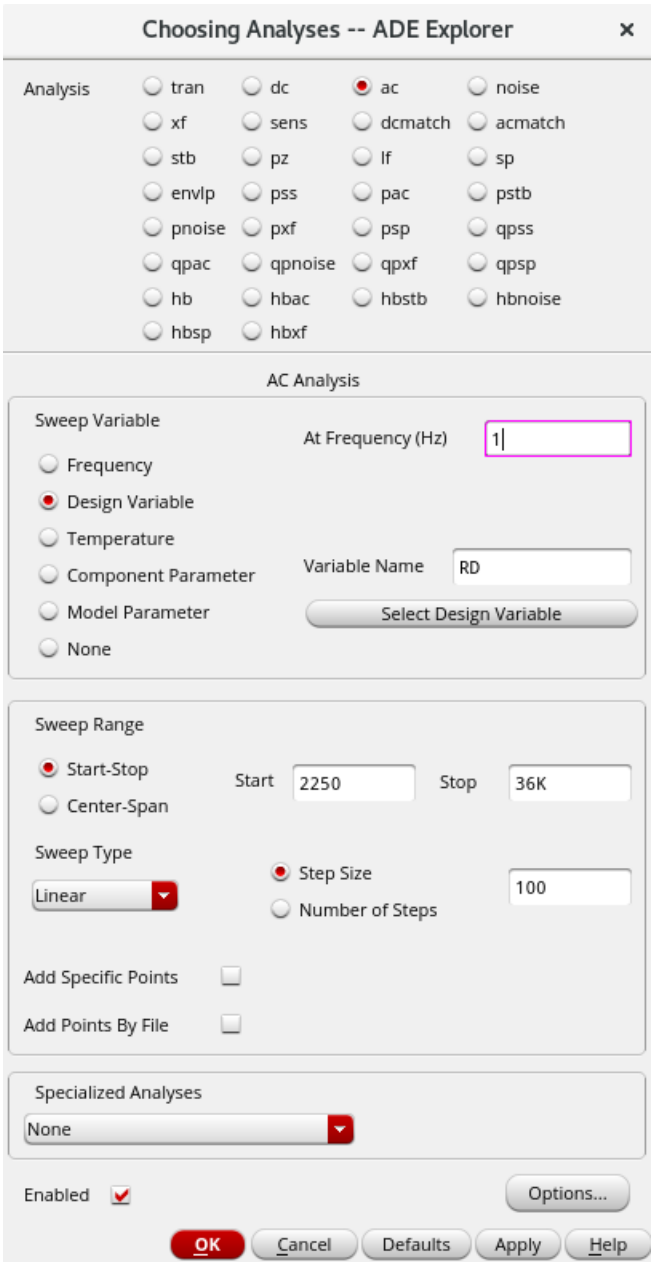
NO , this amplifier 's not linear because the gain is not constant but depends on Vin, because the gain depends on gm and (gm = f(Vin)) and for linear gain, Av should not be f(Vin) but we can solve it by increasing the source resistance.

Maximum Gain

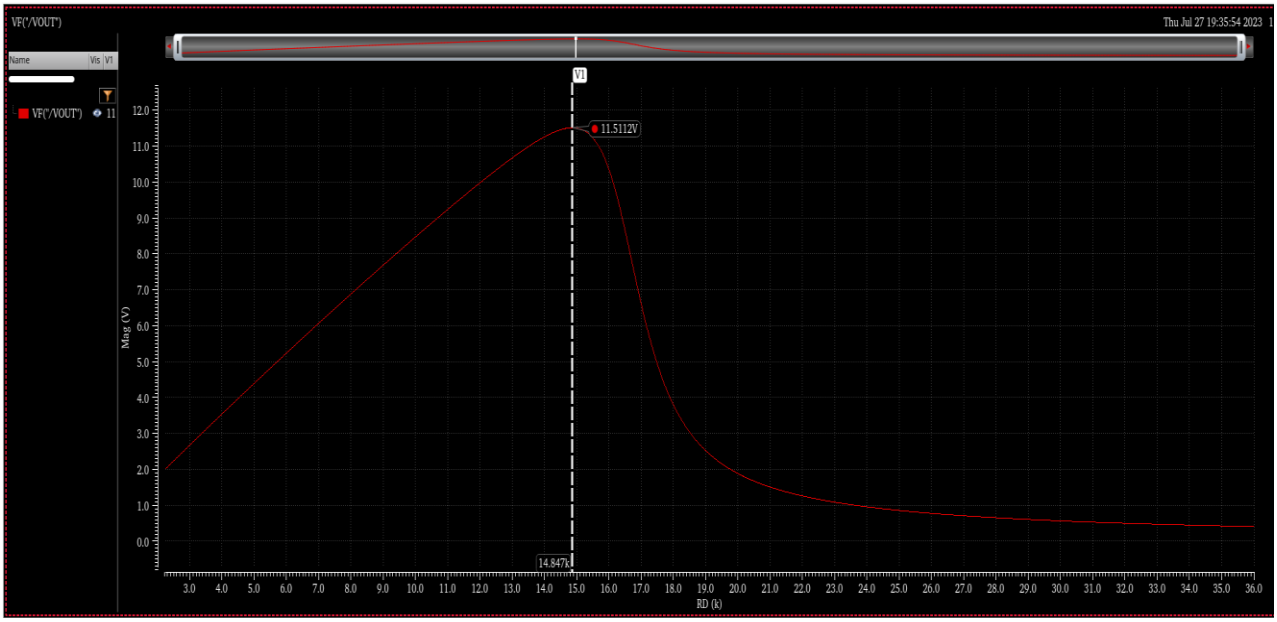
1 SET THE SOURCE AC MAGNITUDE = 1. NOTE THAT AC ANALYSIS IS A LINEAR ANALYSIS, SO WE USE A PAGE 4 OF 5 MAGNITUDE OF ONE SUCH THAT THE OUTPUT IS ITSELF THE GAIN



2 SET AC SIMULATION TO SWEEP DESIGN VARIABLE (RD FROM ¼ THE VALUE YOU SELECTED IN PART 1 TO 4 TIMES THE VALUE YOU SELECTED IN PART 1). SET THE AC SIMULATION FREQUENCY AT 1 HZ (SINGLE FREQUENCY POINT).



3 USE THE CALCULATOR TO PLOT THE GAIN VS RD.



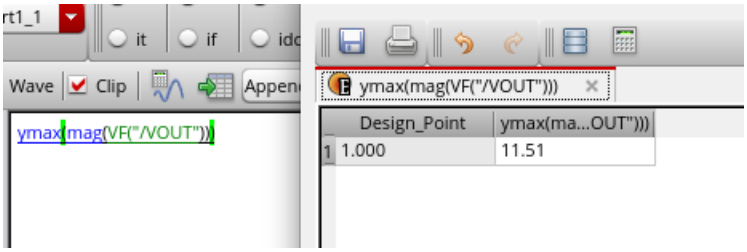
4 YOU WILL FIND THAT THE GAIN INCREASES WITH RD AND THEN DECREASES WITH RD. JUSTIFY THIS BEHAVIOR.

LARGE SIGNAL : VDD=ID*RD + VDS

AS RD increases VDS decreases, because VGS Is constant so ID also approximately constant as long as we are in saturation,
also when we looking from small signal perspective the gain increases, as RD increases and so gain =(RD||R0) * gm also increases.

But then, when RD is more than its max value, the transistor leaves the saturation to triode so the current =f(vgs,vds) and the gain not high like in saturation so it decreases.

5 WHAT IS THE VALUE OF RD THAT GIVES THE HIGHEST GAIN? WHAT IS THE HIGHEST GAIN?



highest gain is 11.51

R=14.85K

6 ANALYTICALLY CALCULATE THE VALUE OF RD THAT GIVES THE HIGHEST GAIN AND THE HIGHEST GAIN USING THE EXPRESSIONS IN PART 1. COMPARE SIMULATION AND ANALYSIS RESULTS.

$$RD = \frac{VDD - V*}{ID} = \frac{1.8 - 0.225}{100u} = 15.75\ K$$

Gain=$\frac{2Vrd}{V*} = \frac{2*15.75*100}{225} = 14$

	SIM	Analytically
RD	14.85 k	15.75 k
HIGHEST GAIN	11.51	14

7 WHAT IS THE AVAILABLE SIGNAL SWING AT THE POINT OF MAXIMUM GAIN?

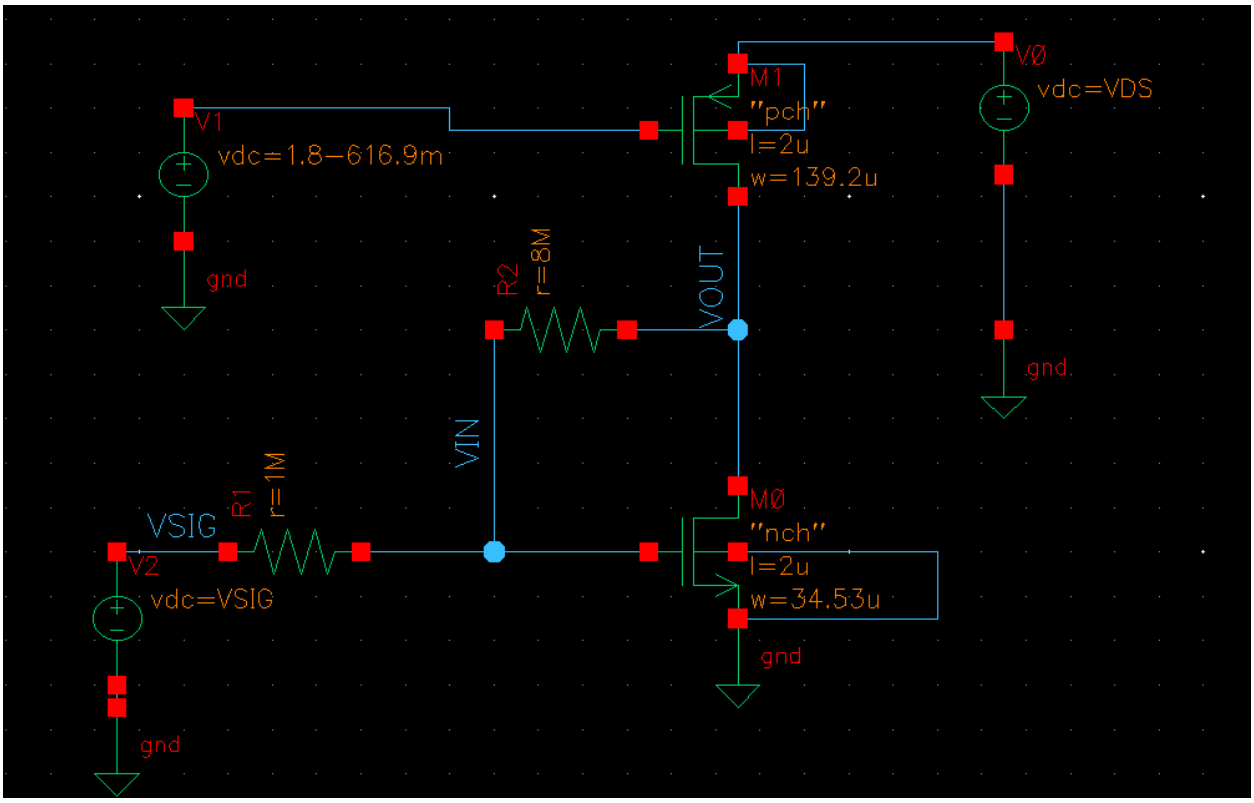
At max gain vds = vout =v* , it can't swing below it as it will leave saturation to triode, but above it, it can swing till the supply voltage VDD=1.8 v (max).

8 IS SCALING DOWN THE SUPPLY VOLTAGE GOOD FOR GAIN? COMMENT.

NO,
VDD=ID*RD + VDS , as VDD decreases and we are it saturation, ID and RD are constant so VDS decreases, till we reach triode, so the gain drop much.

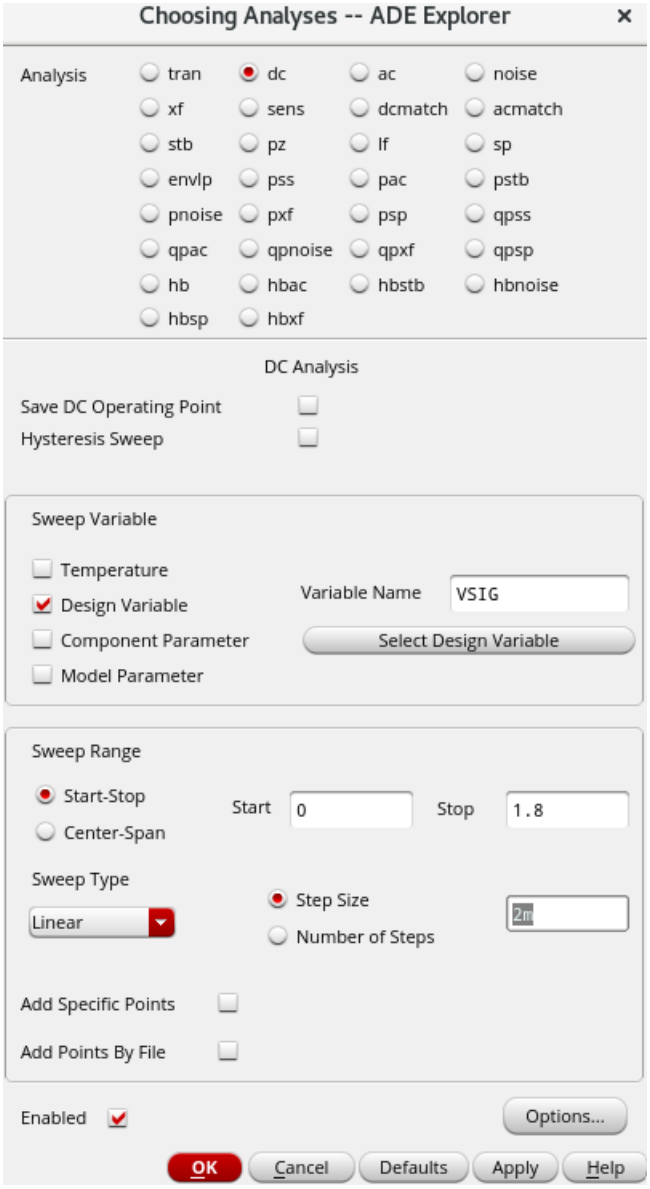
Gain Linearization (feedback)

1 CIRCUIT

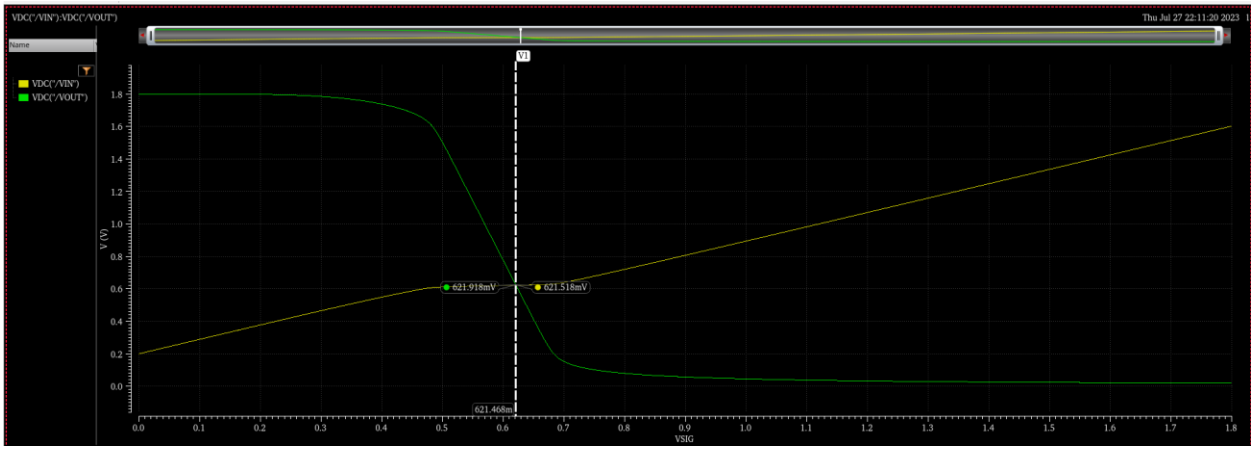


Rf= gain * R1= 8 M ohm

2 PERFORM A DC SWEEP FOR THE INPUT VOLTAGE (VSIG) FROM 0 TO VDD WITH 2MV STEP



3 REPORT VIN AND VOUT VS VSIG (OVERLAID). AT WHAT VOLTAGE DO THE TWO CURVES CROSS? WHY?



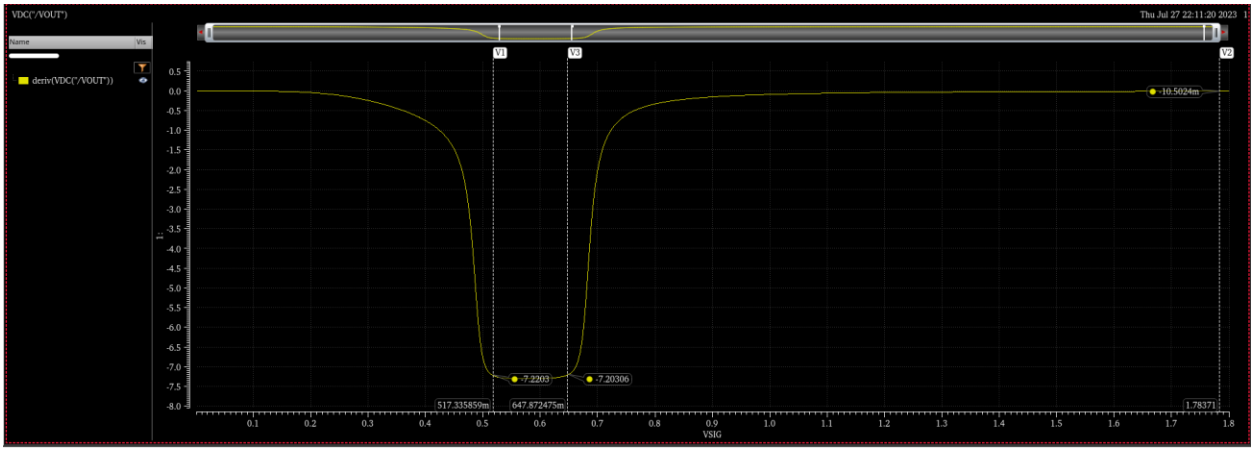
VOUT=VIN AT VSIG = 621.47 mv, VGSQ we got of m1 from part1 = 617.8 mv which is approximately equal to the value of equally Vout and Vin, so the current flowing in the two resistors is equal and it equal zero, so all potentials are equal.

4 IS VOUT VS VSIG LINEAR? WHY?

Yes in saturation only,

The PMOS working as current source with approximately constant current = 100uA , so the nmos transistor is (I to v device) as an approximately constant current equal to 100uA passing through it, vin==VGS of m1 that we calculated before as ID=f(VGS) , so as the current is constant and equal to that value, vin is approximately constant (there is small variation due to feedback circuit and secondary changes) which would make the gain also constant, so Vout is linearly change with Vsig.

5 CALCULATE THE DERIVATIVE OF VOUT. THE DERIVATIVE IS ITSELF THE SMALL SIGNAL GAIN. IS THE GAIN LINEAR (INDEPENDENT OF THE INPUT)? WHY?



Yes, it's linear when the transistor is in saturation, The PMOS working as current source with approximately constant current = 100uA , so the nmos transistor is (I to v device) as a constant current equal to 100uA passing through it, vin==VGS of m1 that we calculated before, so as the current is constant and equal to that value, vin is approximately constant which would make gm and gain constant.

And from nodal analysis when Vin is constant with vsig we see :

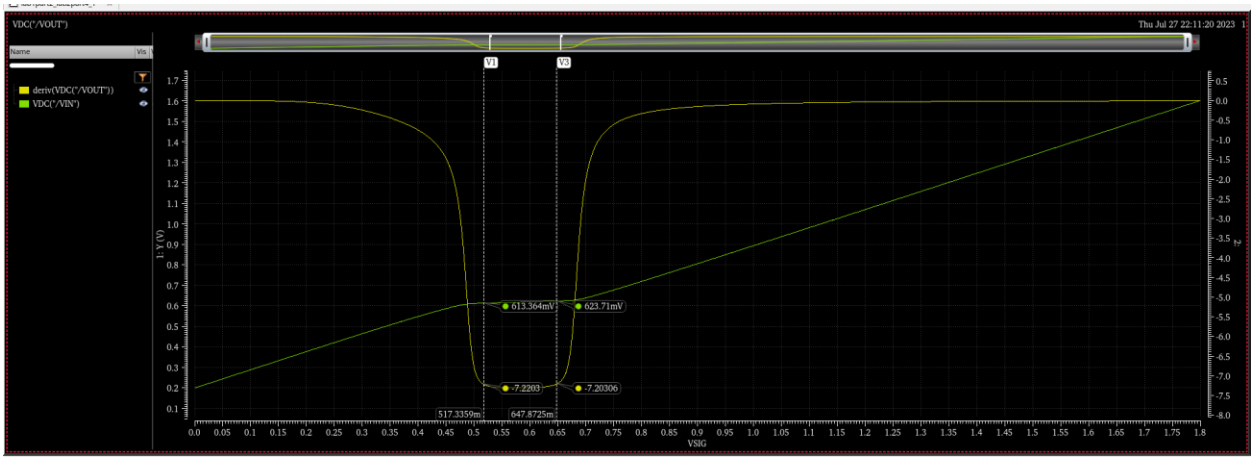
$$\frac{Vsig - Vin}{R1} = \frac{Vin - Vo}{R2}$$

$$vo = 9vin - 8vsig$$

$$\frac{dVo}{dVsig} = \frac{\cancel{dVin}}{\cancel{dVSIG}} - 8\frac{dVsig}{dVsig}$$

$$\frac{dVo}{dVsig} = gain = -8$$

6 WHAT IS VALUE OF VIN IN THE PART WHERE THE GAIN IS LINEAR?



VIN almost constant, just small change From 613.3mv to 623.7 mv which is the the input that will be amplified by the gain

Linear gain is When vsig -> 647.8 mv- 517.3 mv = 130.5 mv **without transition regions.**

7 ANALYTICALLY CALCULATE THE DC INPUT RANGE OVER WHICH THE GAIN IS LINEAR. COMPARE YOUR ANALYSIS WITH THE SIMULATION RESULT

$\frac{VDD-2V*}{|AV|} = \frac{1.8-2*0.225}{8}$ =168mv

Sim	Analytically
130.5 mv	168mv