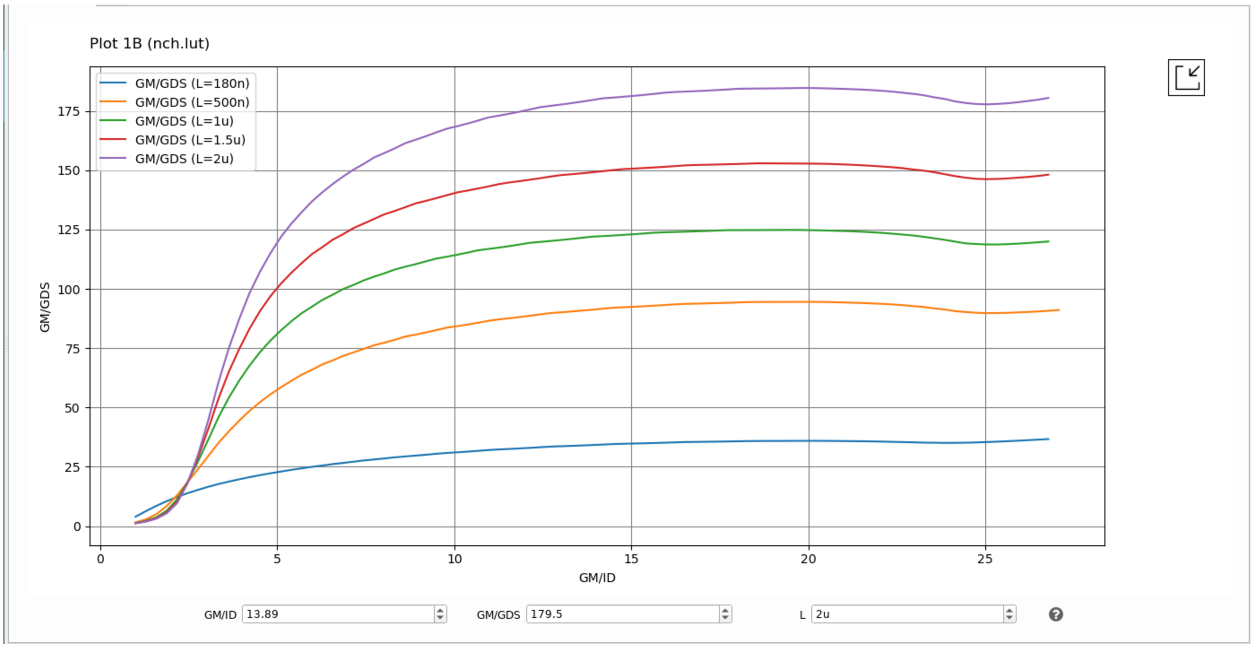
Part1

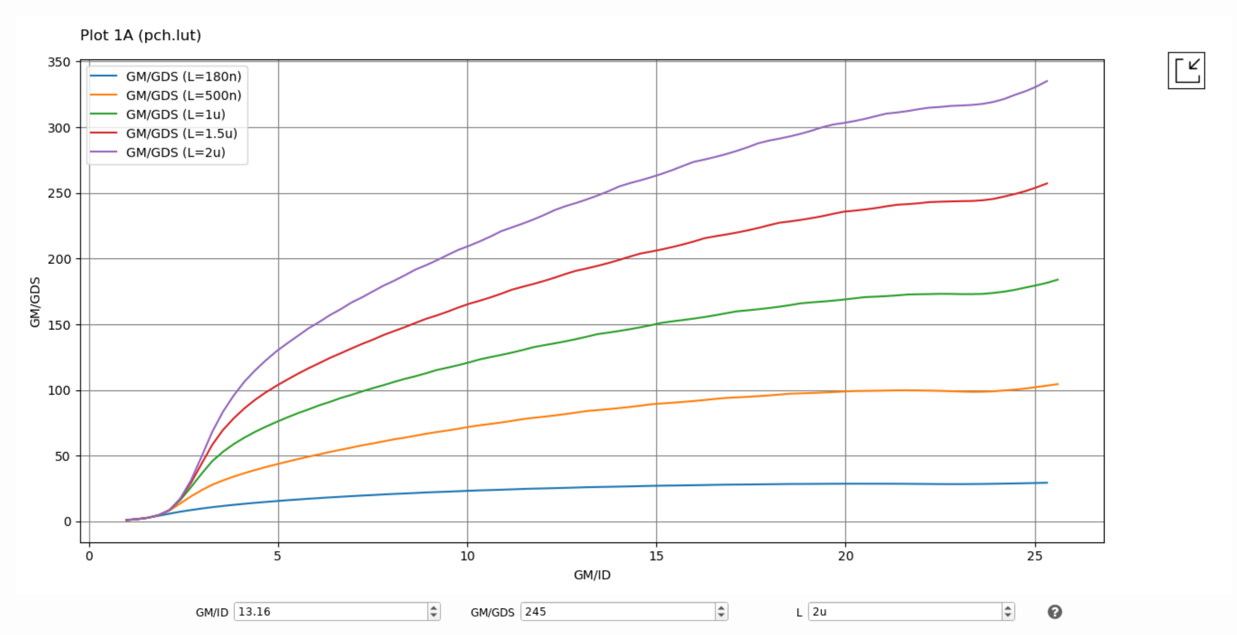
1 Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS = VDD/3 and L = 0.18u,0.5u:0.5u:2u

1.1 gm/gds

NMOS

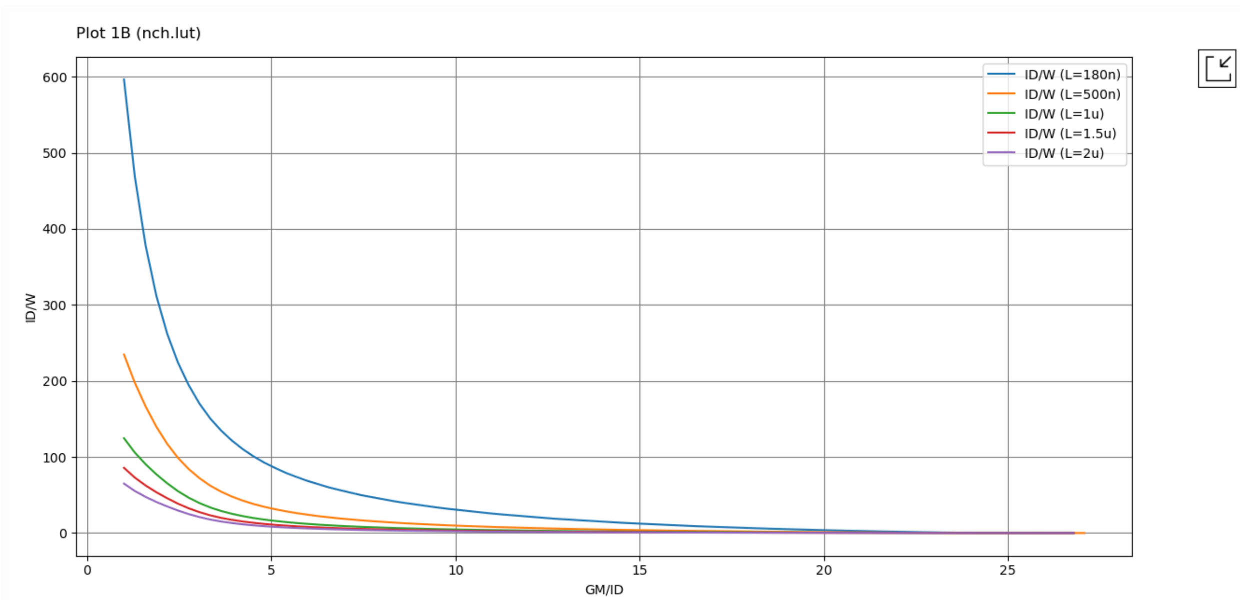


PMOS

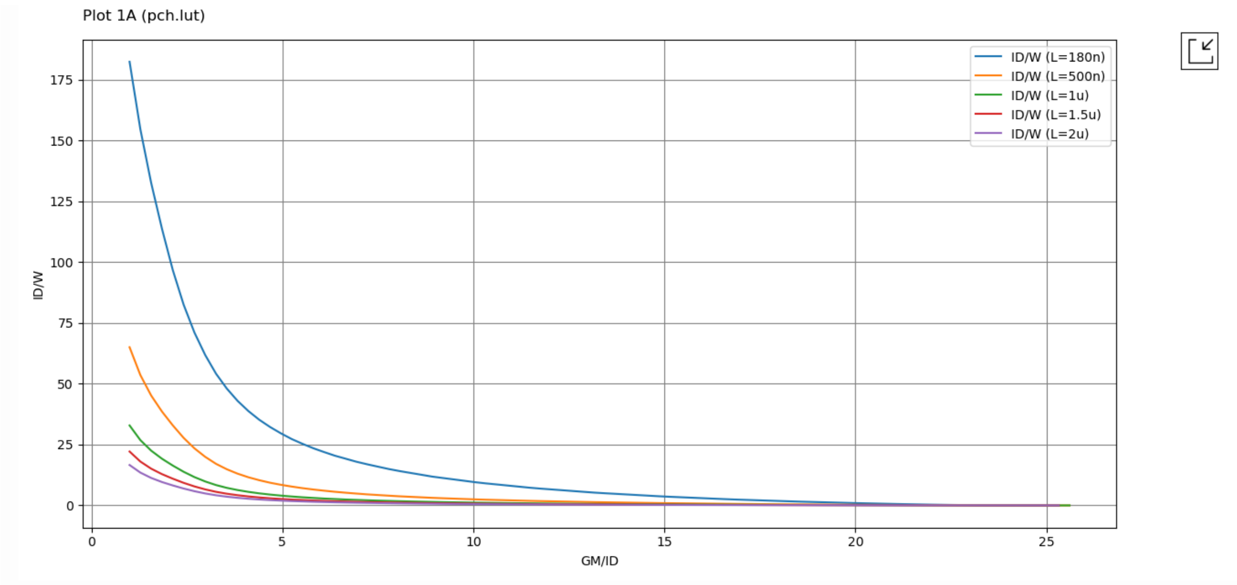


1.2 ID/W

NMOS

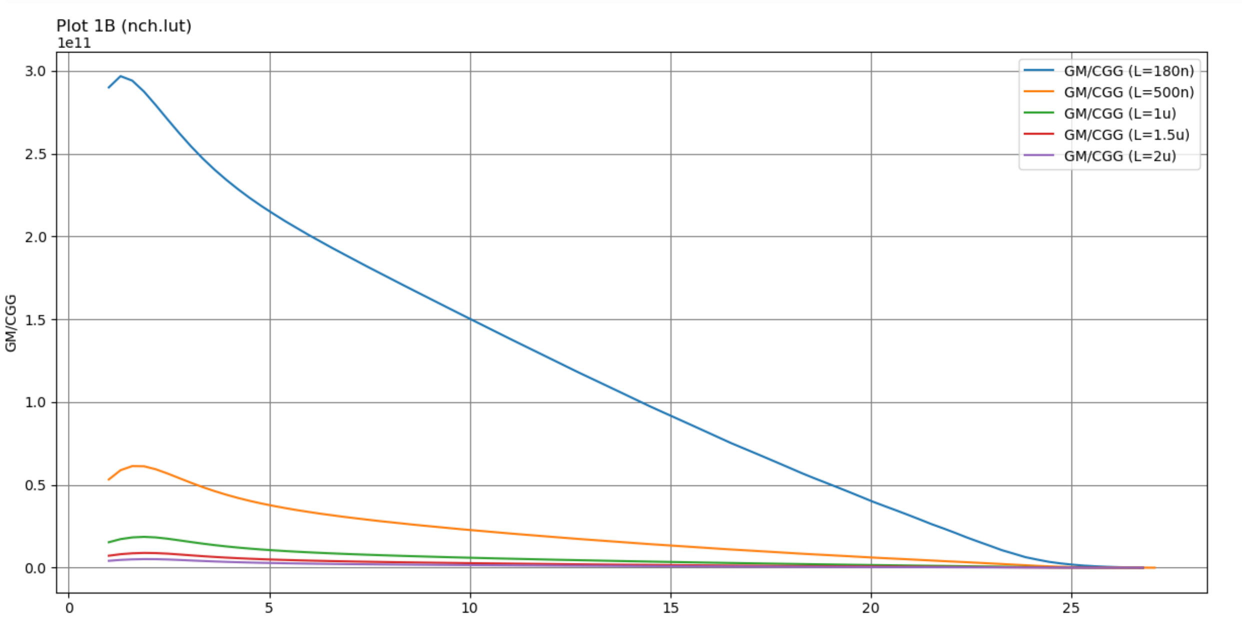


PMOS

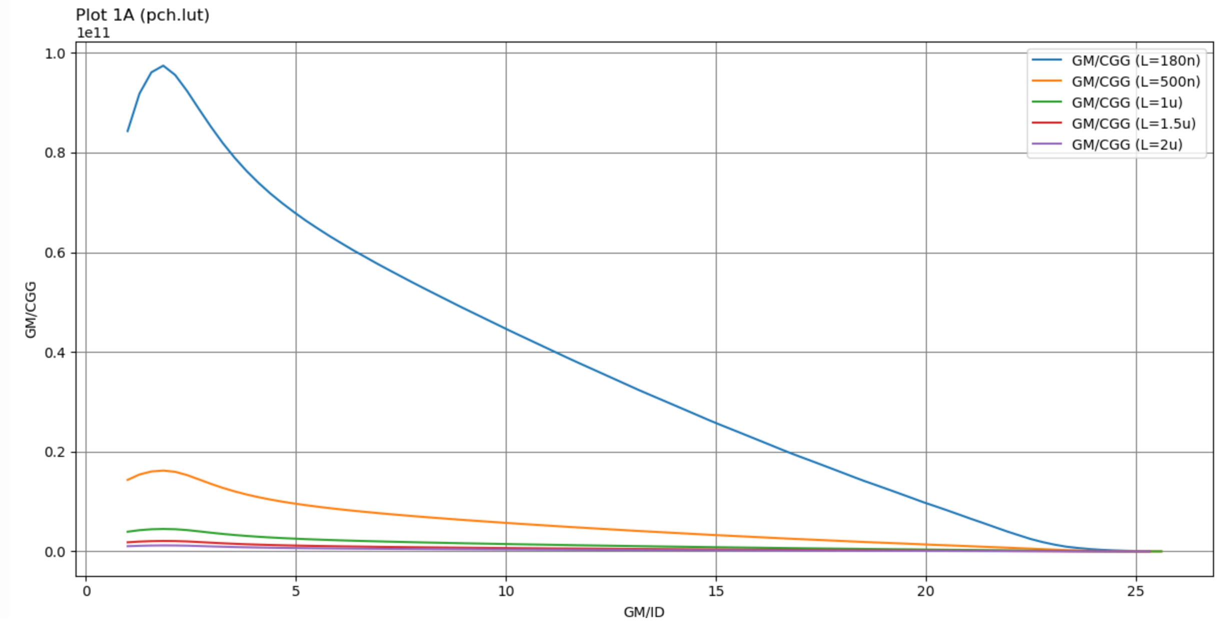


1.3 GM/CGG

NMOS

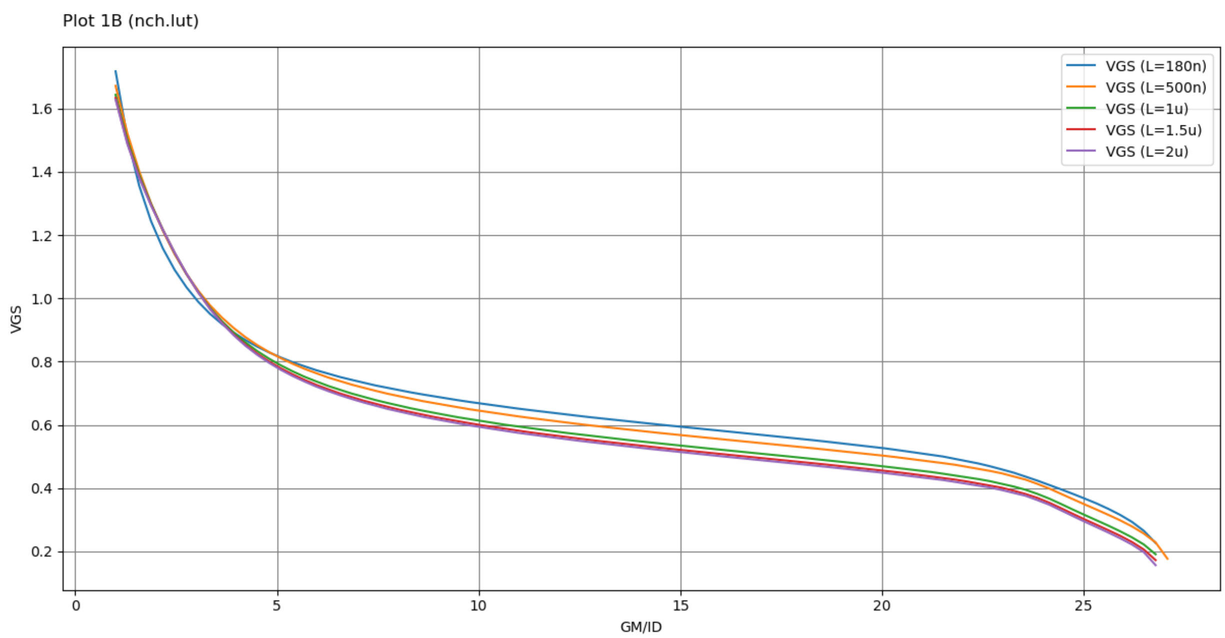


PMOS

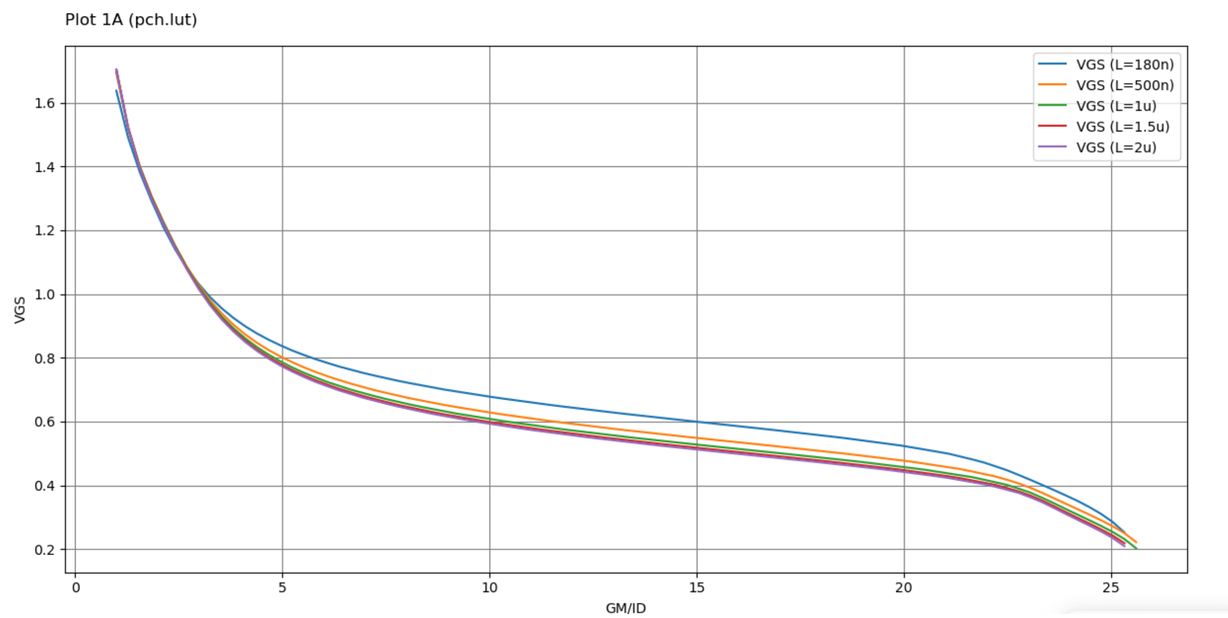


1.4 VGS

Nmos



PMOS

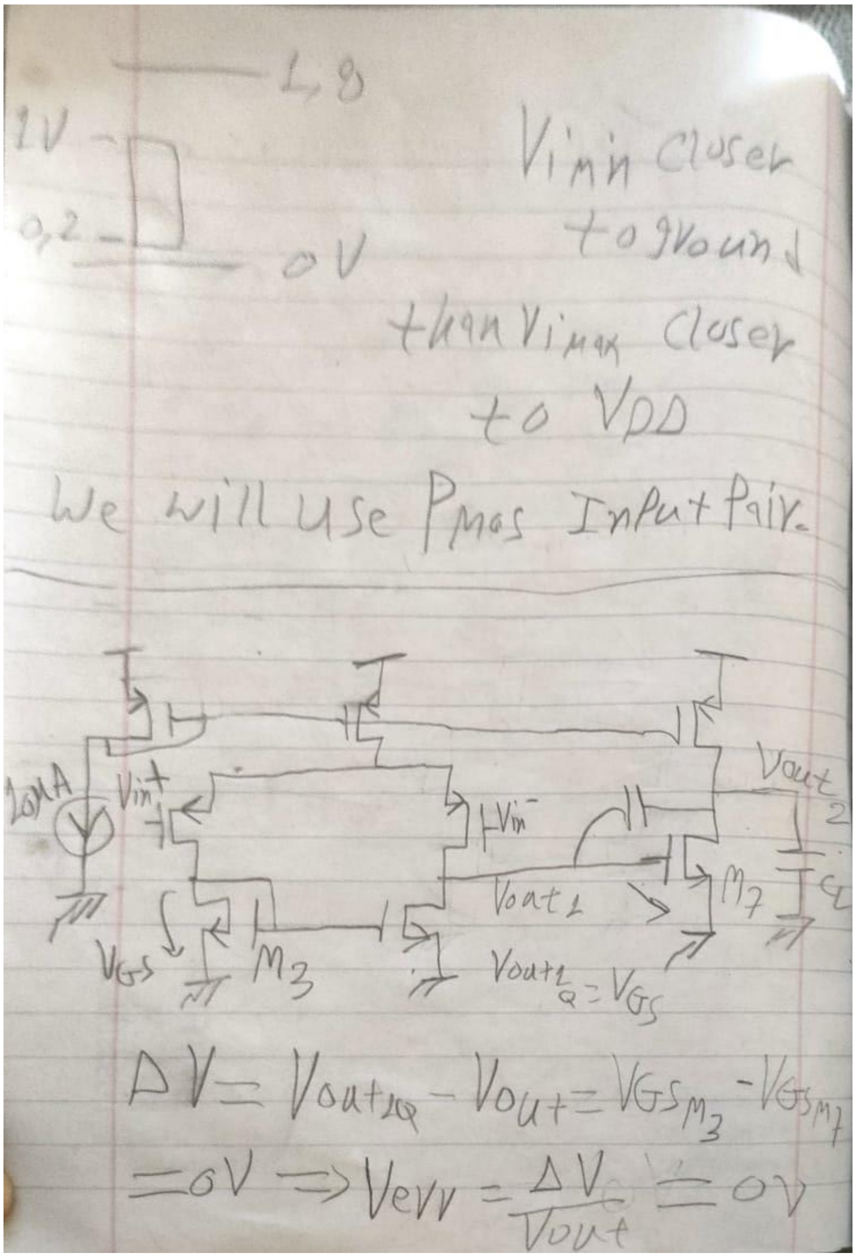


Plot 1A (pch.lut)
VGS (L=180n)
VGS (L=500n)
VGS (L=1u)
VGS (L=1.5u)
VGS (L=2u)
VGS
GM/ID
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
5
10
15
20
25

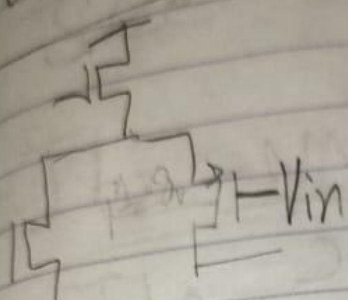
PART2: OTA Design

1 Detailed design procedure and hand analysis. Justify why you used NMOS or PMOS input pair for each stage

1.1 Input pair



To minimize the error we choiced the 2nd stage to be NMOS Input.



We will neglect body effect $V_{bs}=0$

and $\boxed{V_{DS}} = \frac{V_{DD}}{3} = \boxed{0,6V}$

$t_{rise} = 2,2\tau <= 70ns$

$$RC \leq 31,8ns$$

$$\frac{1}{RC} \geq 31,4 \, MRad/s$$

Assuming $CC = \frac{CL}{2} = 2{,}5\,PF$

$\frac{G_M}{CC} \geq 31{,}4M$

$\boxed{G_{M_{I/P}} \geq 78{,}5\,uS}$

$\boxed{G_M = 80}$

$\because$ Slew Rate $= 5$, $I_{b1} = 5 \times 2{,}5 = 12{,}5\,uA$

$\boxed{I_{b2} = 60 - 12{,}5 = 47{,}5u}$

$\boxed{\left(\frac{g_m}{I_D}\right)_{I/P} = \frac{80}{\frac{12{,}5}{2}} = 12{,}8}$

$\frac{actual - Ideal}{Ideal} \times 100 = 0{,}05$

$\frac{1}{A_{OL}} = 5 \times 10^{-4}$

$A_{OL} = 2000 = 66\,db$

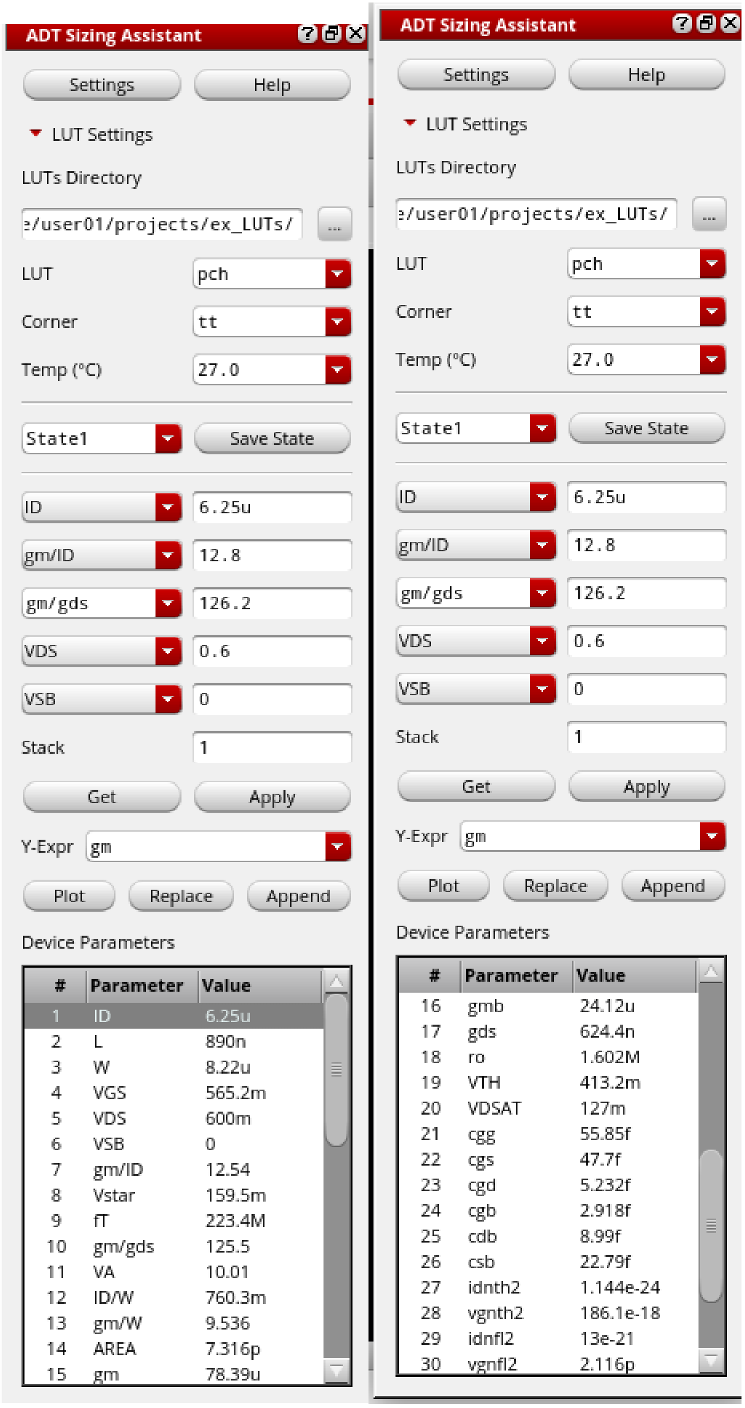
$\therefore A_{OL_{first}} = 36\,db,\ A_{OL_{second}} = 30\,db$

$\frac{g_m V_o}{2} = 63{,}1 \Rightarrow \left.\frac{g_m}{g_{ds}}\right|_{I/P} = 126{,}2$

So for I/P: $I_D = 6{,}25\mu$,

$V_{DS} = 0{,}6,\ V_{GB} = 1{,}2$

$\left(\frac{g_m}{I_D}\right) = 12{,}8,\ \left(\frac{g_m}{g_{ds}}\right) = 126{,}2$


ADT Sizing Assistant
Settings
Help
LUT Settings
LUTs Directory
:/user01/projects/ex_LUTs/
LUT
pch
Corner
tt
Temp (°C)
27.0
State1
Save State
ID
6.25u
gm/ID
12.8
gm/gds
126.2
VDS
0.6
VSB
0
Stack
1
Get
Apply
Y-Expr
gm
Plot
Replace
Append
Device Parameters
Parameter Value
1 ID 6.25u
2 L 890n
3 W 8.22u
4 VGS 565.2m
5 VDS 600m
6 VSB 0
7 gm/ID 12.54
8 Vstar 159.5m
9 fT 223.4M
10 gm/gds 125.5
11 VA 10.01
12 ID/W 760.3m
13 gm/W 9.536
14 AREA 7.316p
15 gm 78.39u
16 gmb 24.12u
17 gds 624.4n
18 ro 1.602M
19 VTH 413.2m
20 VDSAT 127m
21 cgg 55.85f
22 cgs 47.7f
23 cgd 5.232f
24 cgb 2.918f
25 cdb 8.99f
26 csb 22.79f
27 idnth2 1.144e-24
28 vgnth2 186.1e-18
29 idnfl2 13e-21
30 vgnfl2 2.116p

1.2 2ND STAGE INPUT

Second Stage Input — M_8

$$\omega_{P_2} = 4\omega_u \Rightarrow \frac{G_{m_2}}{C_L} = 4\frac{G_{m_1}}{C_C}$$

$$\frac{g_{m_8}}{\cancel{C_C}} = 4 \times \frac{80}{0{,}5\,\cancel{C_L}}$$

$$g_{m_8} = 640\,\mu S$$

2nd Stage gain = 30db = 31,62

$$\frac{g_m}{2 g_{ds}} = 31{,}62 \Rightarrow \left(\frac{g_m}{g_{ds}}\right)_8 = 63{,}24 \simeq 63{,}3$$

$V_{DS} = 0{,}9$, $V_{GB} = 0$, $I_{D_2} = 47{,}5u$


ADT Sizing Assistant
Settings
Help
LUT Settings
LUTs Directory
e/user01/projects/ex_LUTs/
LUT
nch
Corner
tt
Temp (°C)
27.0
State1
Save State
ID
47.5u
gm
640u
gm/gds
63.3
VDS
0.9
VGB
0
Stack
1
Get
Apply
Y-Expr
gm
Plot
Replace
Append
Device Parameters
Parameter Value
1 ID 47.5u
2 L 280n
3 W 4.8u
4 VGS 607.2m
5 VDS 900m
6 VSB 0
7 gm/ID 13.28
8 Vstar 150.6m
9 fT 7.877G
10 gm/gds 61.73
11 VA 4.649
12 ID/W 9.896
13 gm/W 131.4
14 AREA 1.344p
15 gm 630.7u
ADT Sizing Assistant
Settings
Help
LUT Settings
LUTs Directory
e/user01/projects/ex_LUTs/
LUT
nch
Corner
tt
Temp (°C)
27.0
State1
Save State
ID
47.5u
gm
640u
gm/gds
63.3
VDS
0.9
VGB
0
Stack
1
Get
Apply
Y-Expr
gm
Plot
Replace
Append
Device Parameters
Parameter Value
16 gmb 158.8u
17 gds 10.22u
18 ro 97.87k
19 VTH 466.2m
20 VDSAT 114.8m
21 cgg 12.74f
22 cgs 9.828f
23 cgd 2.232f
24 cgb 683.6e-18
25 cdb 5.425f
26 csb 8.313f
27 idnth2 8.838e-24
28 vgnth2 22.22e-18
29 idnfl2 10.08e-18
30 vgnfl2 25.33p

1.3 MIRROR LOAD

For Mirror Load:

We got from S2 :- $V_{GS} = 607{,}2m$
2nd input stage

and gain is same fro 1st stage input, so $\frac{g_m}{g_{ds}} = 126{,}2$

$I_D = 6{,}25$, $V_{DS} = 0{,}6$, $V_{GB} = 0$


ADT Sizing Assistant
Settings
Help
LUT Settings
LUTs Directory
e/user01/projects/ex_LUTs/
LUT
nch
Corner
tt
Temp (°C)
27.0
State1
Save State
ID
6.25u
VGS
607.2m
gm/gds
126.2
VDS
VGS
VGB
0
Stack
1
Get
Apply
Y-Expr
gm
Plot
Replace
Append
Device Parameters
Parameter Value
1 ID 6.241u
2 L 1.22u
3 W 1.63u
4 VGS 607.2m
5 VDS 607.2m
6 VSB 0
7 gm/ID 9.911
8 Vstar 201.8m
9 fT 655.2M
10 gm/gds 125.9
11 VA 12.7
12 ID/W 3.829
13 gm/W 37.95
14 AREA 1.989p
15 gm 61.85u
ADT Sizing Assistant
Settings
Help
LUT Settings
LUTs Directory
e/user01/projects/ex_LUTs/
LUT
nch
Corner
tt
Temp (°C)
27.0
State1
Save State
ID
6.25u
VGS
607.2m
gm/gds
126.2
VDS
VGS
VGB
0
Stack
1
Get
Apply
Y-Expr
gm
Plot
Replace
Append
Device Parameters
Parameter Value
16 gmb 16.85u
17 gds 491.3n
18 ro 2.035M
19 VTH 397.5m
20 VDSAT 157.4m
21 cgg 15.03f
22 cgs 13.42f
23 cgd 747.4e-18
24 cgb 862.7e-18
25 cdb 1.932f
26 csb 5.631f
27 idnth2 875.1e-27
28 vgnth2 228.8e-18
29 idnfl2 43.12e-21
30 vgnfl2 11.27p

1.4 THE TAIL

for the tail:

$\boxed{I = 12{,}5u}$

$C_{mir_{High}} = V_{DD} - V_{GS_{I/D}} - V^*_{Tail}$

$V^*_{Tail_{max}} = 1{,}8 - 1 - 0{,}5652 = 234{,}8\,mV$

⇒ V^* for the Tail current Source is the same for 2nd stage load, so to keep the swing we will take

$V^* = 1{,}8 - 1{,}6 = 0{,}2V$

[299mV)

$C_{MRR} >= 74\,db$, $C_{MRR} = 36 - A_{vcm}$

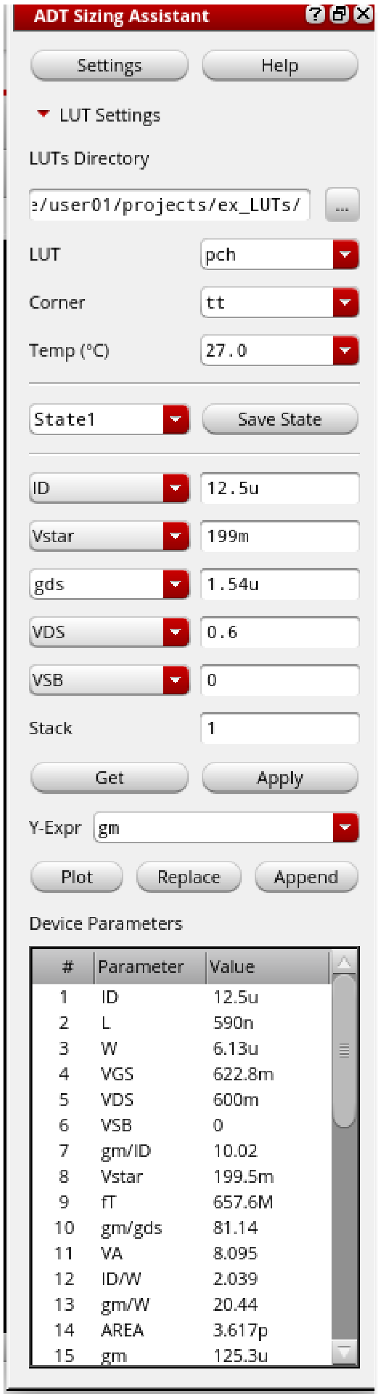
$A_{vcm} =< -38\,db$

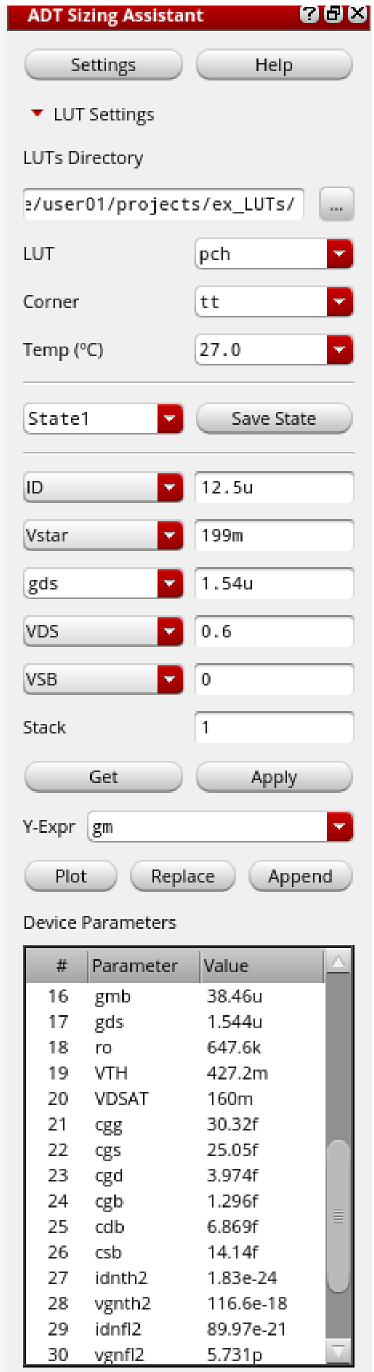
$A_{vcm} =< 0{,}0125$

$$\frac{1}{2\, g_{M_{mirror}}\, r_{o_{tail}}} = 0{,}0125$$

$$\frac{1}{r_{o_{tail}}} = g_{ds} = 1{,}55\,\mu S$$

$V_{DS} = 0{,}6$, $V_{SB} = 0$





1.5 Verify that your gm/ID choices do not violate the CMIR and the peak-to-peak output swing.

Cmir Low-

$C_{mir_{Low}} = -|V_{GS_2}| + |V^*| + V_{GS_3}$

$200m = -701.2m + 160m + V_{GS_{mirror}}$

$\boxed{V_{GS_{max}} = 696.2}$ We didn't Violate the CMRR

V^* 2nd input = 150.6m

So the output Swing low is NOT Violated.

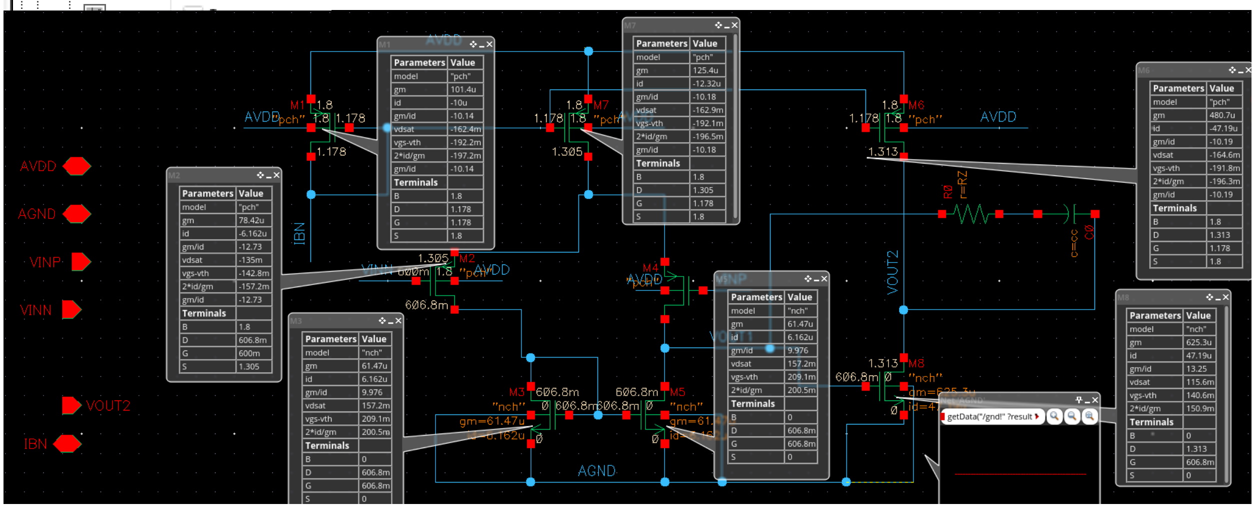
RZ=1/gm2input(from sa) = 1/630.7u

2 A TABLE SHOWING W, L, $gm, ID, gm/ID, vdsat, Vov = VGS - VTH$, AND $V* = 2ID/gm$ OF ALL TRANSISTORS (AS CALCULATED FROM SA).

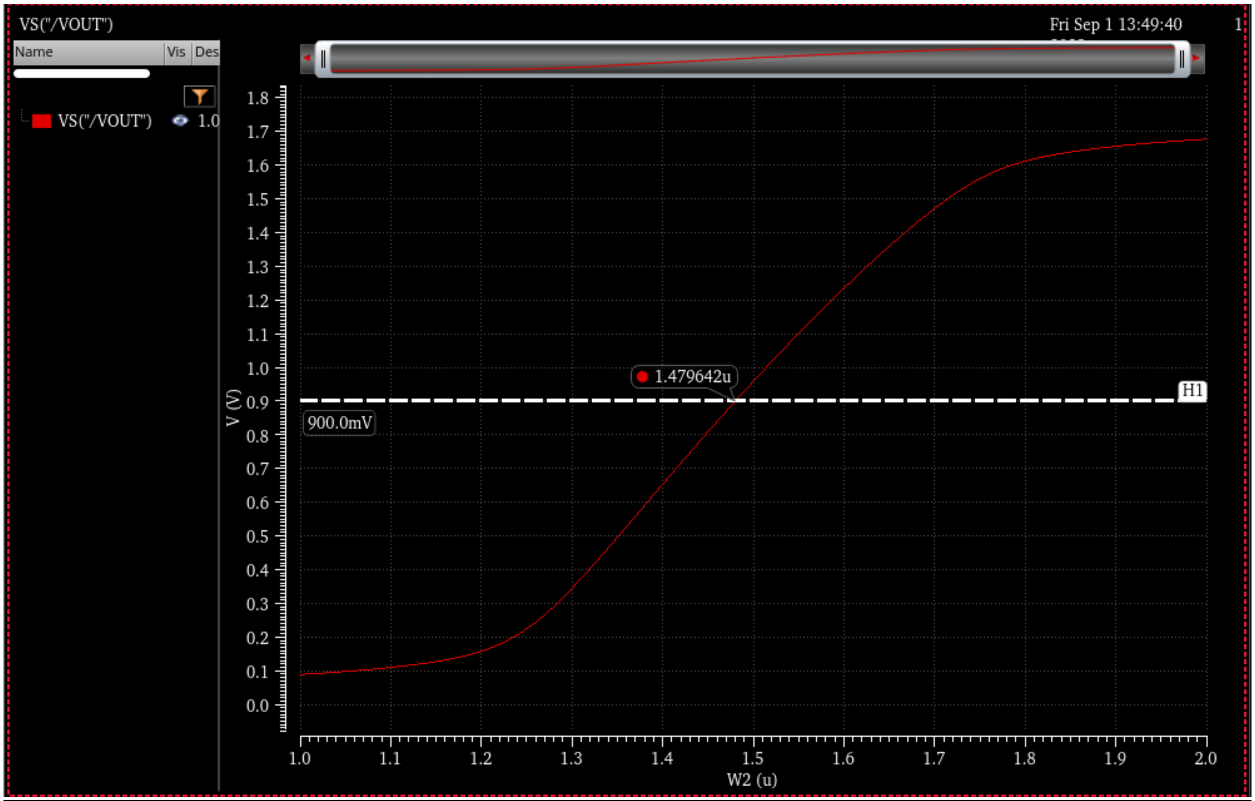
TRANS	W	L	GM	ID	GM/ID	VDSsat	VOV	VSTAR
Input pair	8.22u	890n	78.39u	6.25u	12.54	127m	152m	159.5m
MIRROR LOAD	1.63u	1.22u	61.85u	6.25u	9.911	157.4m	209.7m	201.8m
TAIL CURRENT SOURCE	6.13u	590n	125.3u	12.5u	10.02	160m	195.6m	199.5m
2^{nd} stage input	4.8u	280n	630.7u	47.5u	13.28	114.8m	141m	150.6m

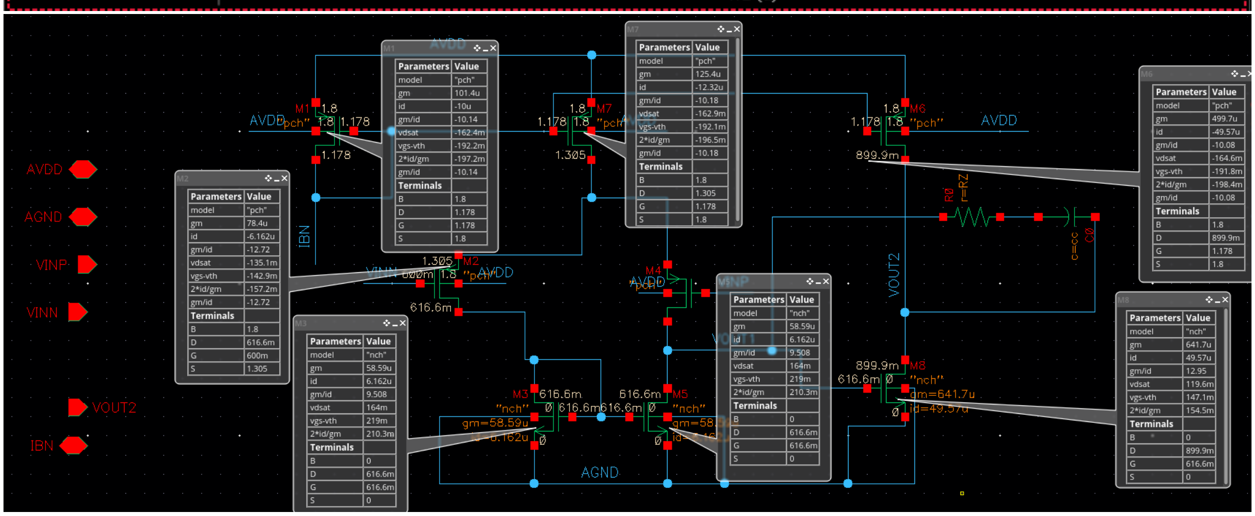
PART 3: Open-Loop OTA Simulation:

CL	5p
L1	890n
L2	1.22u
VICM	0.6
VIC...	0
L3	590n
VID	0
VIDAC	1
W1	8.22u
W2	1.63u
W3	6.13u
L4	280n
W4	4.8u



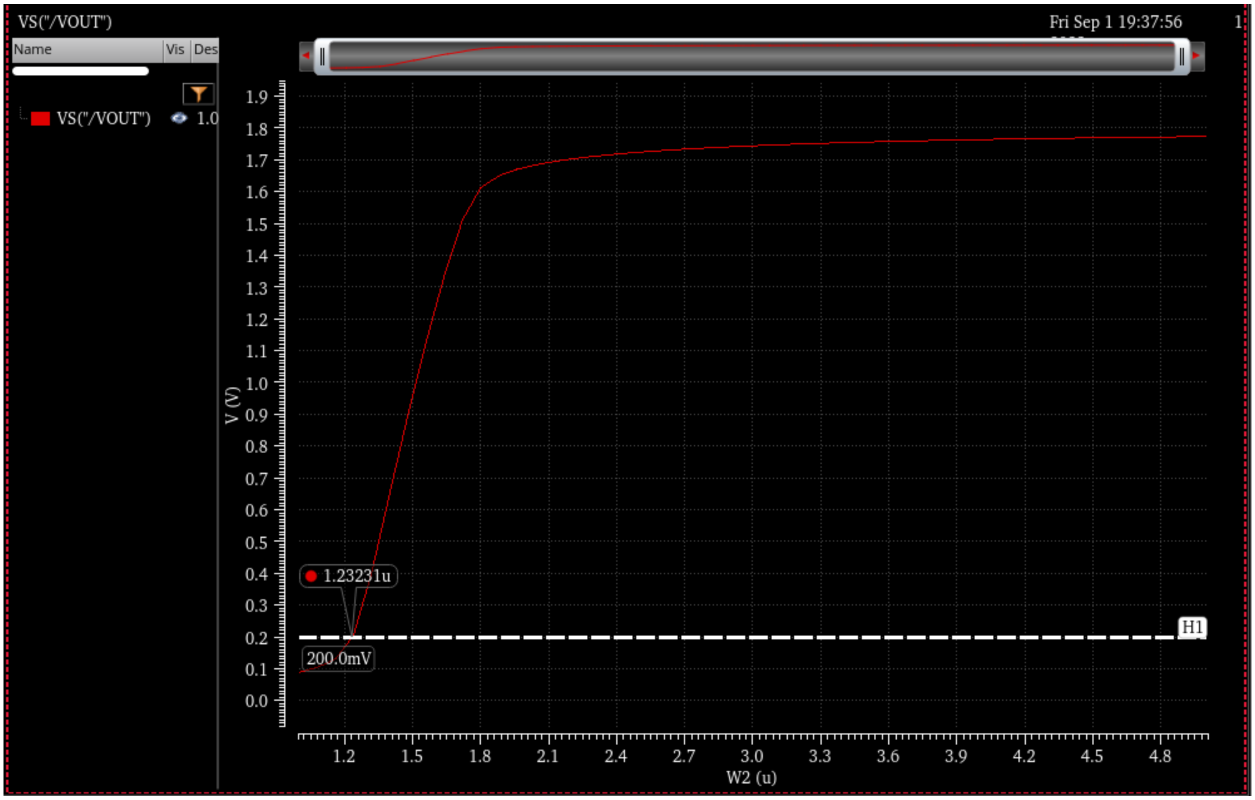
THERE IS schematic offset made vout=1.313, so we swept w(mirror load) to make vout=vdd/2.

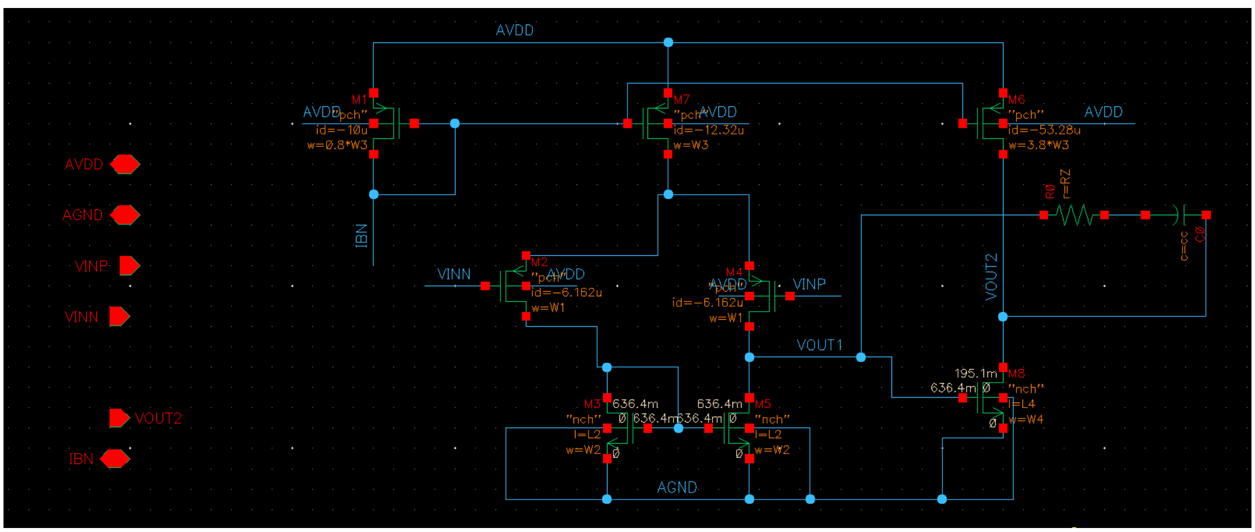




But Current consumption range is violated.

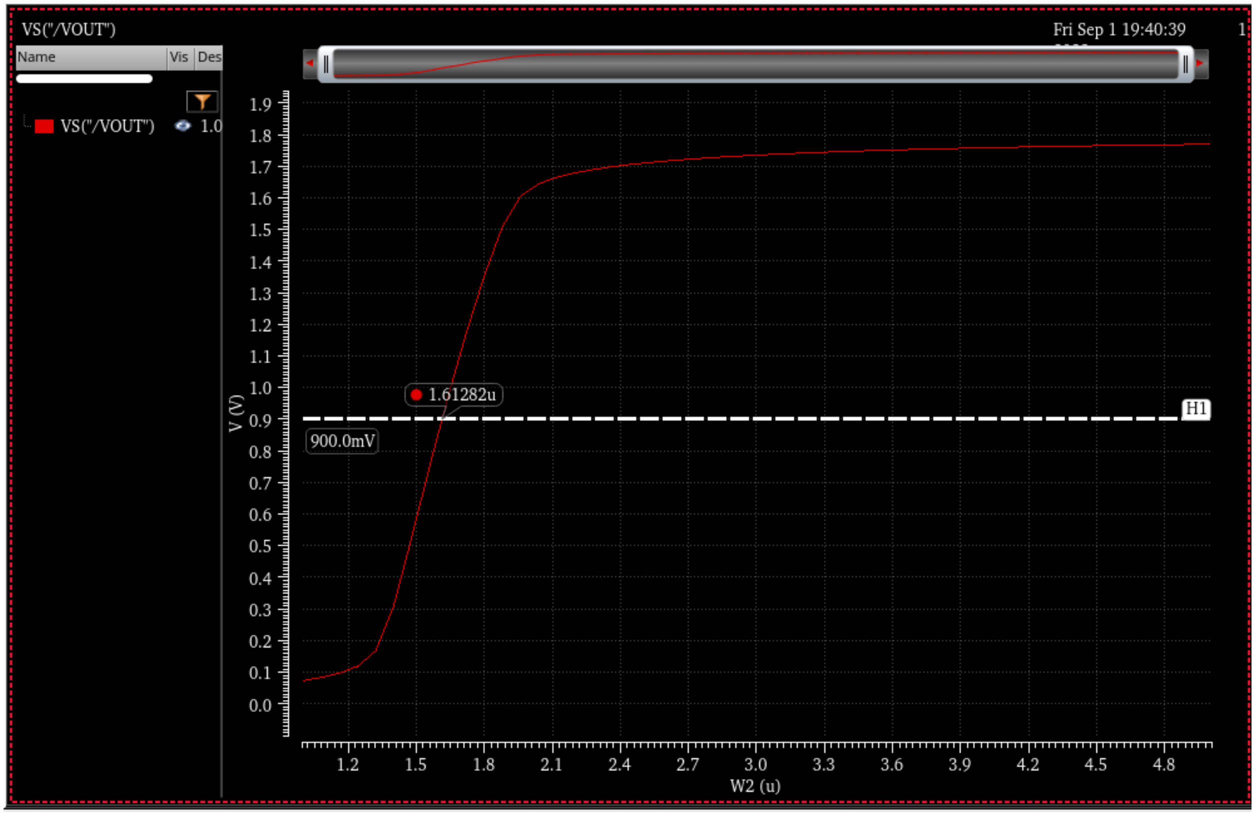
To make sure we don't violate the range we should see the current at the min value 0.2v :

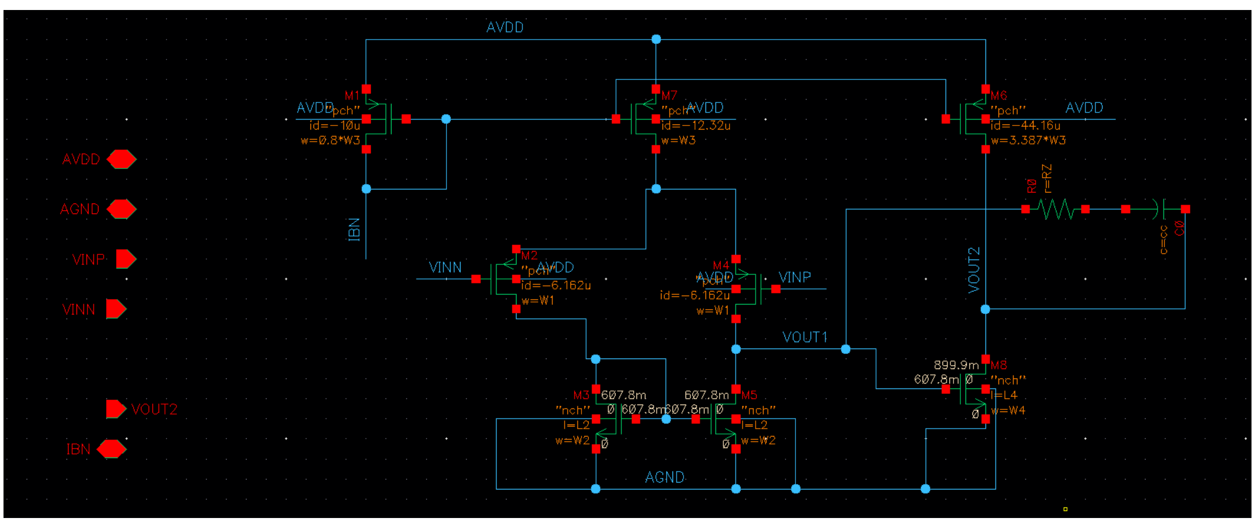




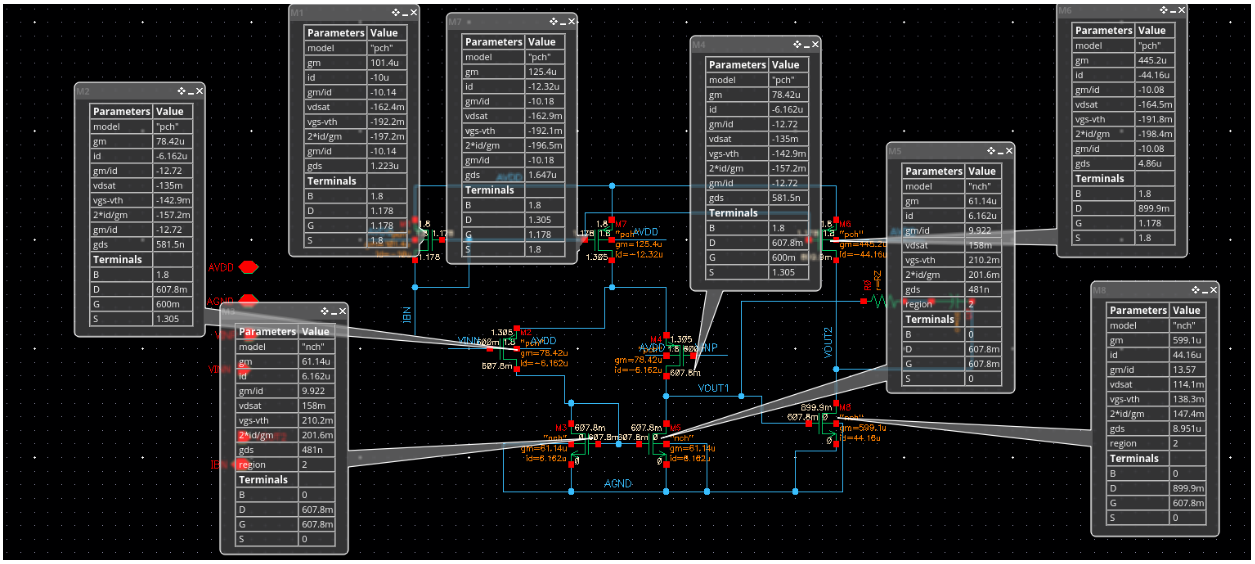
So by doing cross multiplication (under same bias voltage there is a direct relation between width and current):

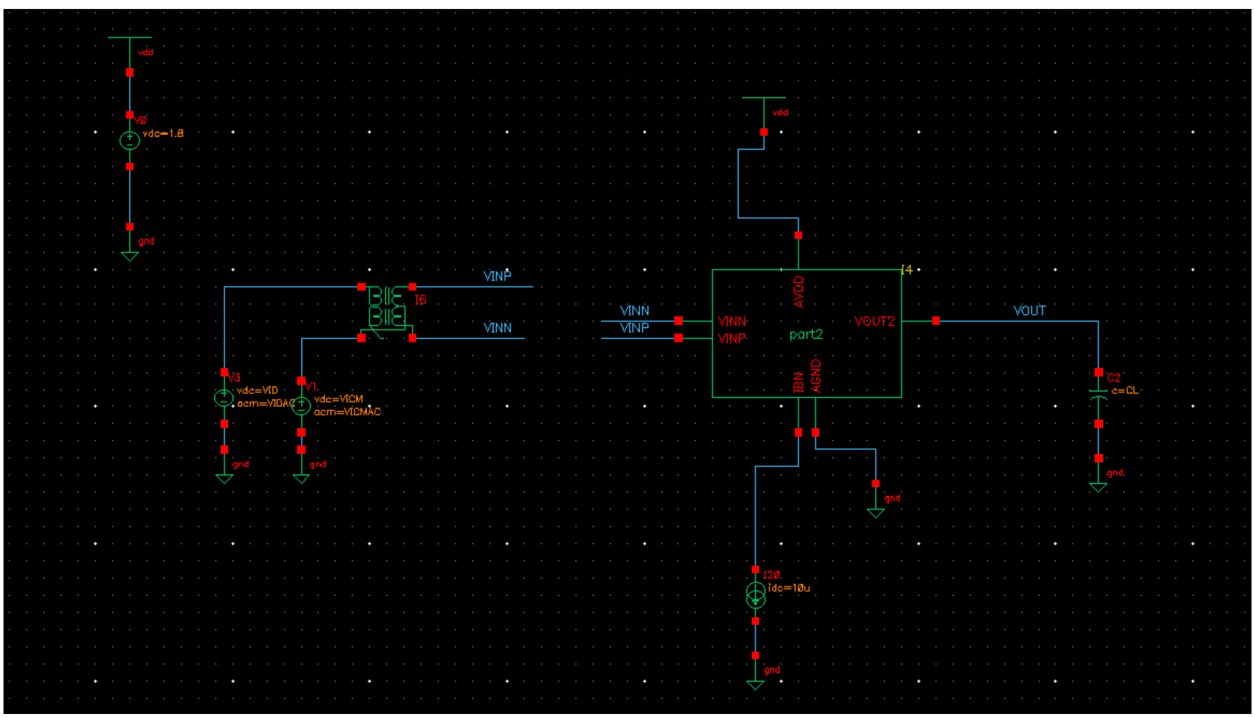
$W6 = \frac{47.5*3.8W3}{53.28}$=3.387W3


VS("/VOUT")
Fri Sep 1 19:40:39
1.61282u
900.0mV
H1
V (V)
W2 (u)


AVDD
AGND
VINP
VINN
VOUT2
IBN
VOUT1

1 Schematic of the OTA and bias circuit with DC node voltages clearly annotated.





1.1 Is the current (and gm) in the input pair exactly equal?

YES, id=6.162u gm=78.42u

1.2 What is DC voltage at the output of the first stage? Why?

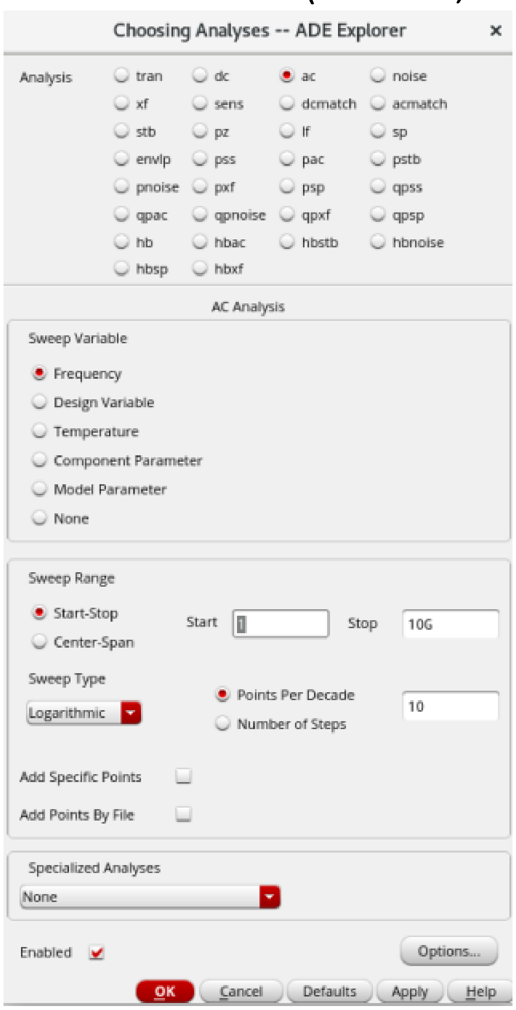
613.3 mv, as VOUT=VGS(M3) and M5 follow M3 and it is diode connected so VGS(0)=VGS(1)=VDS=607.8 mV

1.3 What is DC voltage at the output of the second stage? Why?

VDD/2=0.9, as vgs(m5)=vgs(M8) so there is no schematic offset between the two transistors and as we know $verr = \frac{\Delta Vout}{AV}$ so $\Delta Vout = 0$

2 Diff small signal CCS:

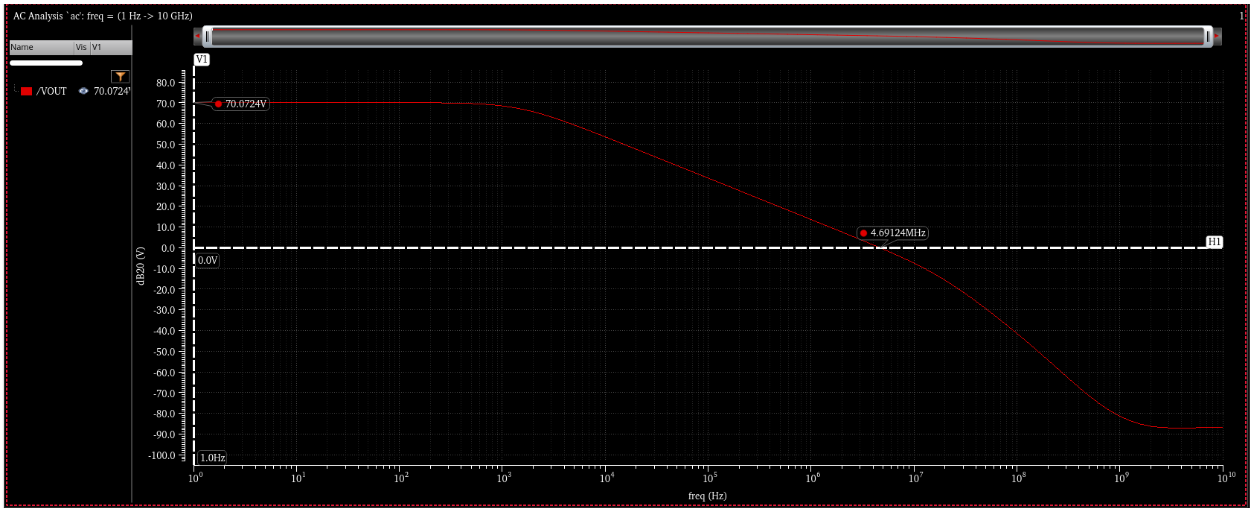
2.1 Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).



2.2 Calculate circuit parameters (Ao, Ao in dB, BW, GBW, UGF)

lab8_part3_1	A0	3.189K			
lab8_part3_1	A0_db	70.07			
lab8_part3_1	BW	1.507K			
lab8_part3_1	fu	4.718M			
lab8_part3_1	GBW	4.805M			

2.3 Plot diff gain (in dB) vs frequency



2.4 Compare simulation results with hand calculations in a table.

$$A_{VD\,1^{st}\,stage} = g_{m_{I/P}} \left[\frac{1}{g_{ds_{I/P}} + g_{ds_{mirror}}} \right]$$

$$= 73{,}8 = \boxed{37{,}36} \text{ db}$$

$$A_{VD\,2nd\,stage} = g_{m(8)} \left[\frac{2}{g_{ds_8} + g_{ds_6}} \right]$$

$$= 43{,}38 = 32{,}74 \text{ db}$$

$$A_{VD\,total} = A_{V\,1st} + A_{V\,2nd} = 70{,}10 \text{ db}$$

$$= 3200\text{K}$$

$$B_{W_1} = \frac{1}{2\pi R_{out1}(GM_2 R_{out2}) C_c}$$

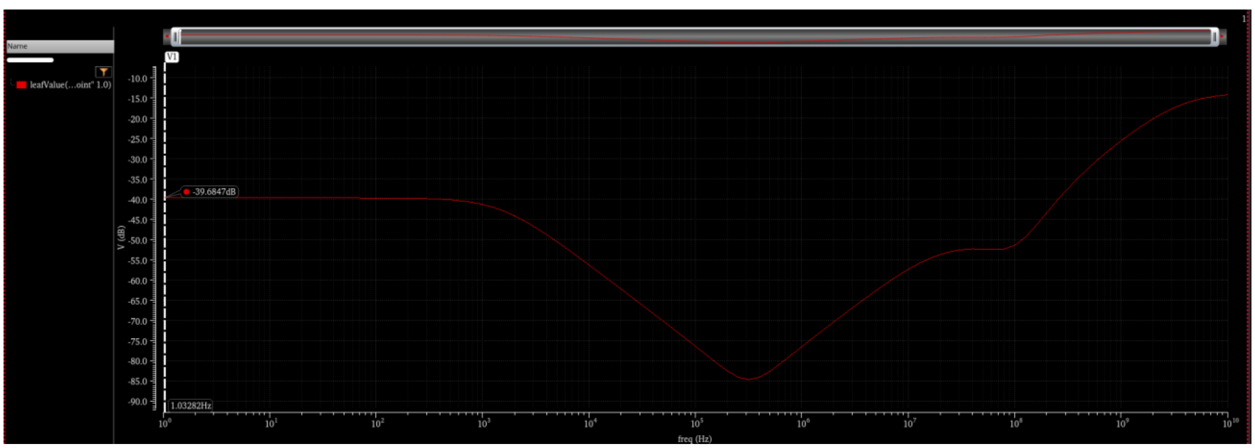
$$= 1559{,}26 \text{ Hz}$$

GBW = UGF = A_{VB} X B_W =

3200 X 1559 = 5.104 M

	Simulated	Analytical
A0	3189	3200
A0_DB	70.07 db	70.10 db
BW	1507	1559
GBW	4.805M	5.104 M
Fu	4.718M	5.104 M

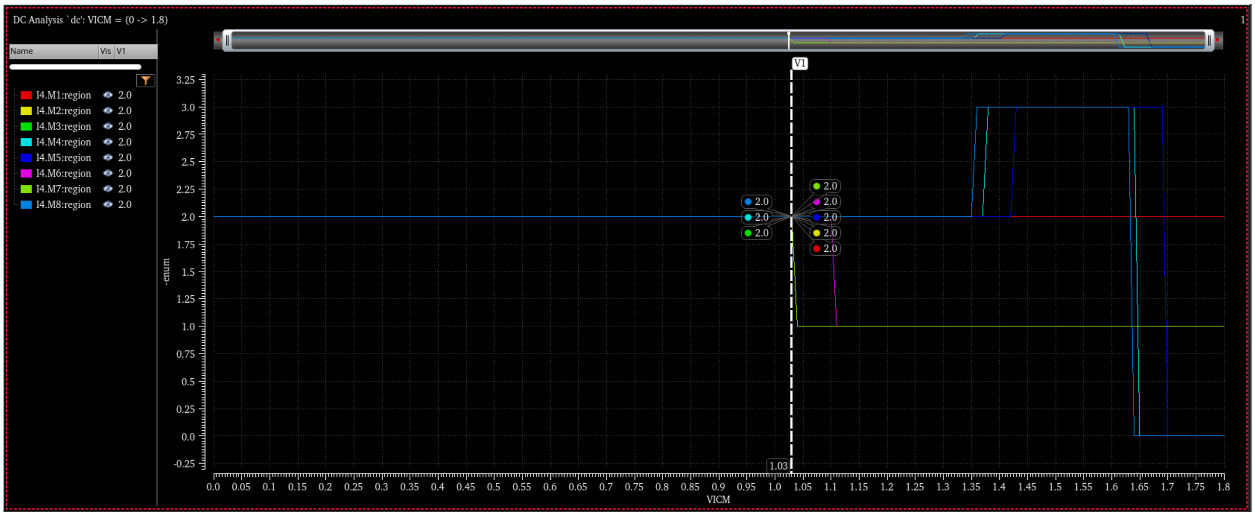
3 CM SMALL SIGNAL CCS:



$$AVcm = \frac{1}{2gm_{mirror} * RSS} = \frac{1}{2 * \frac{gm_{mirror}}{gds_{Tail}}} = 0.0134 = -37.41db$$

	SIMULATOR	ANALYTICAL
AVcm	-39.68 db	-37.41 db

4 CM LARGE SIGNAL CCS (REGION VS VICM):

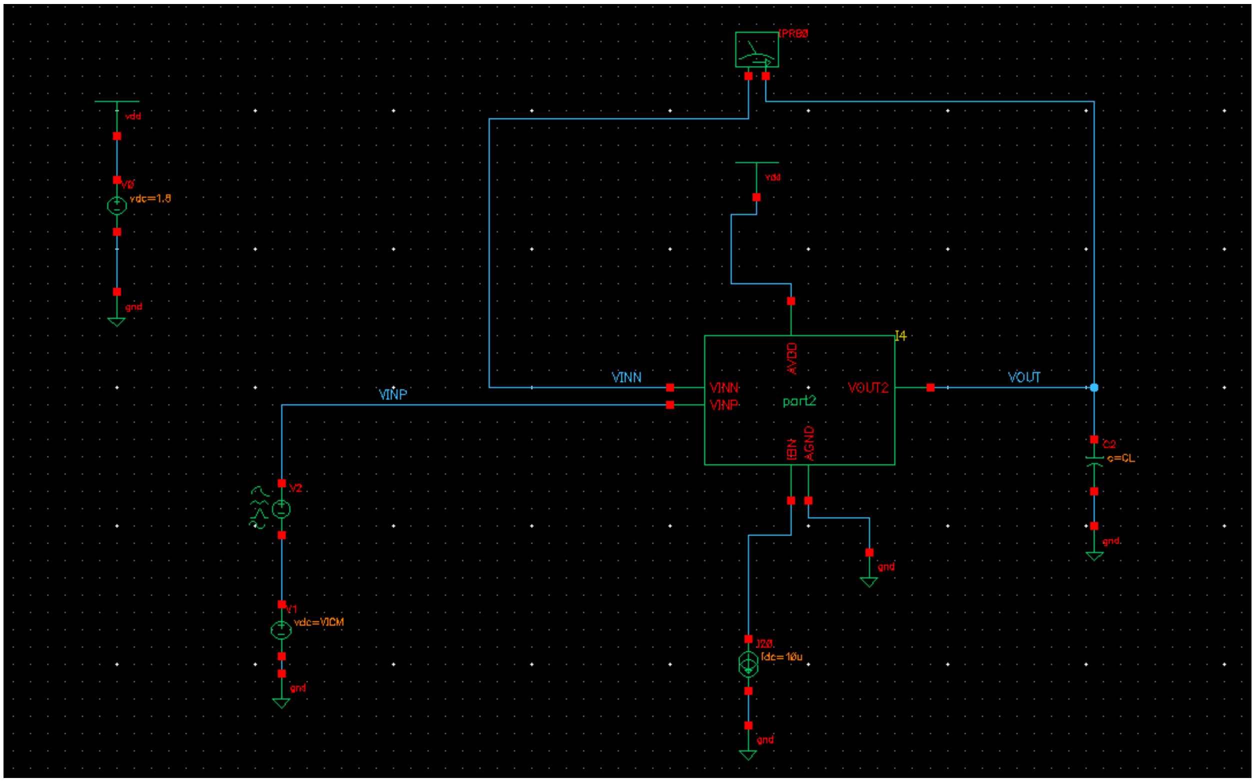


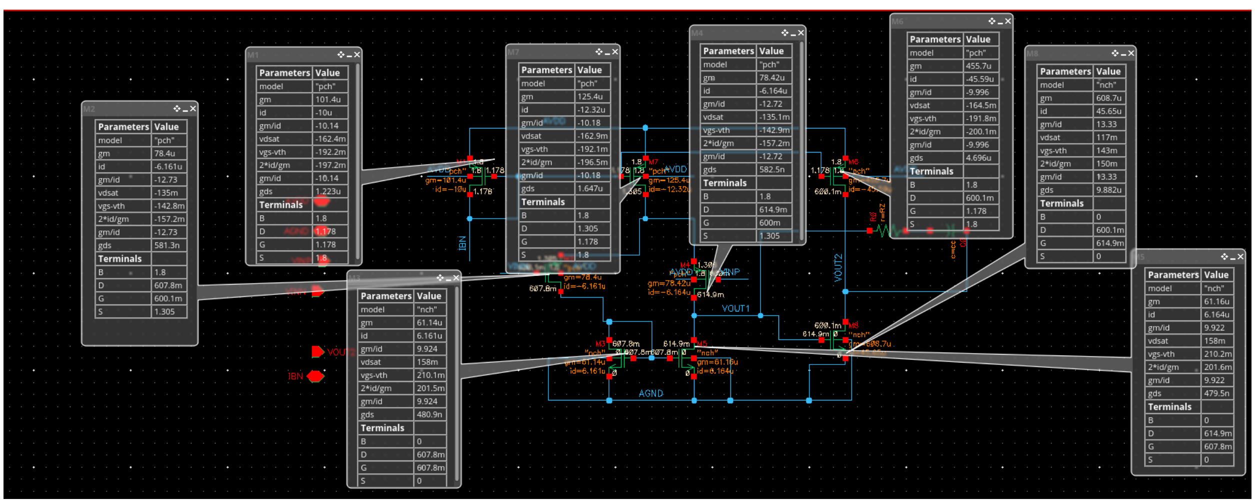
We uses PMOS input pair, body effect caused CMIR to extend till GND.

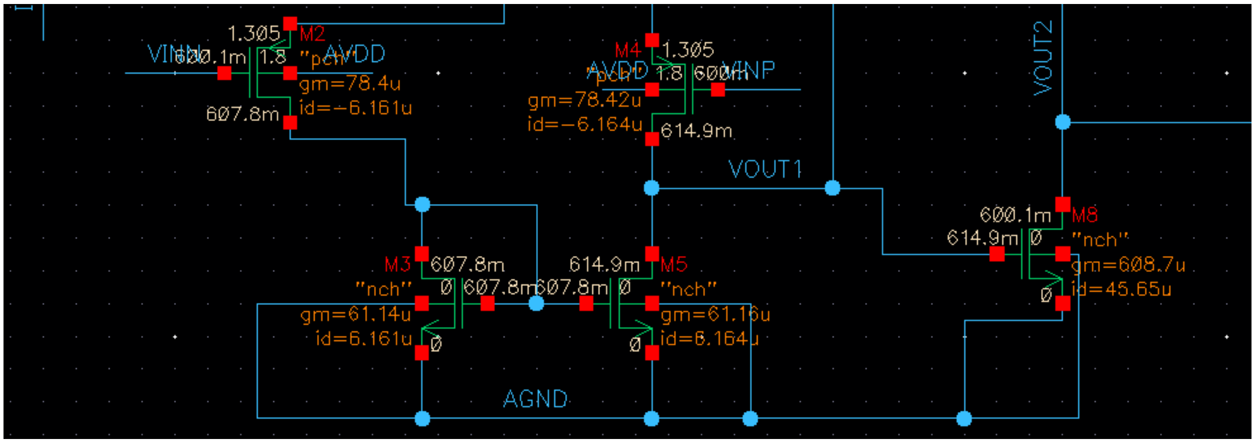
	Sim	Hand analysis
CMIR	1.03-0=1.03	1-0.2=0.8

PART 4: Closed-Loop OTA Simulation

1 Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.







1.1 Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

NO, AS $\frac{\Delta V}{Aol} = \frac{0.9-0.6}{3189} = 0.094mv \sim 1mv$

1.2 Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?

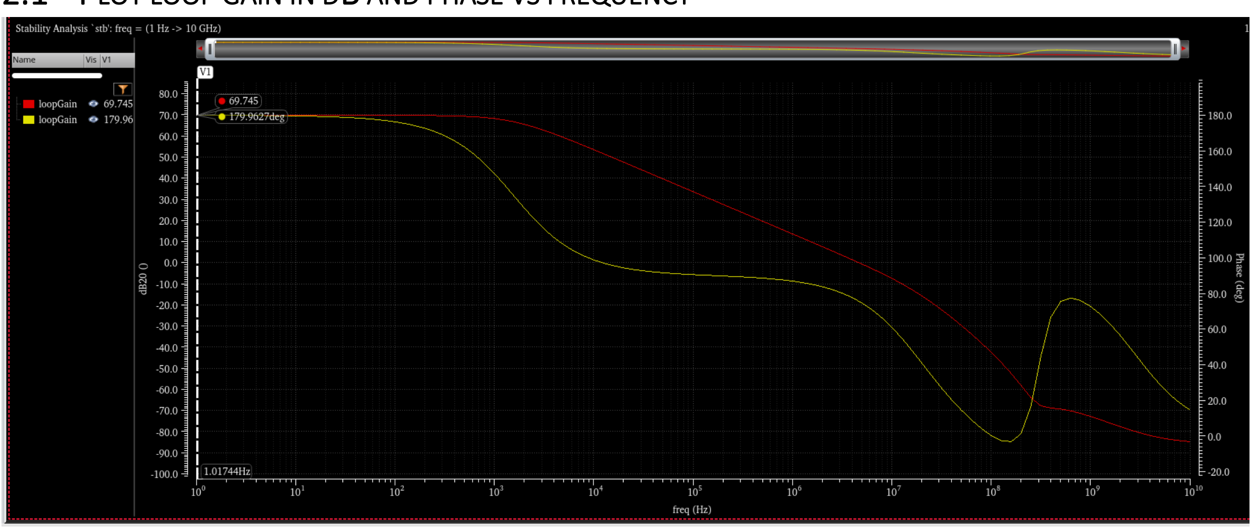
NO, as we made unity buffer feedback, so vout=vin=0.6v not 0.9v.

1.3 Is the current (and gm) in the input pair exactly equal? Why?

No as there is a mismatch between the two inputs, as the output voltage deviates from its CM level and the gain is finite.

2 Loop gain:

2.1 Plot loop gain in dB and phase vs frequency



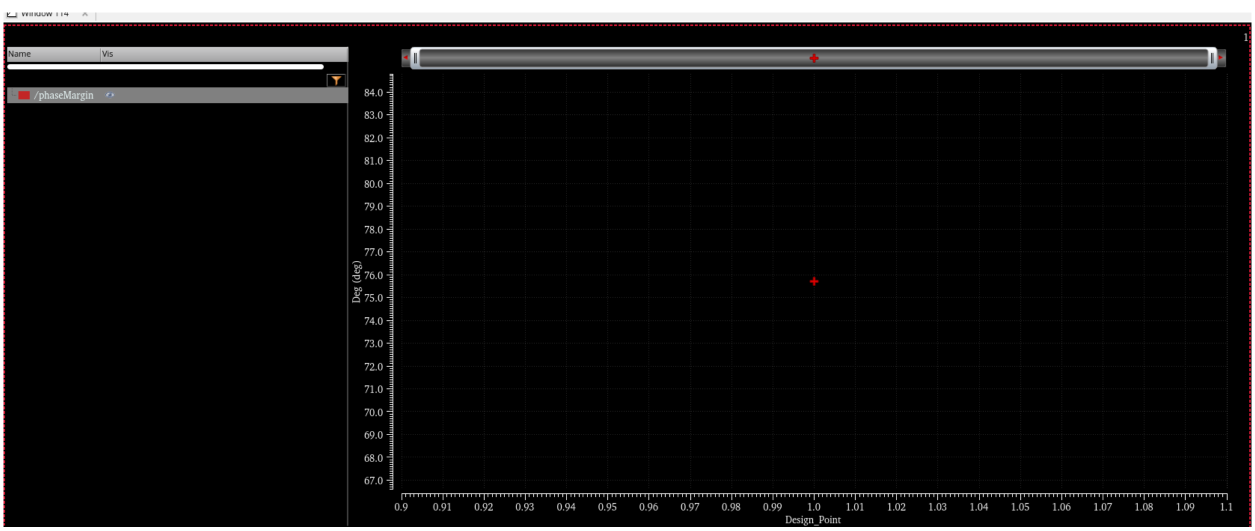
2.2 Compare DC gain, FU, and GBW with those obtained from open-loop simulation. Comment

lab8_part4_1	A	3.071K			
lab8_part4_1	A_DB	69.75			
lab8_part4_1	BW	1.562K			
lab8_part4_1	FU	4.715M			
lab8_part4_1	GBW	4.795M			

	Open loop	Loop gain
A0	3189	3071
A0_DB	70.07 db	69.75 db
BW	1507	1562
GBW	4.805M	4.795 M
Fu	4.718M	4.715 M

The values are too close as expected, as $\beta=1$

2.3 Report PM. Compare with hand calculations. Comment.



Design_Point	getData(...") (deg)
1.000	75.71

Phase margin is too close to the analytical calculation, we made gm of the 2nd stage input is 8 times the gm of input stage and we expected a critical response (PM=76) but some variations happened made the pm a little less.

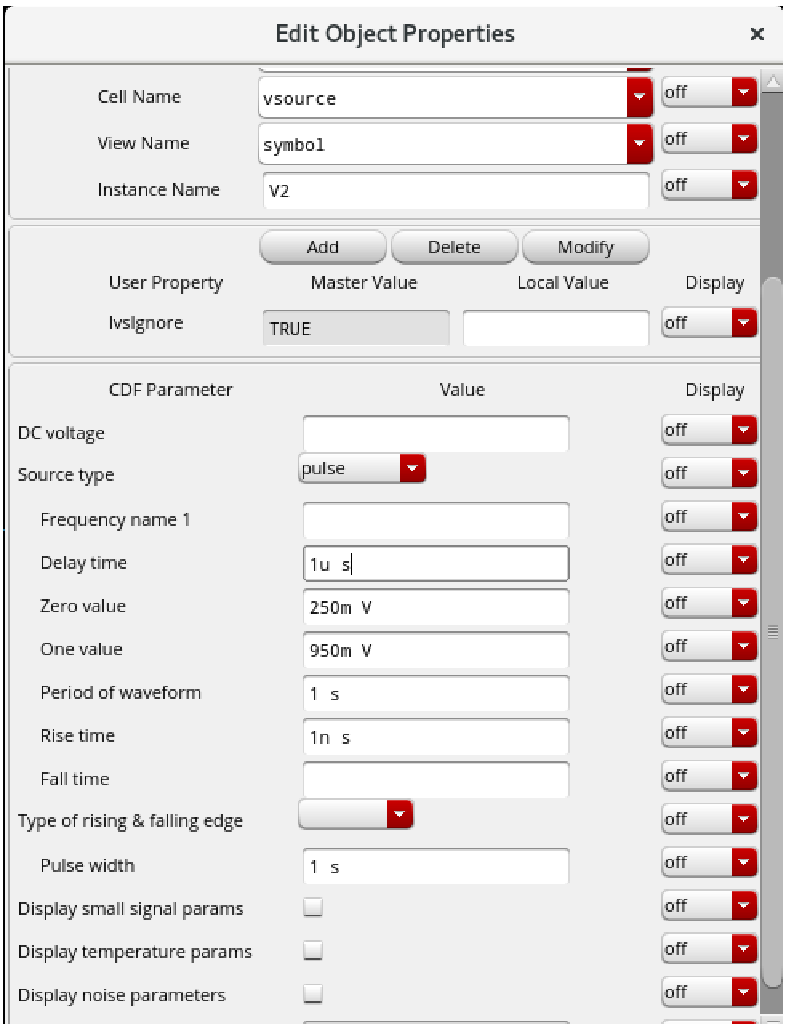
2.4 COMPARE SIMULATION RESULTS WITH HAND CALCULATIONS IN A TABLE.

	Loop gain	Analytical
A0	3071	3200
A0_DB	69.75 db	70.10 db
BW	1562	1559
GBW	4.795 M	5.104 M
Fu	4.715 M	5.104 M

For analytical calculations loopgain=βAol, and β=1 so loopgain=Aol that we calculated above.

3 SLEW RATE:

3.1 APPLY A STEP INPUT WITH THE FOLLOWING PARAMETERS (DELAY = 1US, INITIAL VALUE = CMIR-LOW + 50MV, FINAL VALUE = CMIR-HIGH – 50MV, RISE TIME = 1NS, PERIOD = 1S, WIDTH = 1S). NOTE THAT WE WANT A SINGLE STEP INPUT, WHICH IS WHY WE SELECTED VERY LARGE PERIOD AND WIDTH FOR THE PULSE.



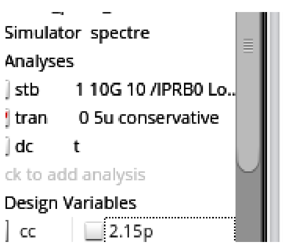
3.2 Report Vin and Vout overlaid

3.3 Report the slew rate.

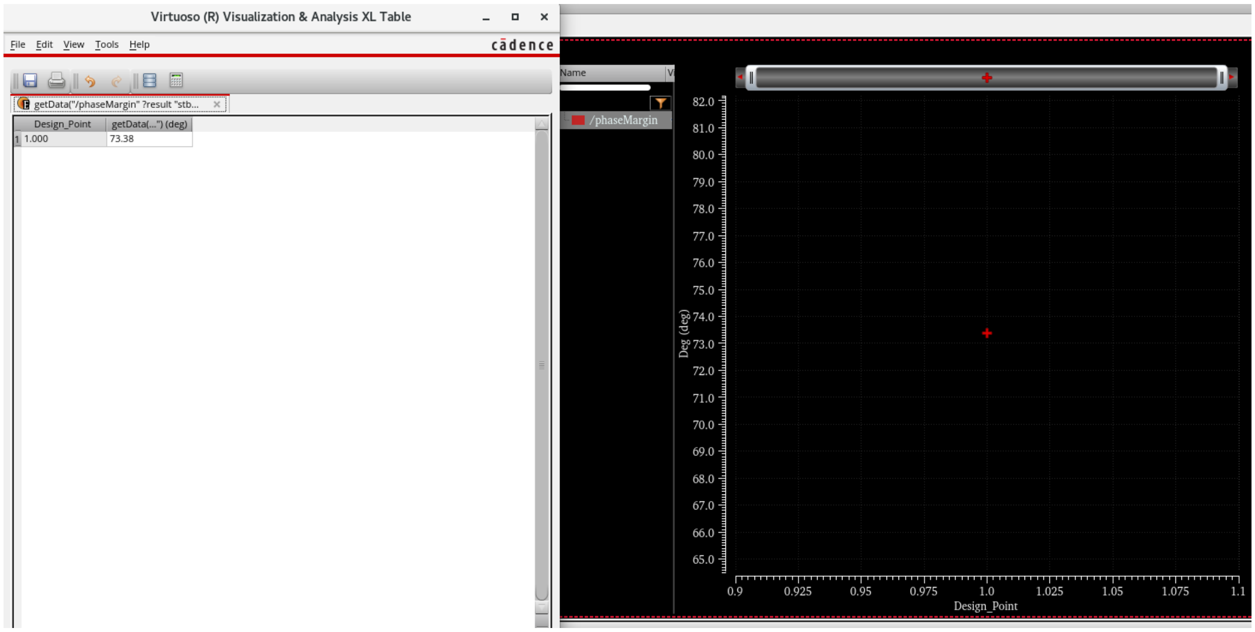
Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
lab8_part4_1	slewRate(VT("/VOUT") 0.25 nil 0.95 nil 10 90 nil "time")	4.409M			

3.4 Compare simulation results with hand calculations in a table

It Is less than the expected value 5 but we can decrease cc to get slew rate >5
But we should make sure the new value of cc doesn't violate the PM specs which is happened successfully.

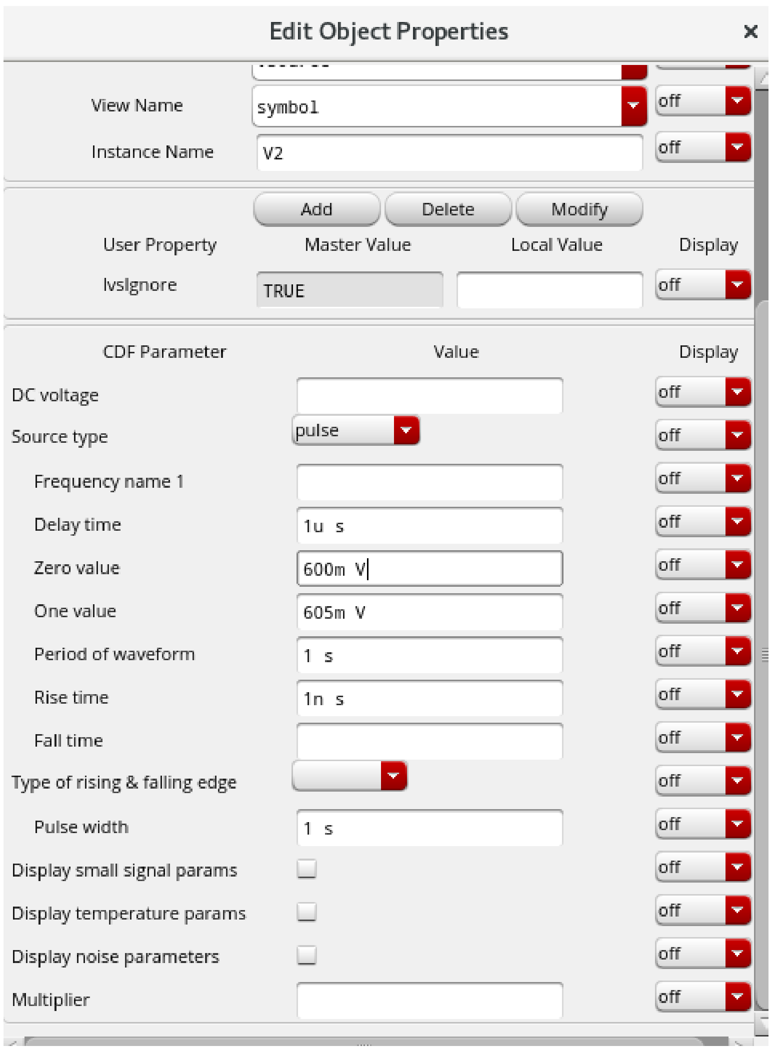


Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
lab8_part4_1	slewRate(VT("/V...	5.07M			

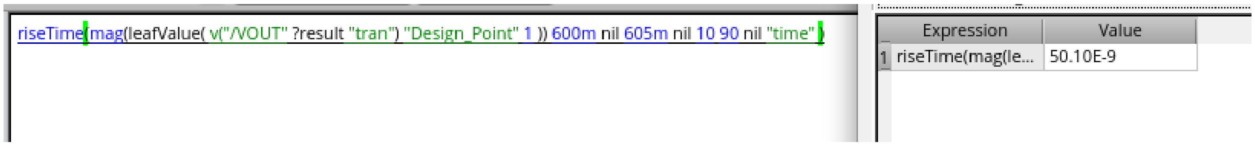


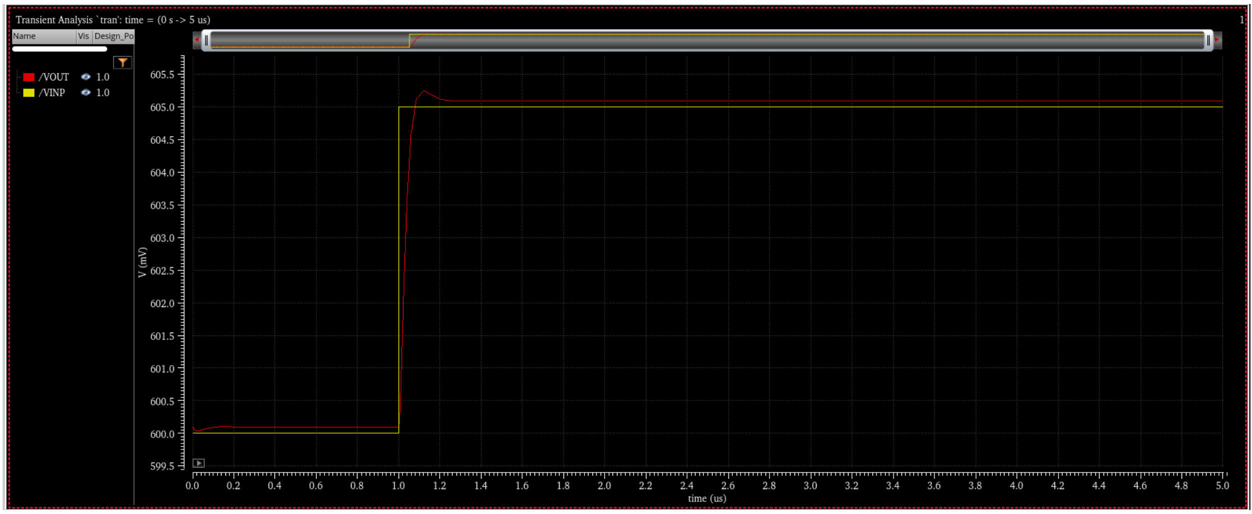
Cc	Sim	Analytical
2.5p	4.41	(12.5/2.5) = 5
2.15p	5.07	(12.5/2.15) = 5.814

4 Apply a small signal step input with the following parameters (delay = 1us, initial value = the middle of the CMIR, final value = the middle of the CMIR + 5mV, rise time = 1ns, period = 1s, width = 1s). Note that we want a single step input, which is why we selected very large period and width for the pulse. Note that we apply a small signal pulse (5mV step) to measure the small signal settling time.



4.1 CALCULATE THE OUTPUT RISE TIME FROM SIMULATION.



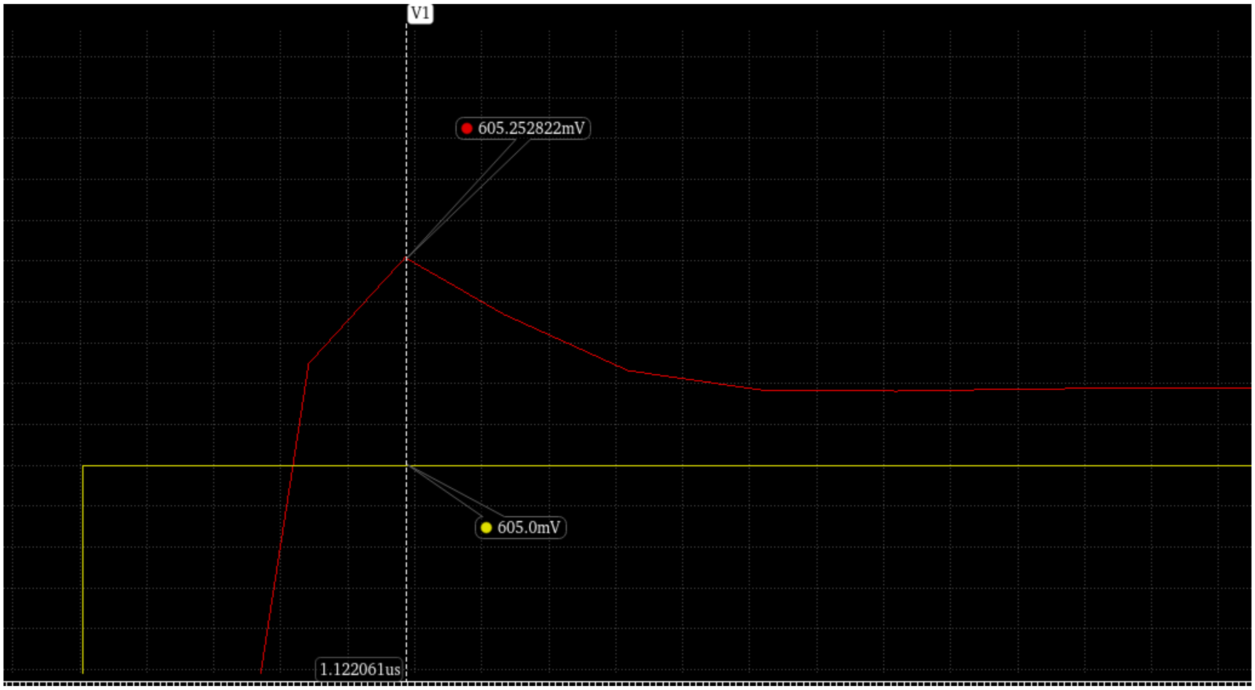


4.2 COMPARE SIMULATION RESULTS WITH HAND CALCULATIONS IN A TABLE

HAND CALCULATION	Simulation
$\frac{2.2}{2\pi * UGF(in\ hz)} = \frac{2.2}{2\pi * 5.104 * 10^6} = 68.6n$	50.1n

As written in the hint, using trise = 2.2τ is based on first-order model, and first-order model is an approximation to the overdamping system which is too slow, but as we showed above the phase margin is 75.7 which is second order under damping system which is too close to critical damping.

4.3 DO YOU SEE ANY RINGING? WHY?



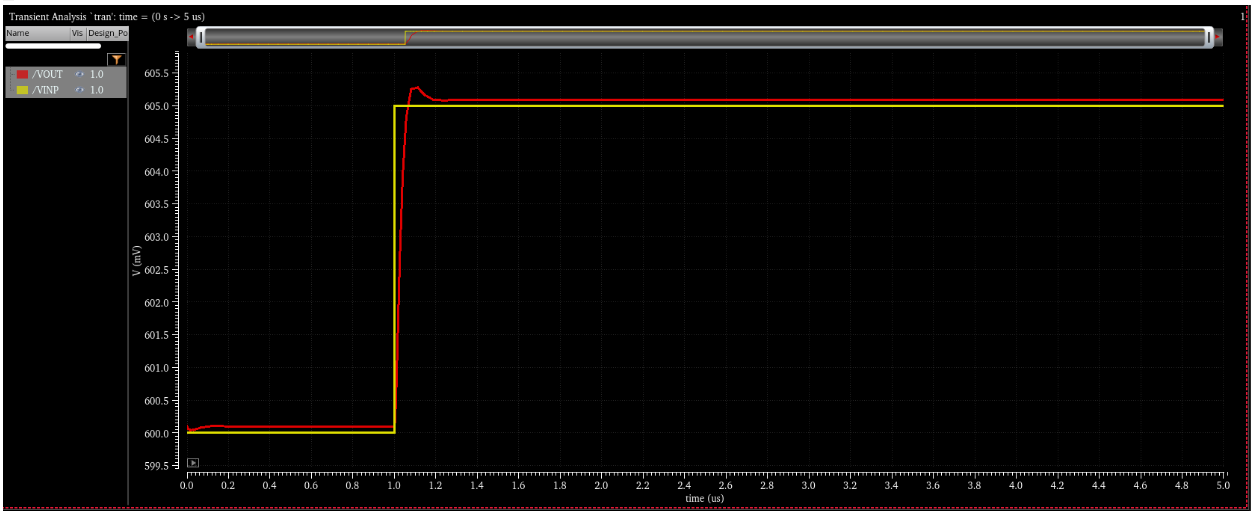
yes, there is an over shoot as the phase margin is 75.7 which is second order underdamped system, and if we increased the PM to be more 76 (critical) we wouldn’t see any, and there is also no oscillations as PM is not too small.

If we used the new cc=2.15p :

lab8_part4_1	A0	3.071K				
lab8_part4_1	A0_DB	69.75				
lab8_part4_1	BW	1.819K				
lab8_part4_1	FU	5.432M				
lab8_part4_1	GBW	5.585M				
lab8_part4_1	/phaseMargin_stb_margin	73.6				

lab8_part4_1	slewRate(VT("/V...	5.07M			

	Expression	Value
1	riseTime(leafVal...	43.62E-9



[Trise (analytical)= $\frac{2.2}{2\pi * UGF(in\ hz)} = \frac{2.2}{2\pi * 5.432*10^{6}} = 64.46\text{ns}$]

ALL THE SPECS ARE NOT VIOLATED