NOTE: THIS REPORT HAS BEEN DONE BASEED ON V3 VERSION, AS IT WAS TOO LATE TO CHANGE EVERYTHING.

PART 1: Sizing Chart

1 THE % CHANGE IN CURRENT TRANSLATES TO A SPEC ON THE $\lambda = 1/VA$ OF THE DEVICE. HOW MUCH IS THE REQUIRED λ?

$$\Delta I_D = \lambda \, \Delta V_{ds}$$

$$\frac{\Delta I_D}{\Delta V_{ds}} = \lambda = 0.1$$

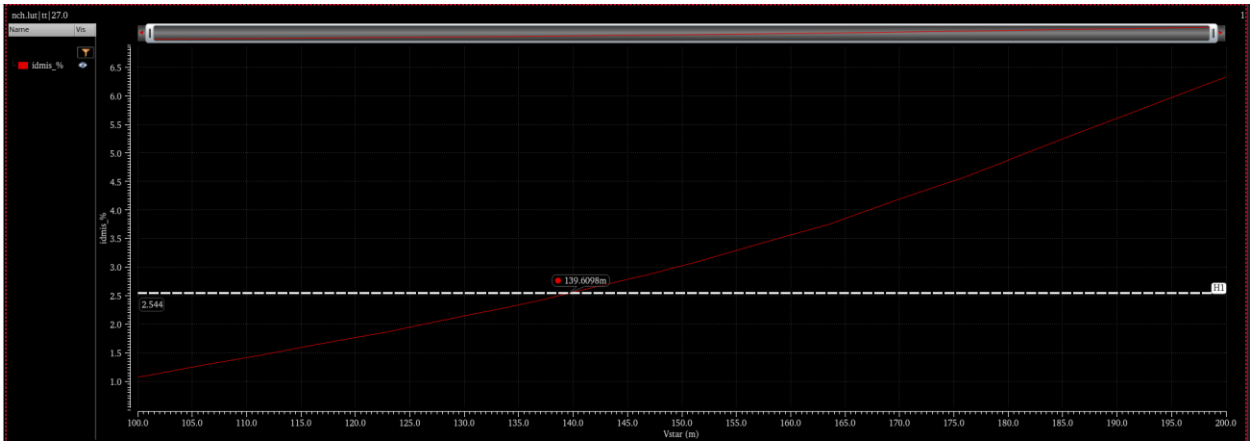
2 SINKING CURRENT MEANS WHICH DEVICE TYPE? NMOS OR PMOS?

NMOS

3

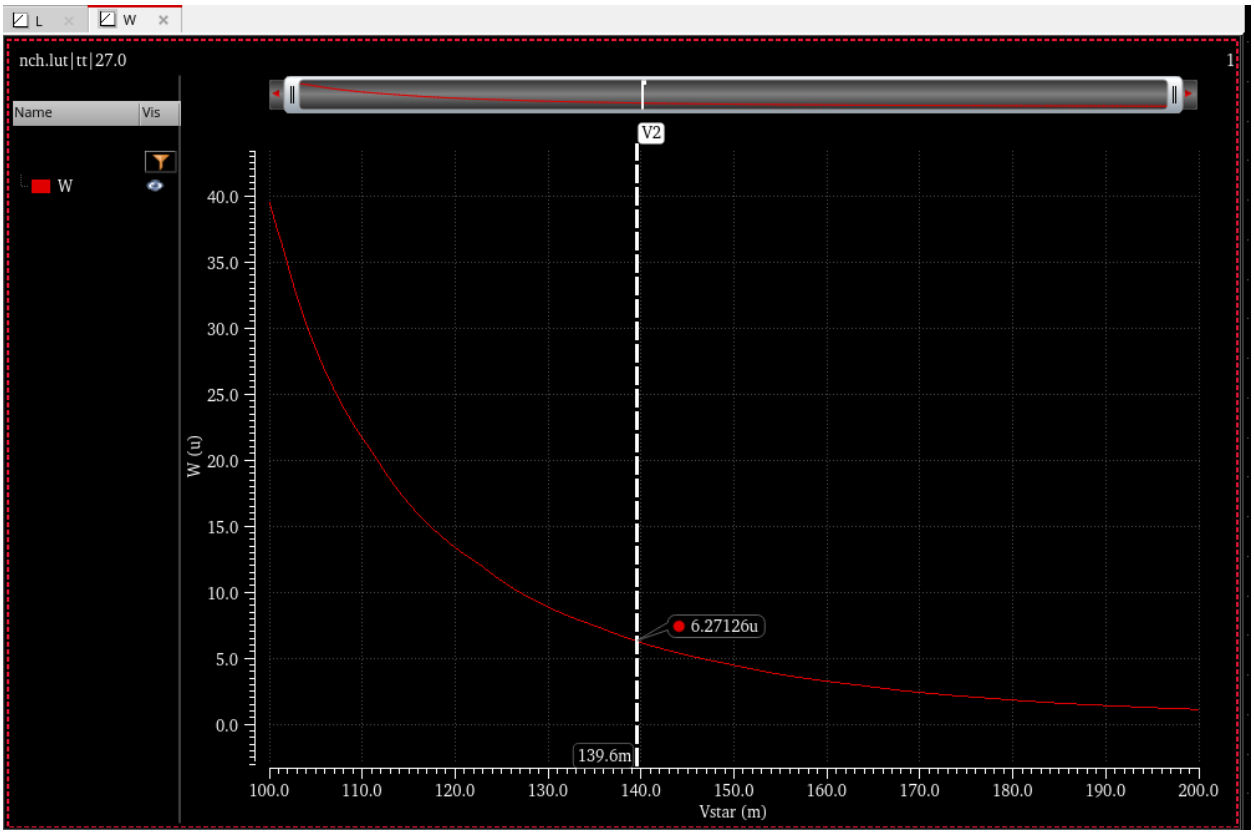

ADT Sizing Assistant
Settings
Help
LUT Settings
State1
Save State
ID
10u
Vstar
100m:200m
1/VA
0.1
VDS
1
VSB
0
Stack
1
Get
Apply
Y-Expr
gm
Plot
Replace
Append
Device Parameters
Parameter Value
1 ID Double click t...
2 L Double click t...
3 W Double click t...
4 VGS Double click t...
5 VDS Double click t...
6 VSB Double click t...
7 gm/ID Double click t...
8 Vstar Double click t...
9 fT Double click t...
10 gm/gds Double click t...
11 VA Double click t...
12 ID/W Double click t...
13 gm/W Double click t...

4 PICK A BIAS POINT (VSTAR) THAT GIVES IDMIS < 3%. DETERMINE W AND L. WE WILL USE THESE SIZING PARAMETERS FOR THE CASCODE CURRENT MIRROR AS WELL.

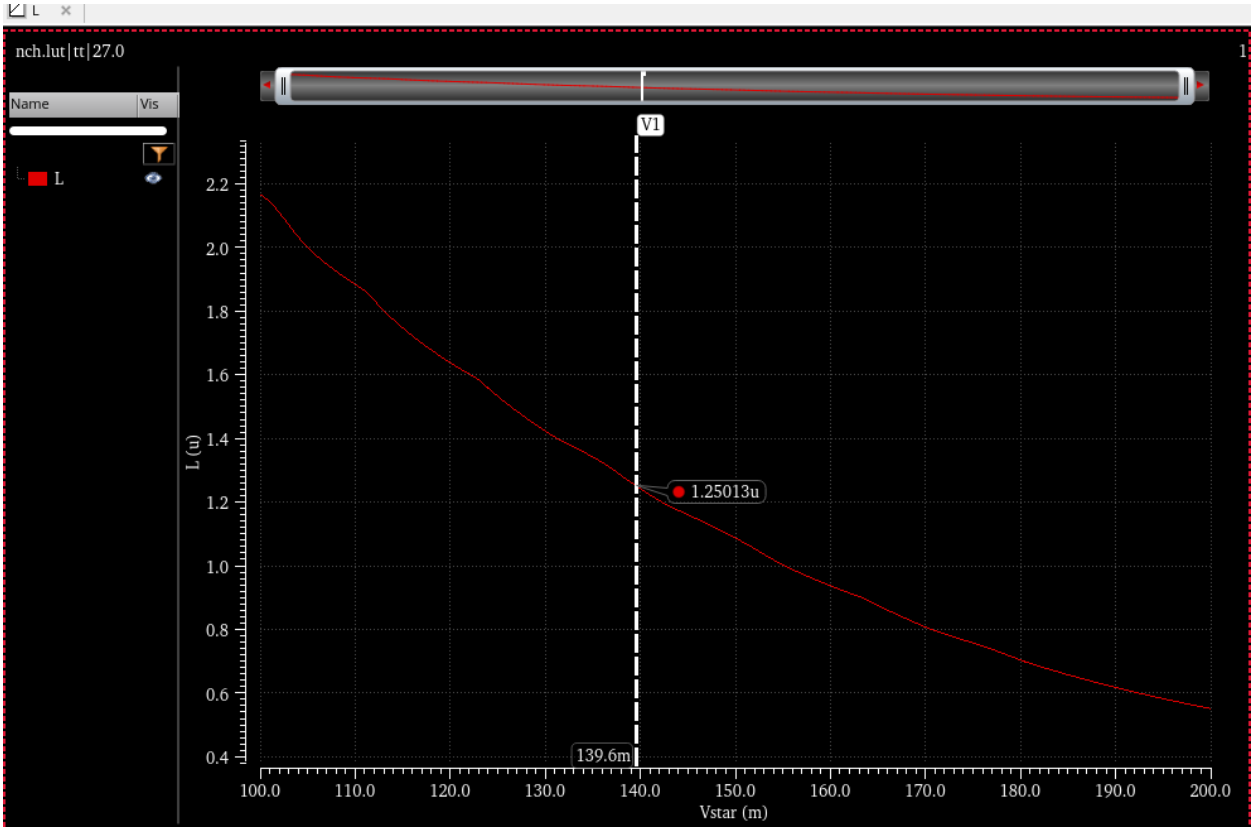


The change in current chosen is 2.544

5 W



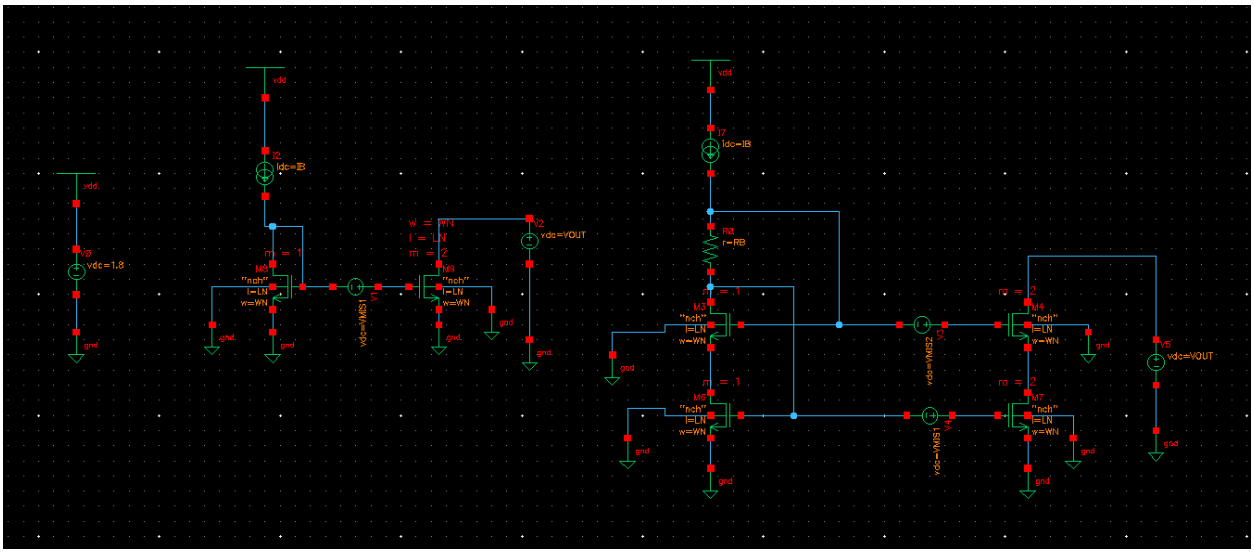
6 L



7 CAN WE DO THE PREVIOUS DESIGN TRADE-OFFS EXPLORATION SWEEPS USING A STANDARD SPICE SIMULATOR, I.E., SWEEP VSTAR AT A CONSTANT λ? WHY?

NO, we can't, Because in standard SPICE simulation, we can't change V* and L (geometry dimensions) at the same time.

Part 2: Current Mirror Simulation

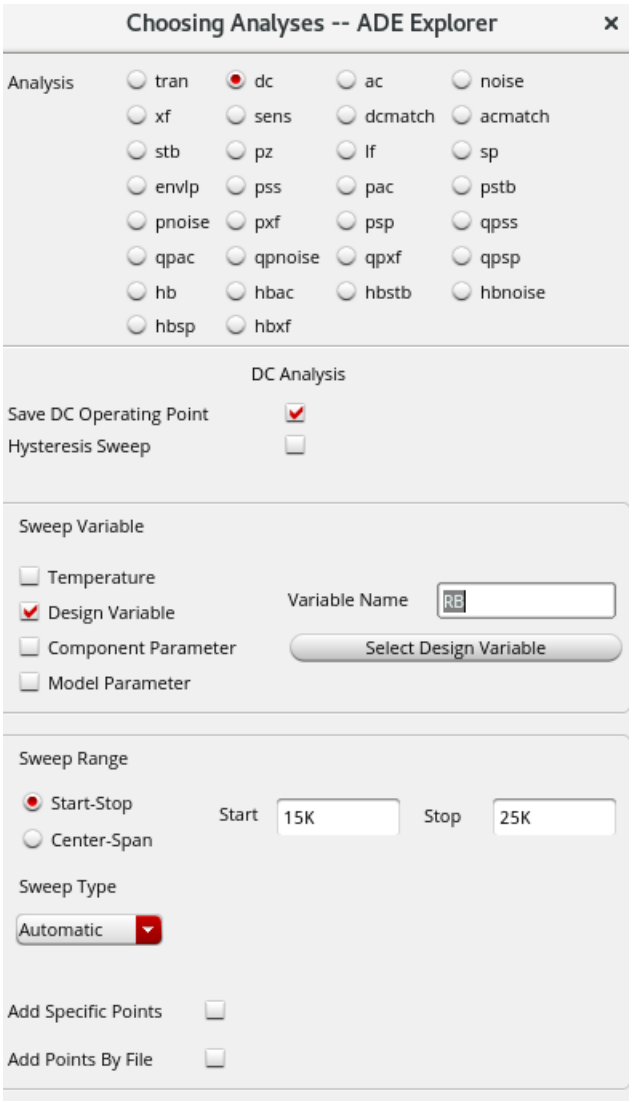


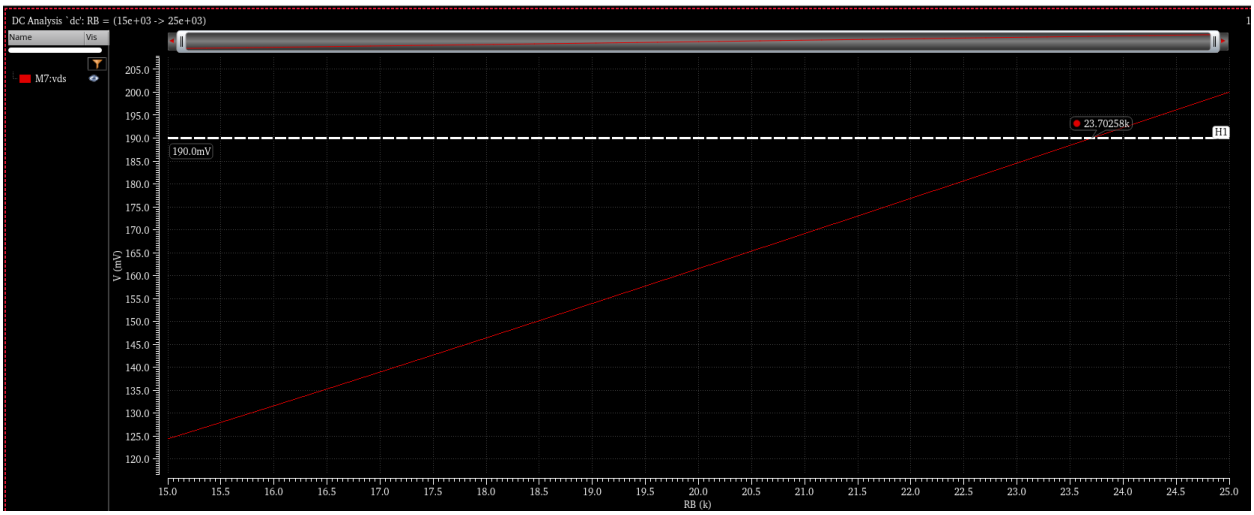
OP ANALYSIS

1 CALCULATE A ROUGH VALUE FOR RB.

RB=$\frac{\text{VDS2}}{\text{IB}} = \frac{(140+50)m}{10u}$ =19K

2 Report $VDS3$ vs RB. Choose RB to satisfy the $50mV$ saturation margin requirement. Is the selected RB value larger or smaller than the rough analytical value? Why?

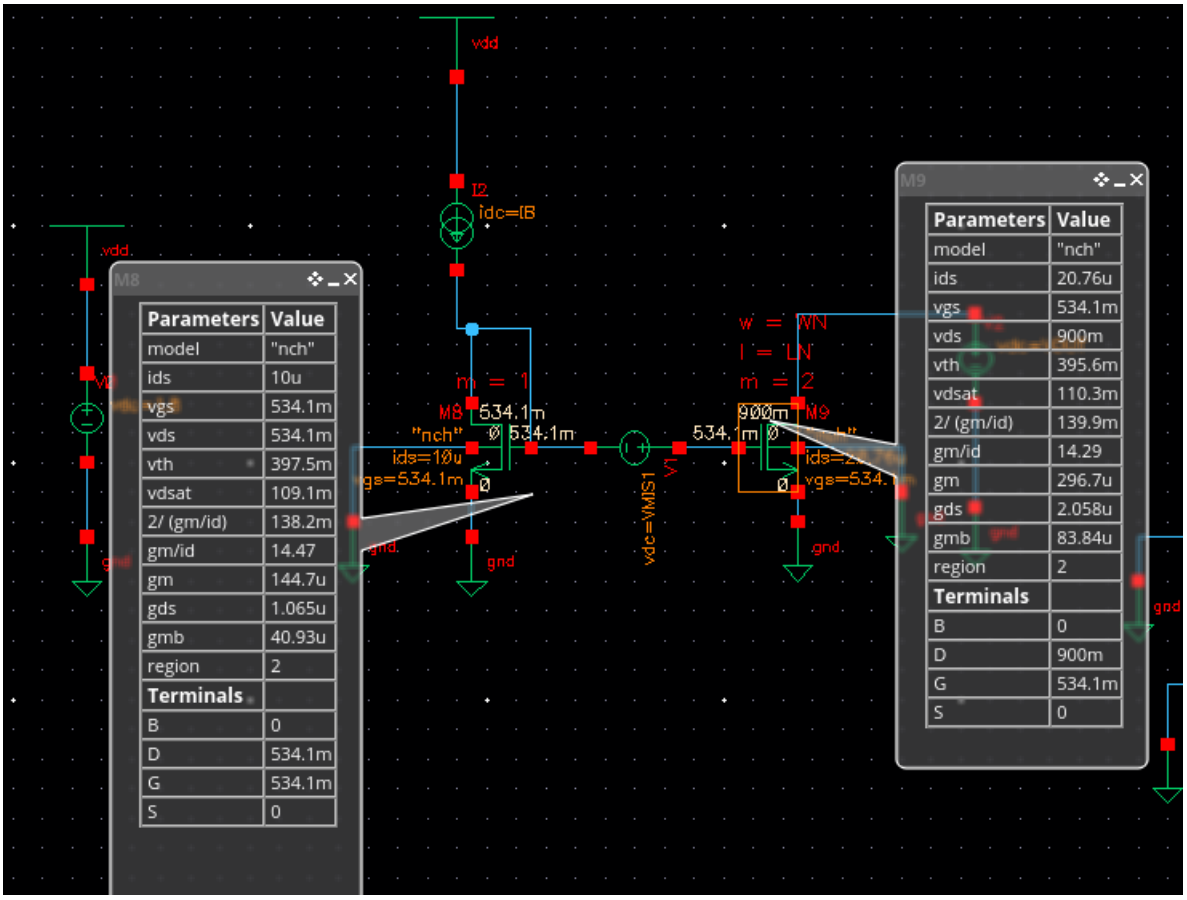


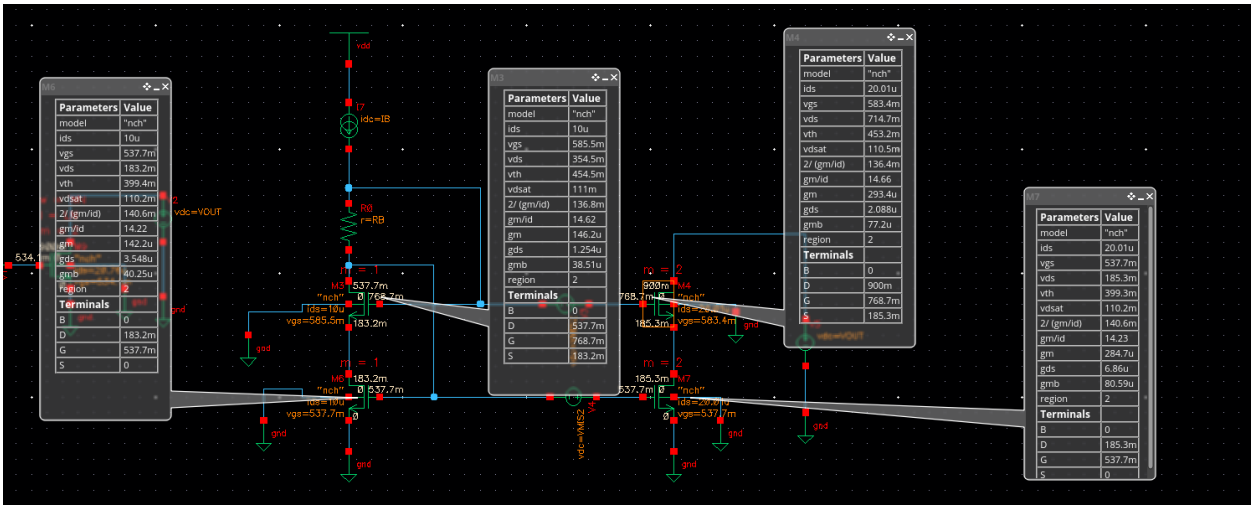


RB from SIM = 23.7k

Yes the sim value is larger than the rough analytical value, as VGS4 not equal to VGS6 (in my schematic) because of body effect which leads to higher RB.

3 SIMULATE THE OP POINT.



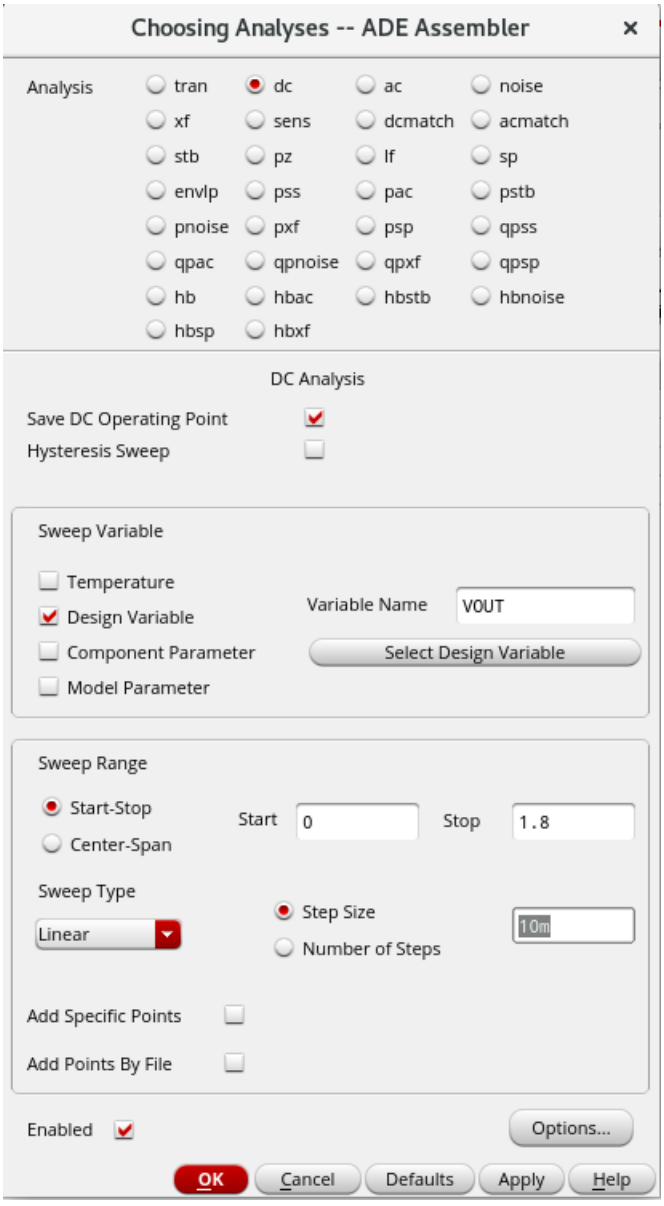


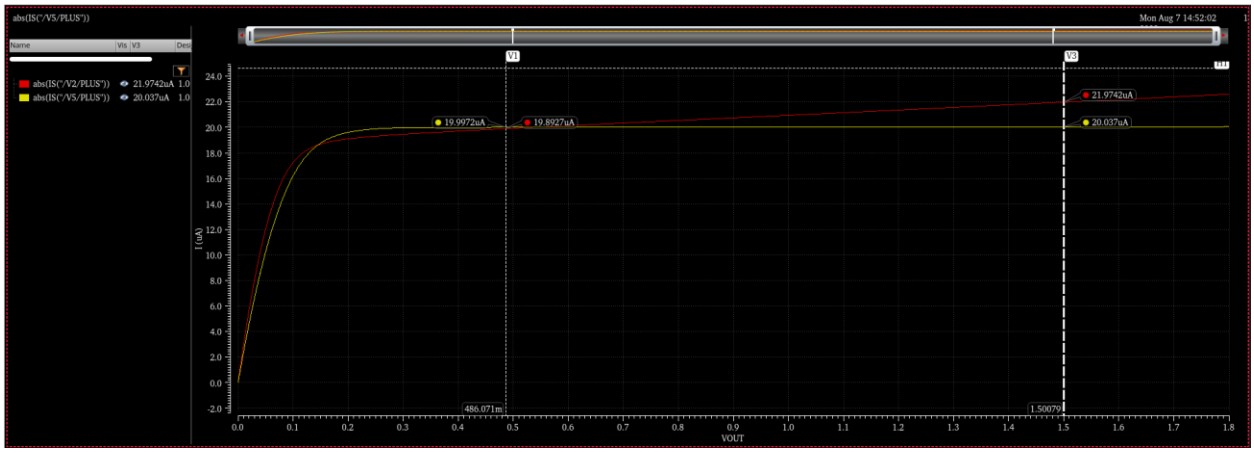
4 DO ALL TRANSISTORS OPERATE IN SATURATION?

Yes all TRANS in region 2 (saturation).

DC Sweep ($Iout$ vs VOUT)

1 PERFORM DC SWEEP (NOT PARAMETRIC SWEEP) USING VOUT = 0:10M:VDD. REPORT $Iout$ VS VOUT FOR THE TWO CMS OVERLAID IN THE SAME PLOT.





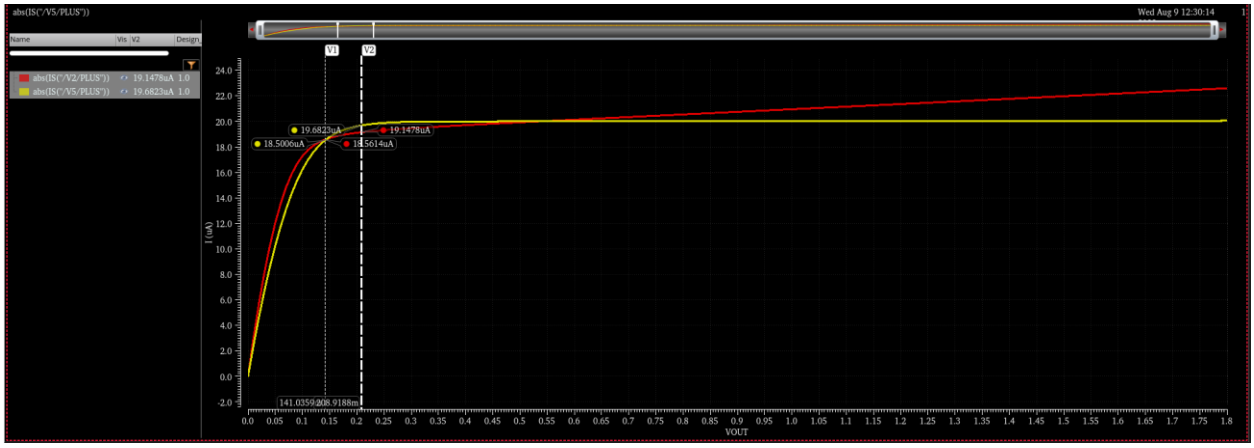
RED : basic (common source) current Mirror

YELLOW: cascode current Mirror

1.1 COMMENT ON THE DIFFERENCE BETWEEN THE TWO CIRCUITS

As Vout (VDS) increases the cascode circuit is more robust and stable than the common source, AS in common source Vout directly affect the Vds of M1(M9 in mine) and as we increasing Vds, VA increased but this is not the case in cascode, as there are two transistors and vds of the lower TRANS is determined by Vb so the current is much more stable.

1.2 FROM THE PLOT, FIND AN ESTIMATE FOR THE COMPLIANCE VOLTAGE OF EACH CURRENT MIRROR

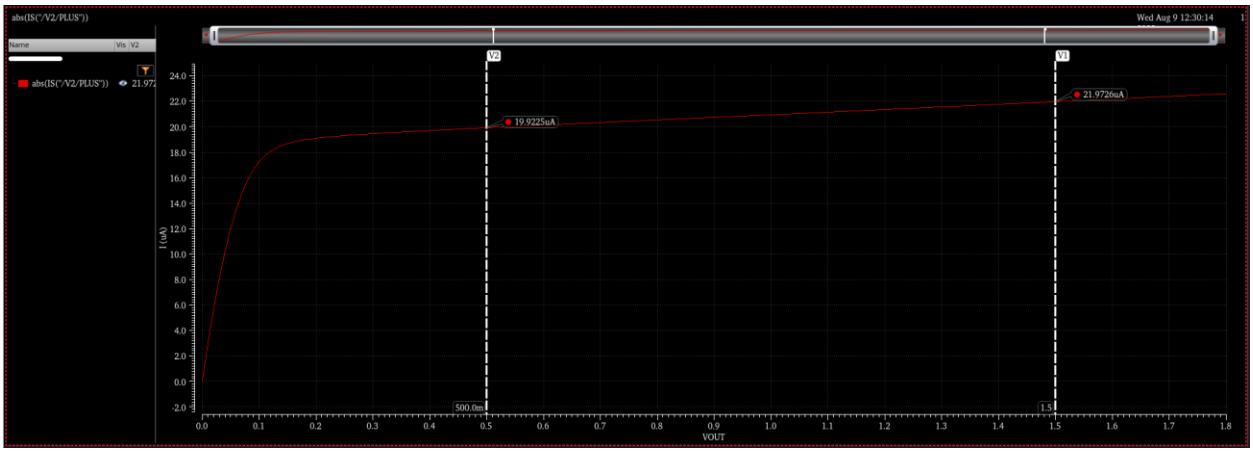


For CS : 141 mv

For cascode : 209 mv

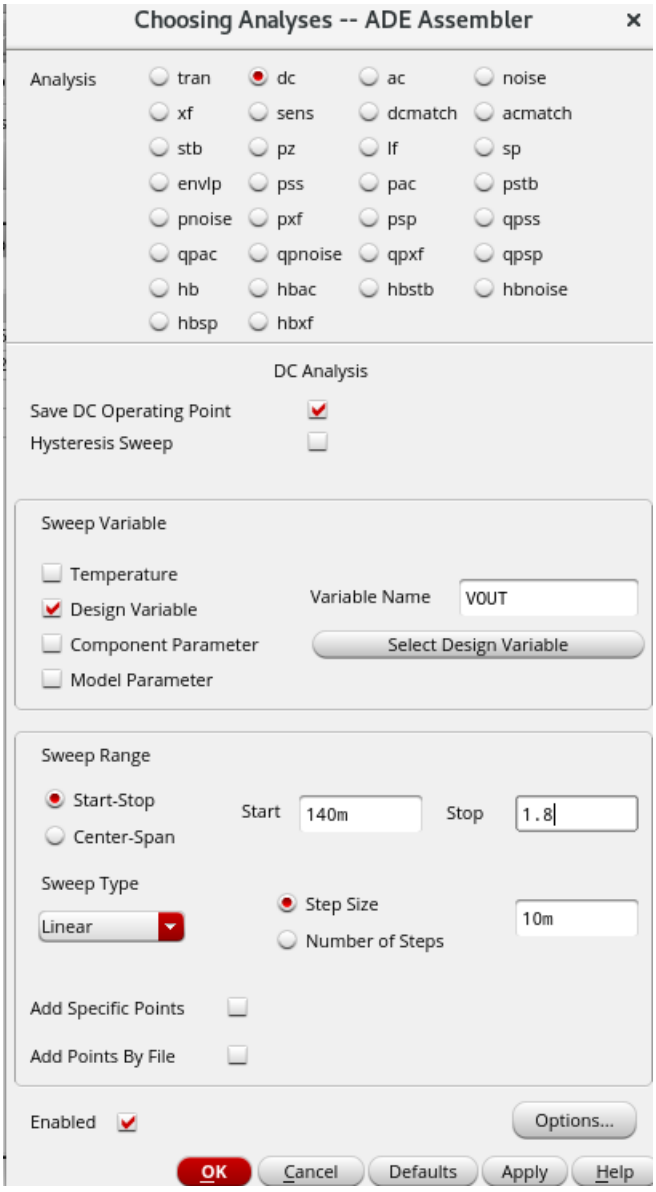
1.3 *Iout* OF THE SIMPLE CM IS EXACTLY EQUAL TO IB*2 AT A SPECIFIC VALUE OF VOUT. WHY? Because in the case of the simple CM, Vout is equal to VDS so it directly affect it and as we increasing VDS, VA increased and more CLM affects .

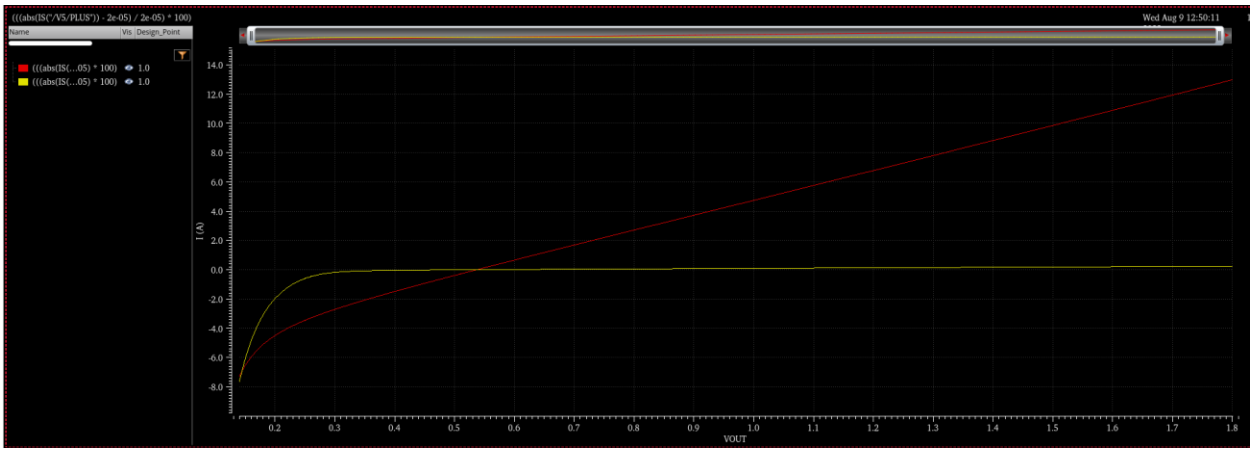
2 FOR THE SIMPLE CURRENT MIRROR, CALCULATE THE PERCENT CHANGE IN *Iout* WHEN VOUT CHANGES FROM 0.5V TO 1.5V (I.E., 1V CHANGE). COMPARE THE RESULT TO THE VALUE EXPECTED FROM PART 1.



$\frac{21.97\text{-}19.92}{20} * 100 = 10.25\%$ so close the the error given in part 1.

3 REPORT THE PERCENT OF ERROR IN $Iout$ VS VOUT

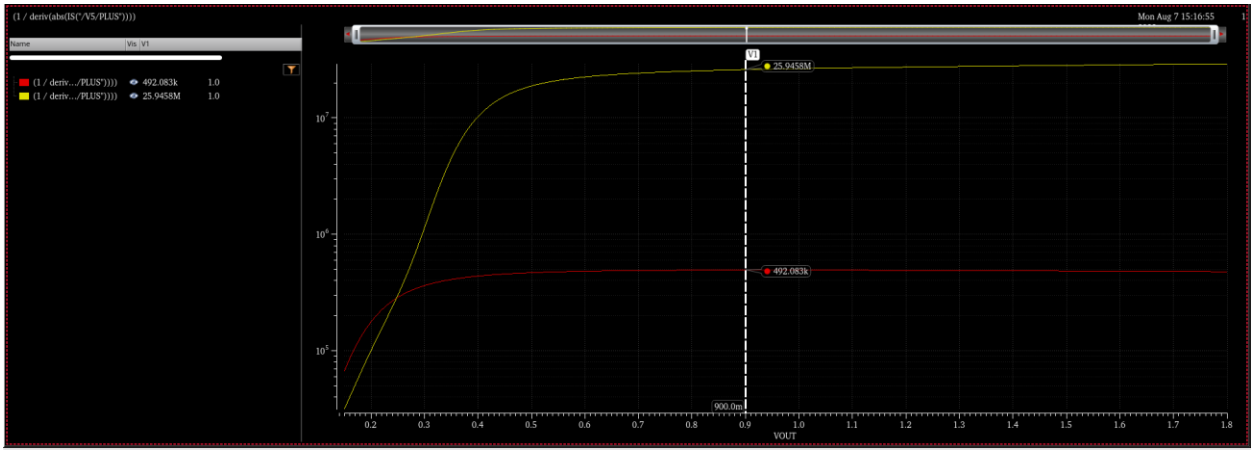




3.1 COMMENT ON THE DIFFERENCE BETWEEN THE TWO CIRCUITS

As said above, the cm has large dependence on vout as it the direct VDS of it, and as we increasing VDS, VA increased so, the current as more dependent on Vout, but in cascode case there is decreased dependence on VOUT as it not the direct vds of the mirror device.

4 REPORT ROUT VS VOUT (TAKE THE INVERSE OF THE DERIVATIVE OF $Iout$ PLOT) FOR THE TWO CMS IN THE CURRENT MIRROR OPERATING REGION



ROUT(CS)=492k

ROUT(CASCODE)=25.9M

4.1 Comment on the difference between the two circuits

The cascode has larger Rout as expected, because it boosts Rout
in cm: Rout=r09

In cacosde: Rout= gm4*r04*r07

4.2 Does Rout change with VOUT? Why?

Yes, because Rout depends on ro which depends on VDS (AS VDS increased r0 increased).

5 Analytically calculate Rout of both circuits at VOUT = VDD/2. Compare with simulation results in a table

For cm mirror : Rout=ro9=1/gds9=1/2058u= 485.9k ohm

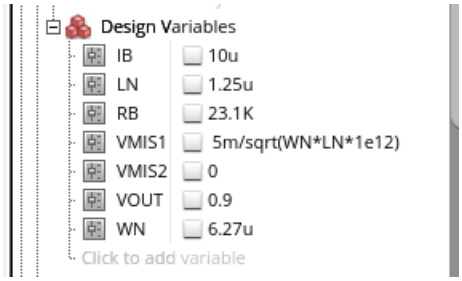
For cascode: Rout= gm4*r04*r07= 293.4u * (1/2.088u) * (1/6.86u) =21.3M

we neglected body effect, so it is expected to see higher Rout in SIM more than the case of Analytical

	SIM	ANALYTICAL
Cm mirror	492K	485.9K
Cascode	25.9M	21.3M

Mismatch

1 Set VMIS1 = 5m/sqrt(W*L) and VMIS2 = 0. This models the standard deviation of the mismatch in VTH for the current mirror devices. Run OP simulation. Find the percent change in IOUT



LAB4_part1_1	(((abs(IS("/V5/PL...	2.553			
LAB4_part1_1	(((abs(IS("/V2/PL...	6.363			

In cacosde -> 2.55 %

In cs -> 6.36 %

2 Analytically calculate the percent change in $Iout$ and compare it to the simulation result

$$\text{Vmismatch} = \frac{5\text{mu}}{\sqrt{6.27*1.25}} = 1.76\text{mv}$$

$$\text{GM} = \frac{\Delta\text{I}}{\text{Vmismatch}} = \frac{2\text{ID}}{\text{V*}}$$

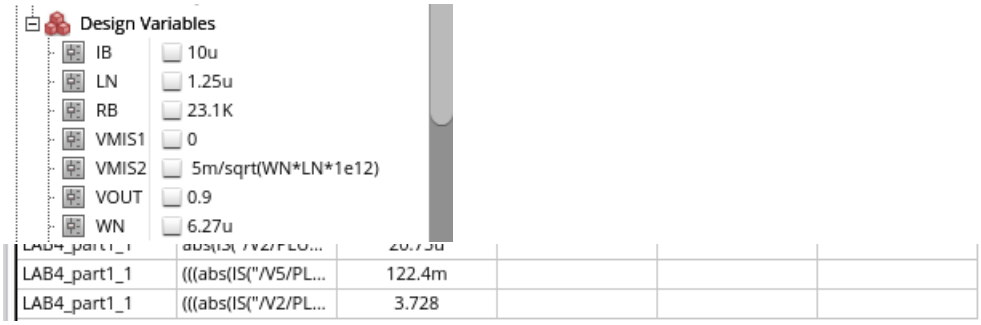
$\frac{\Delta I}{ID} = \frac{2Vmis}{V^*} = \frac{2*1.76m}{140m} = 0.025 = 2.5\%$ for CS

$\frac{\Delta I}{ID} = \frac{2Vmis}{V^*} = \frac{2*1.76m}{140m} = 0.025 = 2.5\%$ for Cacode circuit

	SIM	ANALYTICAL
Cm mirror	6.36	2.5
Cascode	2.55	2.5

NOTES: Dc bias point is the same for the two circuits analytically, and we didn't get into consideration the dependence on Vds effect.

3 SET VMIS1 = 0 AND VMIS2 = 5M/SQRT(W*L). THIS MODELS THE STANDARD DEVIATION OF THE MISMATCH IN VTH FOR THE CASCODE DEVICES. RUN OP SIMULATION. FIND THE PERCENT CHANGE IN $Iout$.



In cacosde circuit -> 0.1224 %

In cs mirror circuit -> 3.728 %

4 ANALYTICALLY CALCULATE THE PERCENT CHANGE IN $Iout$ AND COMPARE IT TO THE SIMULATION RESULT.

For CS: vmismatch1 = 0v so there is no mismatch which leads to no change in current

For Cascode: the upper transistor is degenerated with RS=ro (we didn't take into consideration the body effect)

$$GM = \frac{\text{gm4}}{1 + \text{gm4*r07}} = \frac{293.4u}{1 + 293.4u * (1/6.86u)} = 6.7u$$

$$\frac{\Delta \text{I}}{\text{ID}} = \frac{\text{GM*Vmismatch}}{\text{ID}} * 100 = 0.059\%$$

	SIM	ANALYTICAL
Cm mirror	3.728	0
Cascode	0.1224	0.059%

5 WHICH MISMATCH CONTRIBUTION IS MORE PRONOUNCED? WHY?

Vmis1 as if we looked from large signal perspective we could see it affects directly VGS of the down transistor (M7) so it gives larger change in current, but Vmis2 affects the two transistors so it affects VDS of (m7) (secondary change) as long as we are still in saturation, and from small signal perspective we could see that the upper transistor is degenerated with the lower transistor so it gives lower Gm, and GM = $\frac{\Delta I}{\text{Vismatch}}$

6 WHICH DESIGN DECISION IS BETTER: SETTING THE SAME W AND L FOR THE MIRROR AND CASCODE DEVICES? OR USING LARGER W AND L FOR THE CURRENT MIRROR DEVICES? WHY?

Using larger W and L as it decreases the mismatch noise, AS we are increasing the Area,but the cascode devices wouldn't be necessary for their area to be increased, AS we showed in the previous question the affect of mismatch is much less.