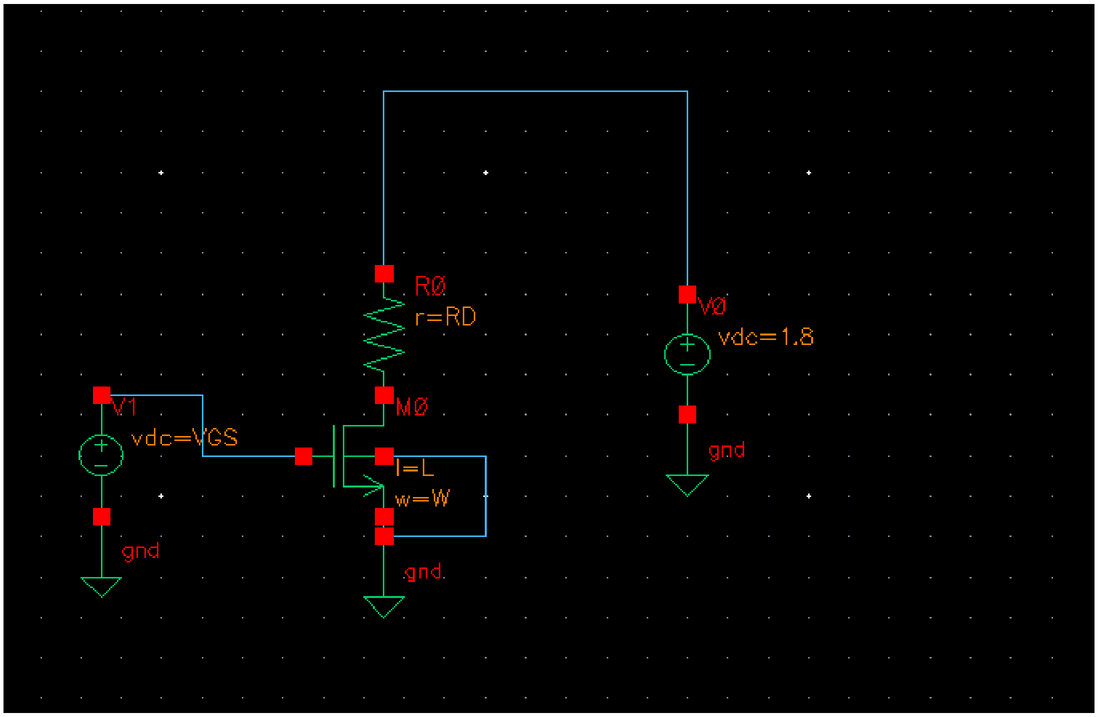
Lab 02 Common Source Amplifier

PART 1: Sizing Chart

1 ASSUMING CM OUTPUT = $VRD = VDD/2$ AND GIVEN THE DC BIAS CURRENT, DETERMINE THE VALUE OF RD.



$$RD = \frac{1.8 - 0.9}{150\mu} = 6K\ \Omega$$

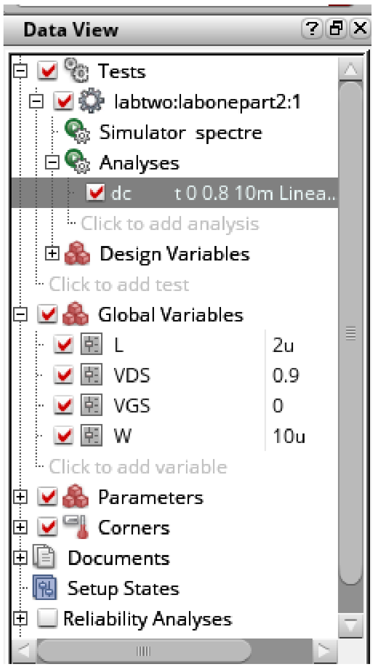
Vrd=0.9 V

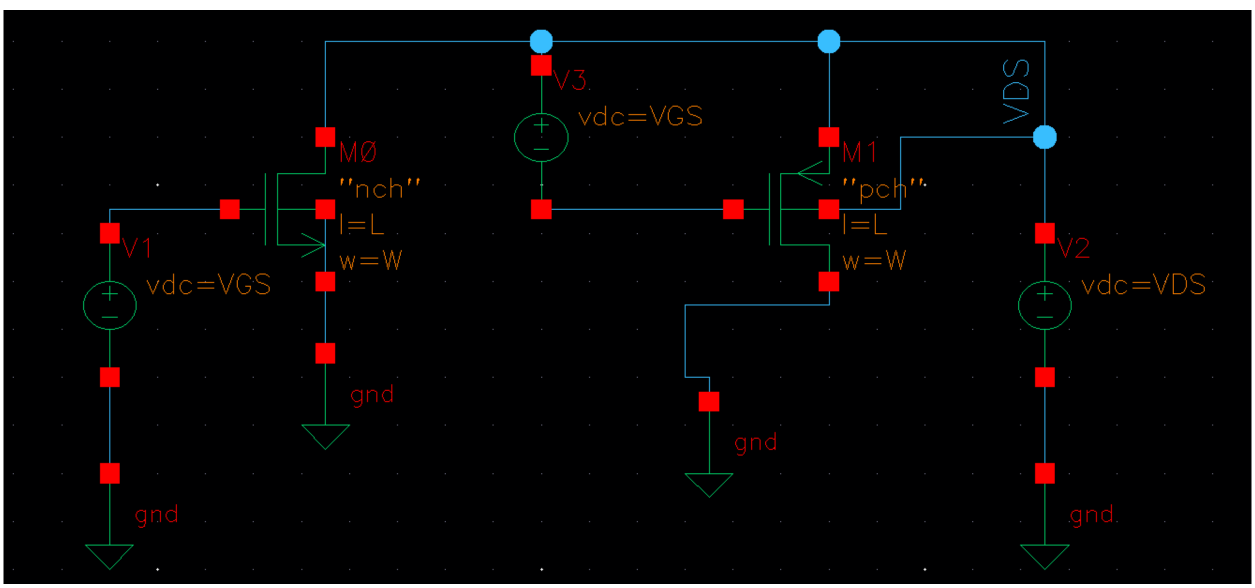
2 GIVEN Av AND VRD , CALCULATE THE REQUIRED $V*$ (AGAIN NOTE THAT $V* \neq Vov$ FOR A REAL MOSFET). LET'S NAME THIS VALUE $VQ*$.

$$|Av| = \frac{2Vrd}{V*}, V* = \frac{2Vrd}{|Av|}$$

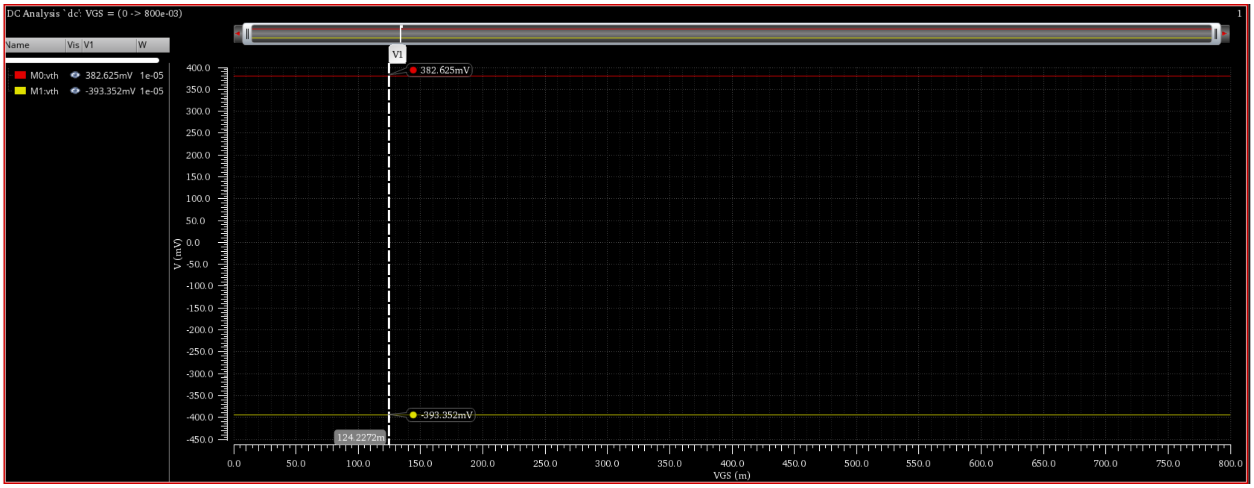
$$V* = \frac{2*0.9}{6} = 0.3\ V$$

3 Create a testbench for NMOS and PMOS characterization (we will use the PMOS later in Part 2 of this lab). Use $W = 10\mu m$ (we will understand why shortly) and $L = 2\mu$



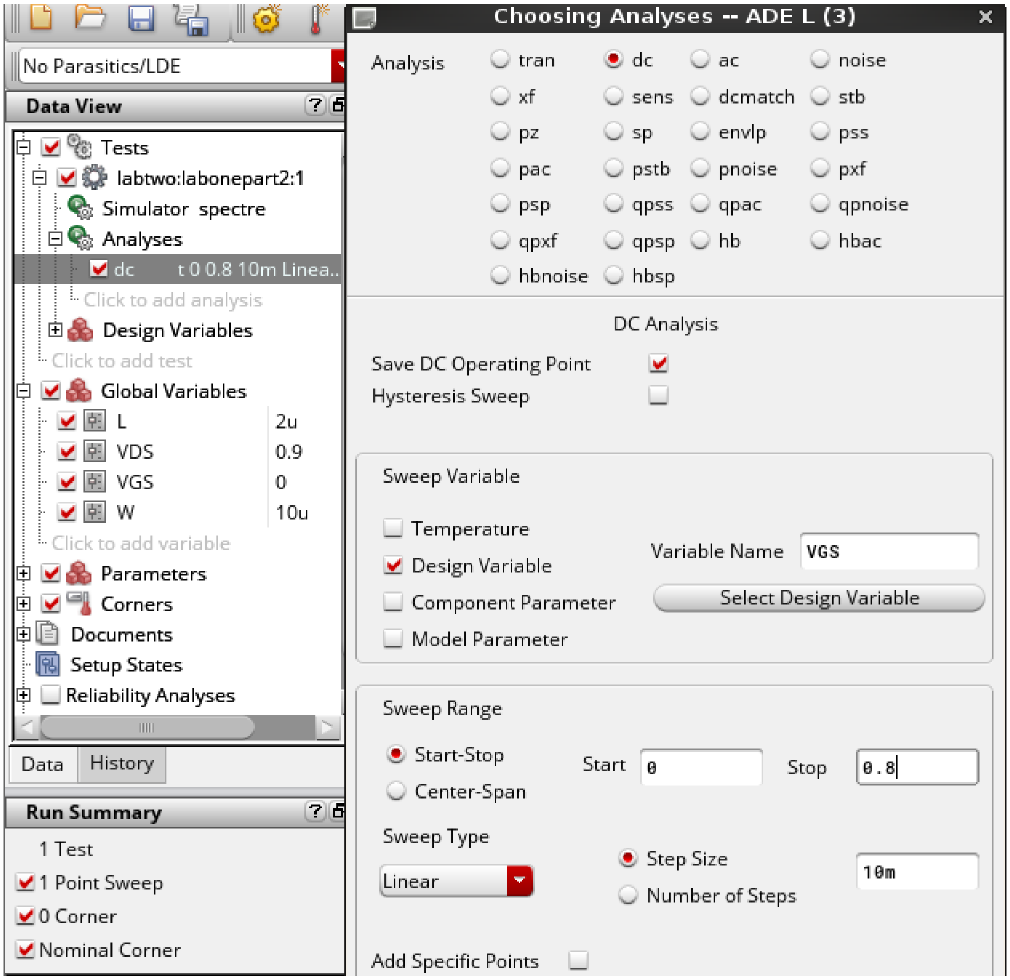


4 SWEEP VGS FROM 0 TO ≈ $VTH + 0.4V$ WITH 10MV STEP. SET $VDS = VDD/2$.

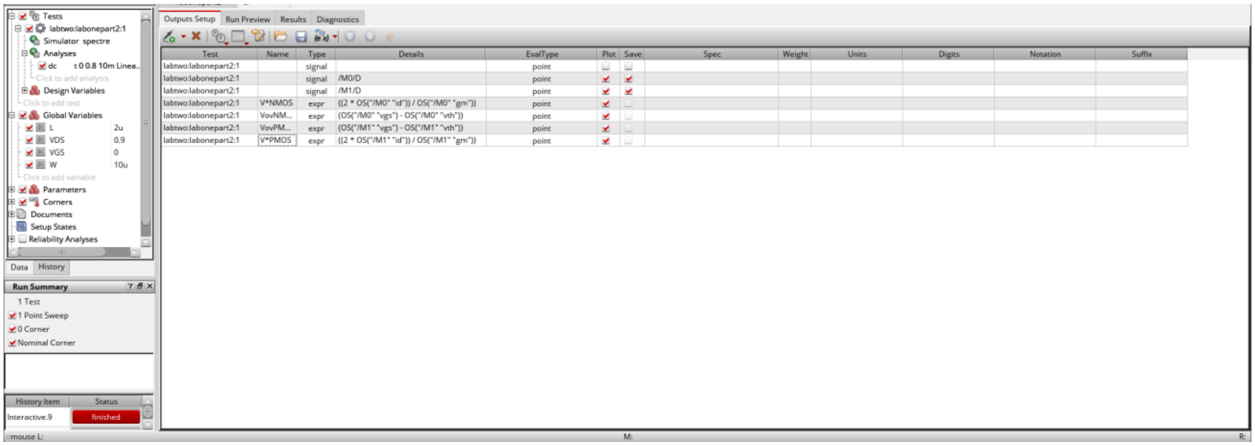


|Vth| for Nmos is 382.6mv , for Pmos 393.352 .

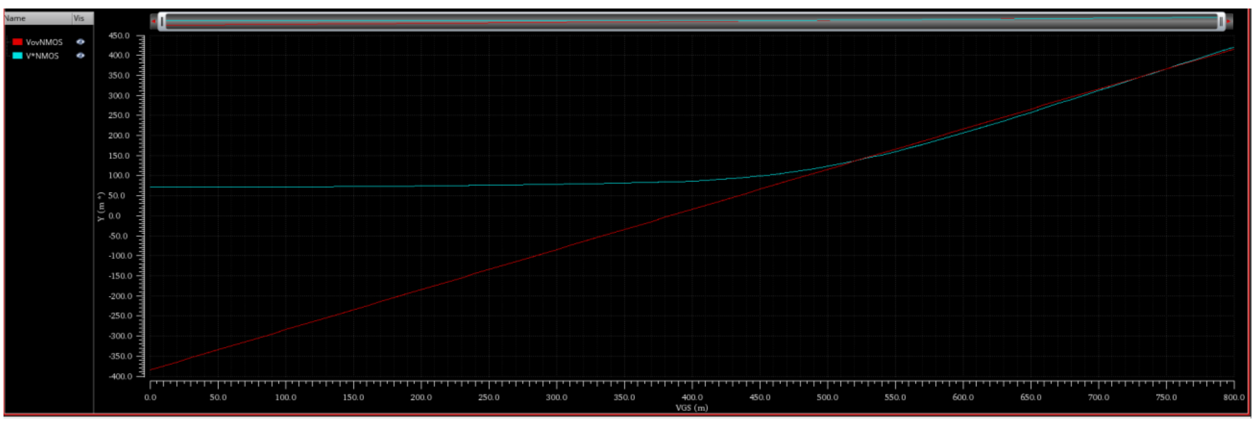
We well sweep VGS from 0 to ≈ 0.4 + 0.4 = 0.8v



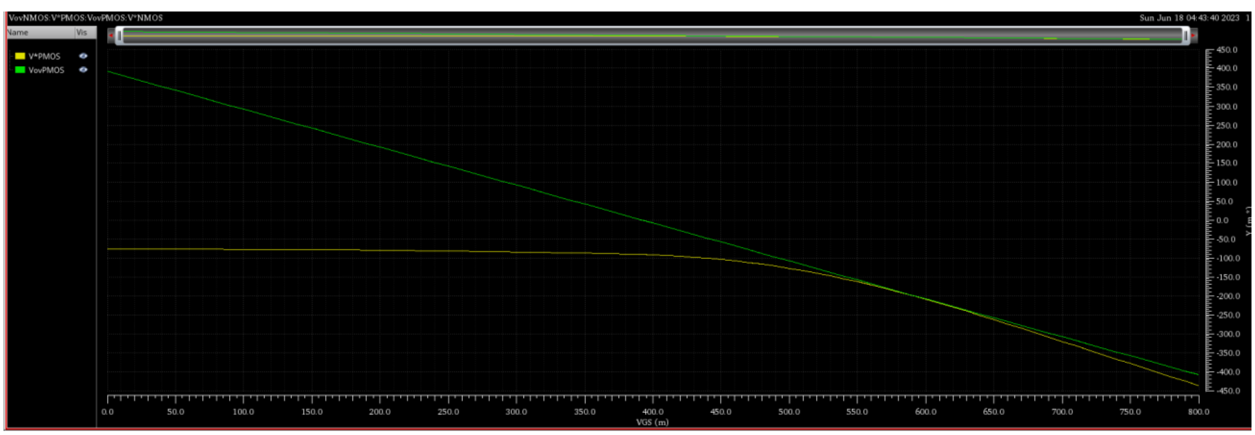
5 COMPARE $V* = 2ID/gm$ AND $Vov = VGS - VTH$ BY PLOTTING THEM OVERLAID. USE THE CALCULATOR TO CREATE EXPRESSIONS FOR $V*$ AND Vov. EXPORT THE EXPRESSIONS TO ADEXL.



6 PLOT $V*$ AND Vov OVERLAID VS VGS. MAKE SURE THE Y-AXIS OF BOTH CURVES HAS THE SAME RANGE.



NMOS

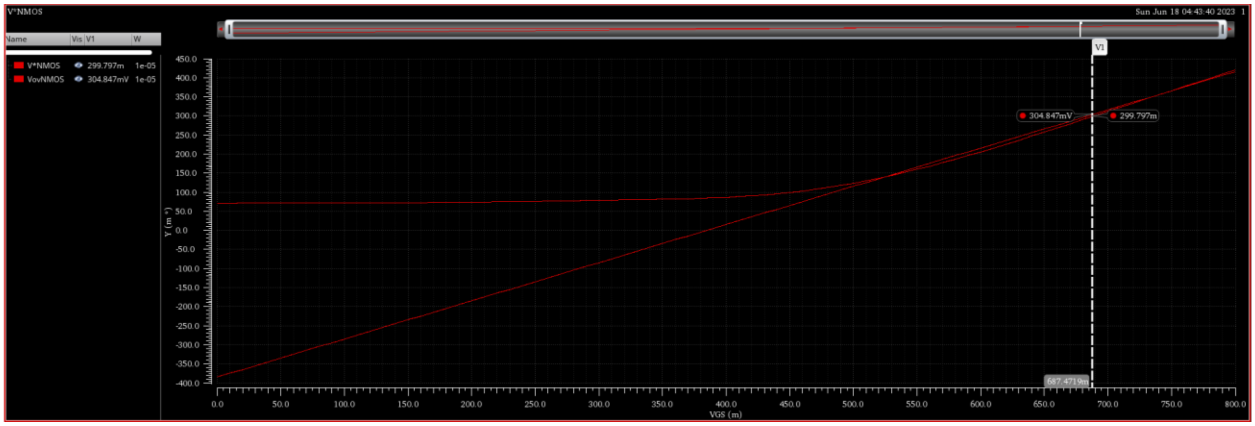


PMOS

NOTE : weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law , the beginning of the strong inversion region, $V*$ and Vov are relatively close to each other (i.e., square-law is relatively valid) , but the strong inversion (high Vov) it is not shown clearly because we swept Vgs to only (Vth+0.4) .

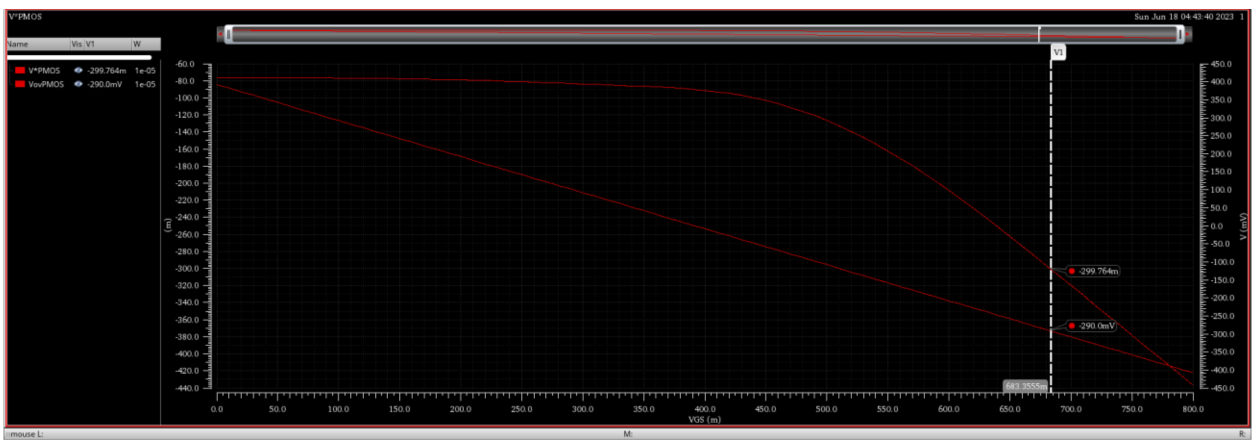
7 ON THE $V*$ AND Vov CHART LOCATE THE POINT AT WHICH $V* = VQ*$. FIND THE CORRESPONDING $VovQ$ AND $VGSQ$.

NMOS :



Vovq =304.85m && VGSq=687.47m

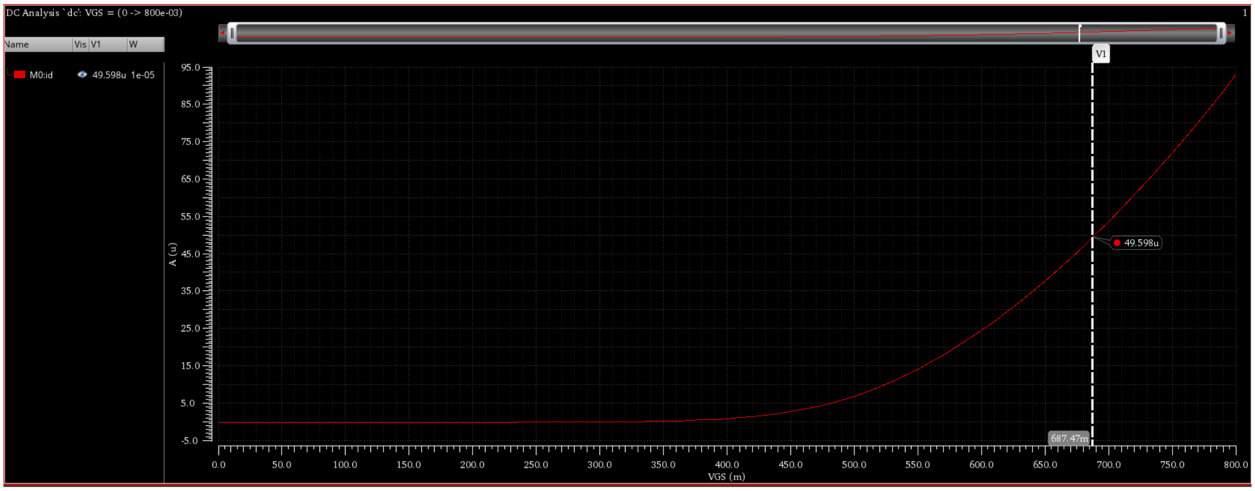
Pmos :

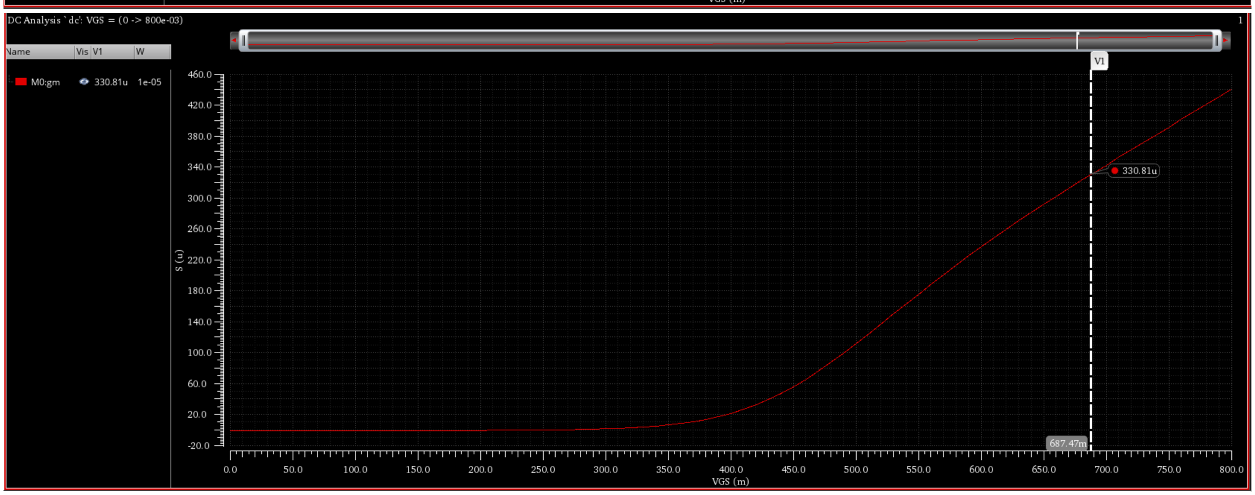


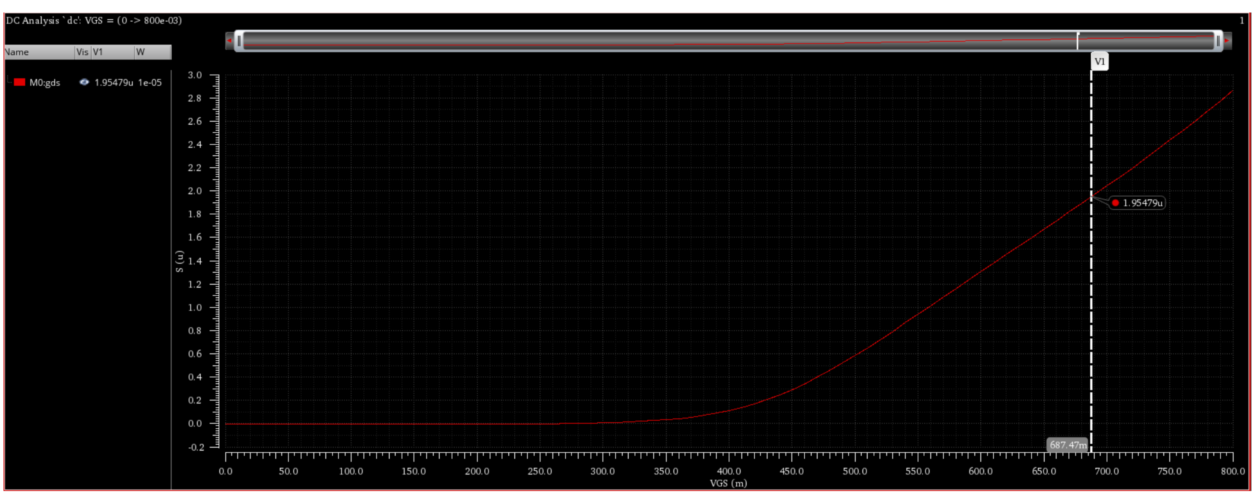
$|Vov$q$|$ =290 m && $|V$GSq$|$=683.35m

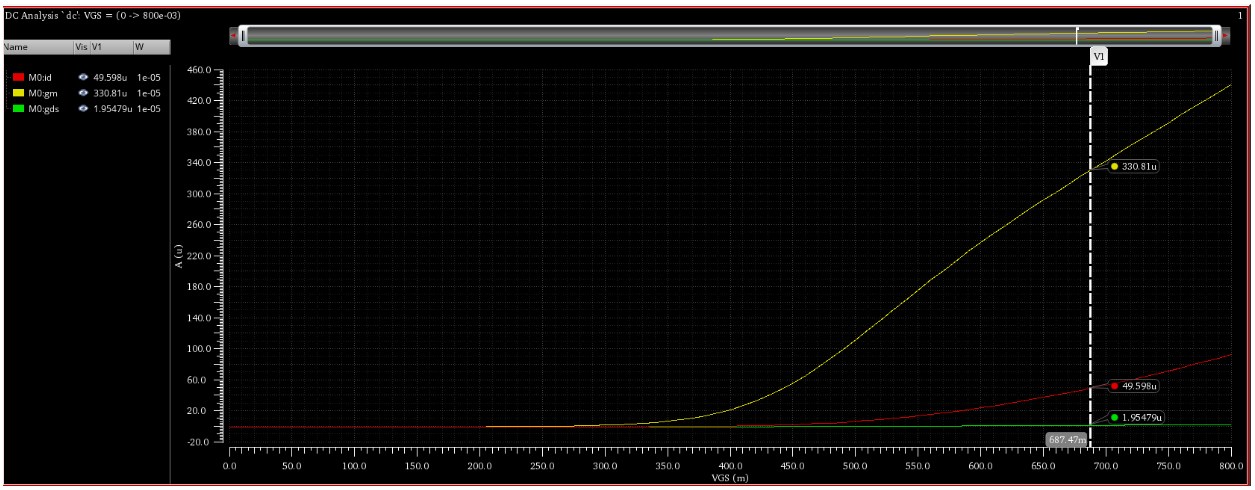
8 PLOT ID, gm, AND gds VS VGS. FIND THEIR VALUES AT $VGSQ$. LET'S NAME THESE VALUES IDX, gmX, AND $gdsX$.

NMOS:



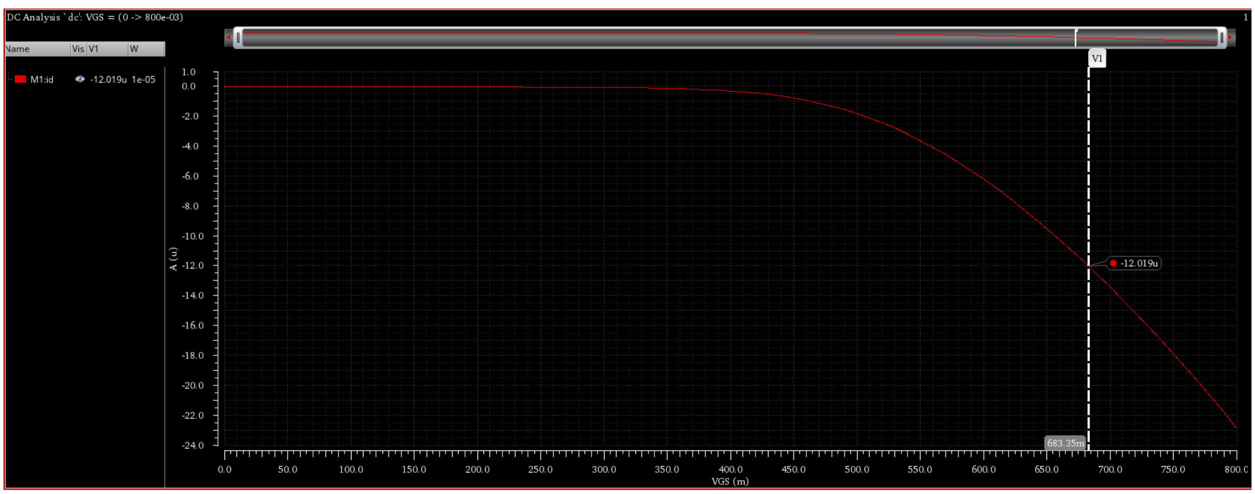


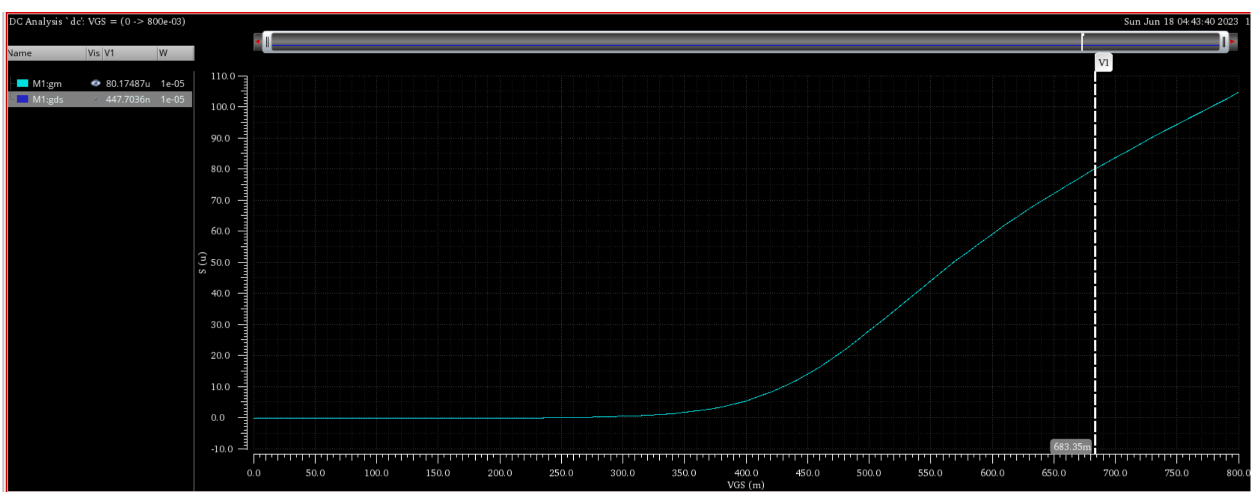


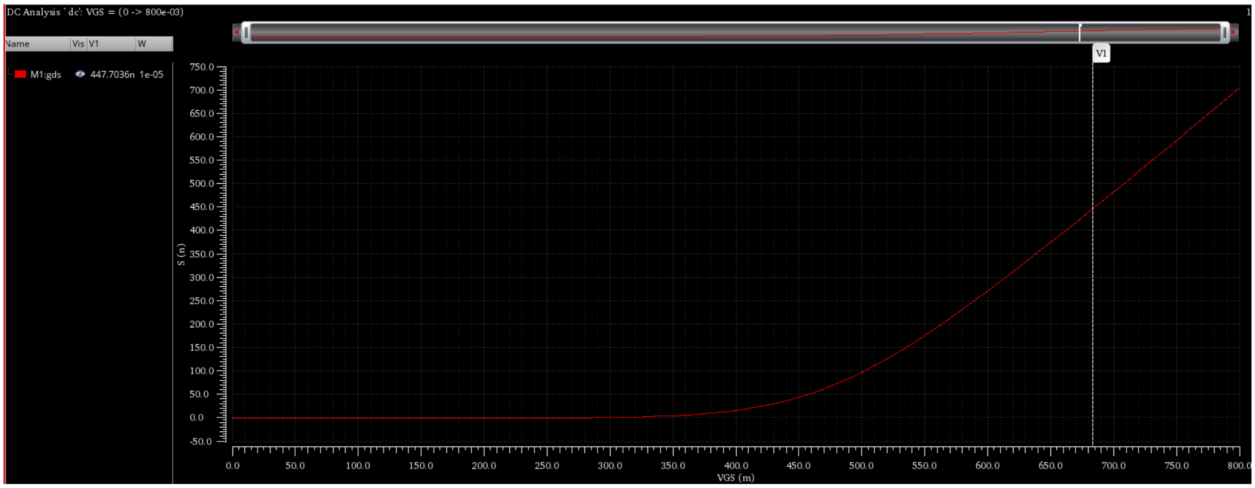


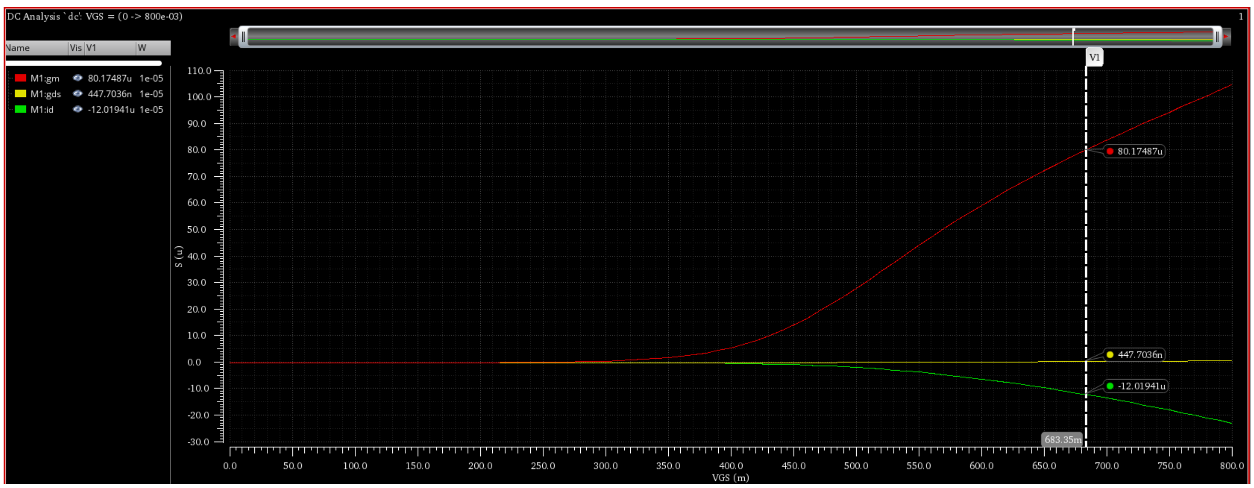
IDX =49.598uA , gmX=330.81u , $gdsX$=1.95479 u

PMOS:









$|IDX| = 12.019\ \mathrm{uA}$, $gmX = 80.1745\mathrm{u}$, $gdsX = 447.7036\ \mathrm{n}$

9 Calculate W

$$Wnmos = \frac{10\mathrm{u} * 150\mathrm{u}}{49.598\mathrm{u}} = 30.243u$$

$$Wpmos = \frac{10\mathrm{u} * 150\mathrm{u}}{12.019\ \mathrm{uA}} = 124.8u$$

- Use DC gain = -6 and ID = 150uA.

10 CALCULATE gmQ AND $gdsQ$ USING RATIO AND PROPORTION AND DOUBLE CHECK THAT $Av = -gm(RD||ro\ )$ MEET THE REQUIRED GAIN SPEC.

$$gm(nmos) = \frac{30.234\text{u} * 330.81\text{u}}{10\text{u}} = 1000.468u$$

$$gds(nmos) = \frac{30.234\text{u} * 1.95479\text{u}}{10\text{u}} = 5.912u$$

$$r0(nmos) = \frac{1}{\text{gds}} = 169.15K$$

$$|Av(nmos)| = 1000.468u * \frac{6k * 169.15K}{6\text{k} + 169.15K} = 5.797 \sim 5.8$$

$$gm(pmos) = \frac{124.8\text{u} * 80.1745\text{u}}{10\text{u}} = 1000.577u$$

$$gds(pmos) = \frac{124.8\text{u} * 447.7036\text{ n}}{10\text{u}} = 5.587u$$

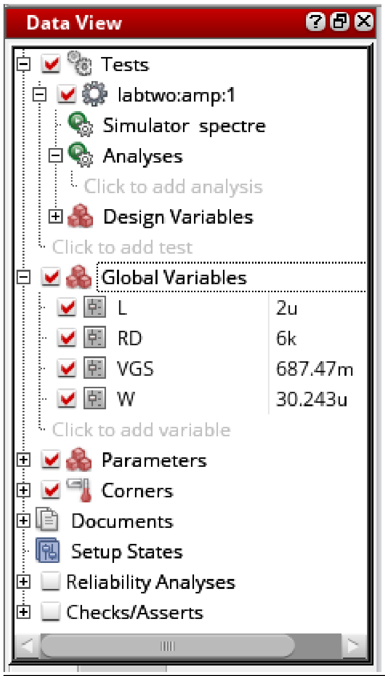
$$r0(pmos) = \frac{1}{\text{gds}} = 178.97K$$

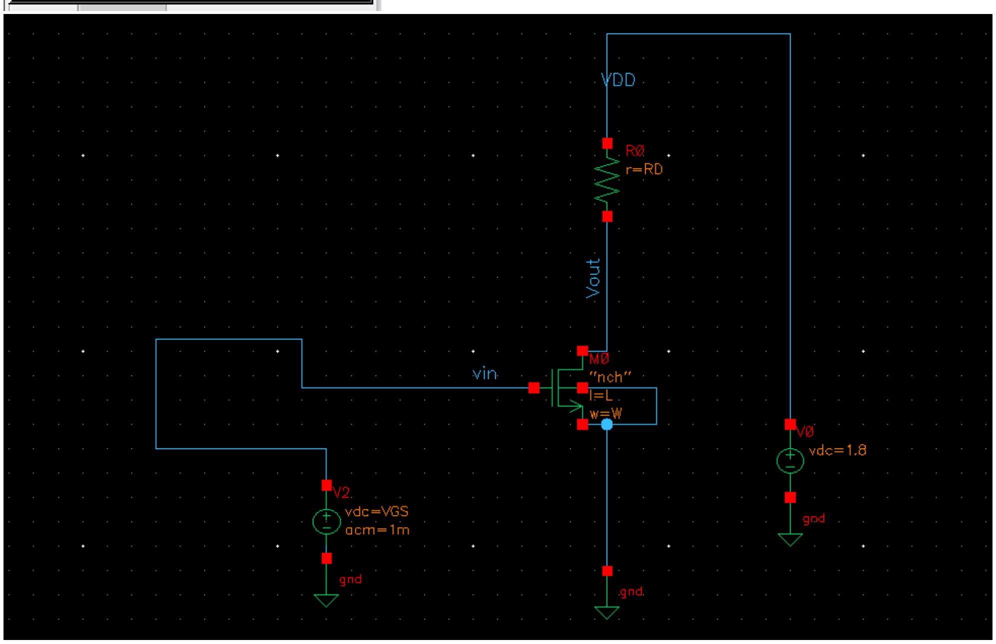
$$|Av(pmos)| = 1000.577u * \frac{6k * 178.97K}{6\text{k} + 178.97K} = 5.8$$

The results meet the specs.

PART 2: CS Amplifier

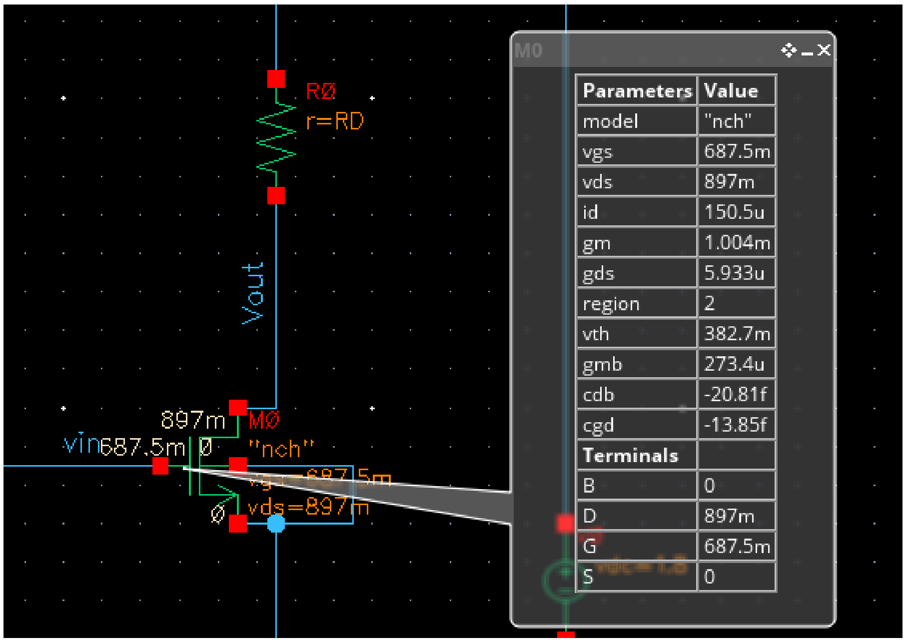
1 Create a testbench for the resistive loaded CS amplifier using the $VGSQ, RD, L,$ and W that you got from the previous part

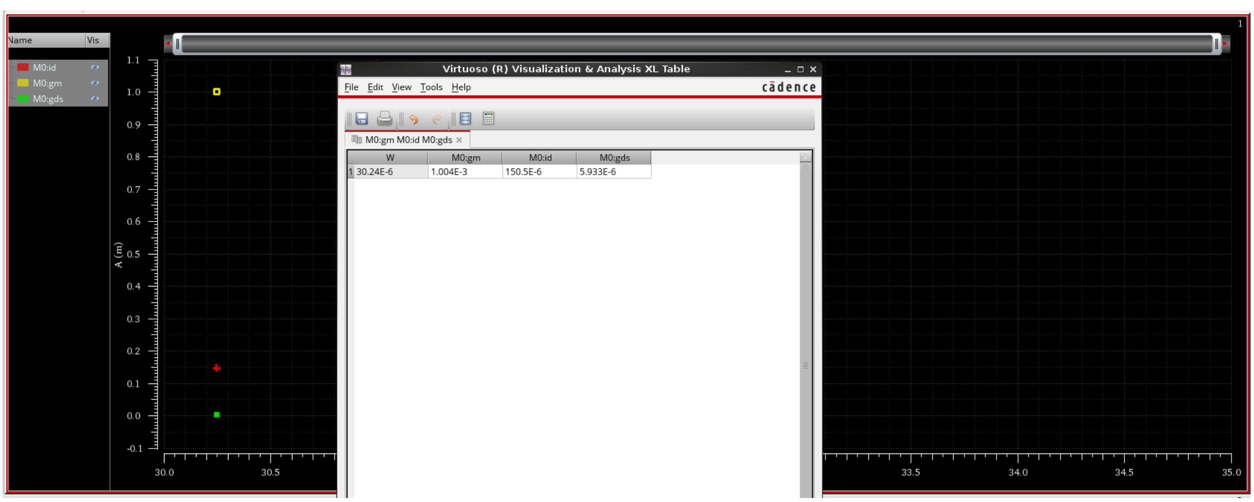




Assume ac small signal 1 m to find the gain in required 6 .

2 Simulate the DC OP. Report a snapshot for the key operating point (OP) parameters. Compare the results with the results you obtained in Part 1. Since we used chart-based design, the results should agree well





	gm	ID	gds
Part 2	1.004m	150.5u	5.933u
Part 1	$1000.468u$	150u	$5.912u$

the results agree well.

Region is 2 which means it works in saturation.

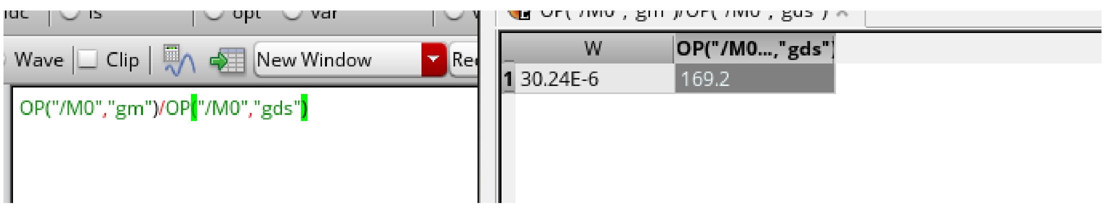
3 COMPARE ro AND RD. IS THE ASSUMPTION OF IGNORING ro JUSTIFIED IN THIS CASE? DO YOU EXPECT THE ERROR TO REMAIN THE SAME IF WE USE MIN L?

r0= 1/gds = 168.55K , RD= 6K , r0 >>RD, Req=$\frac{6*168.55}{6+168.55}k = 5.8k$, error= $\frac{6-5.8}{6}$ =3.33% , yes the error is so small so it is justified to ignore r0.

the error expected to be larger because of short channel effects (channel length modulation) as early voltage (VA) will decrease so r0 would be smaller .

4 CALCULATE THE INTRINSIC GAIN OF THE TRANSISTOR.

|Av|=gm*r0=gm/gds=169.2



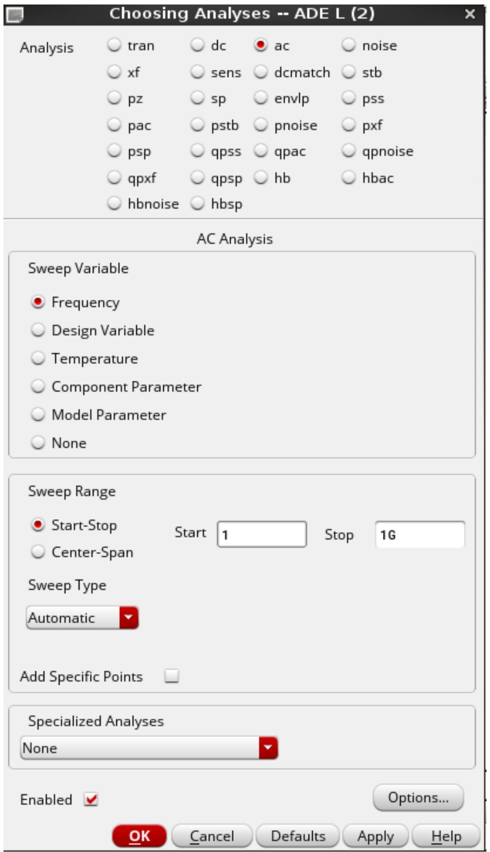
5 CALCULATE THE AMPLIFIER GAIN ANALYTICALLY. WHAT IS THE RELATION (≪,<,= ,>, ≫) BETWEEN THE AMPLIFIER GAIN AND THE INTRINSIC GAIN?

GM=-gm , RS=0,vgs=0 && Rout=RD||r0

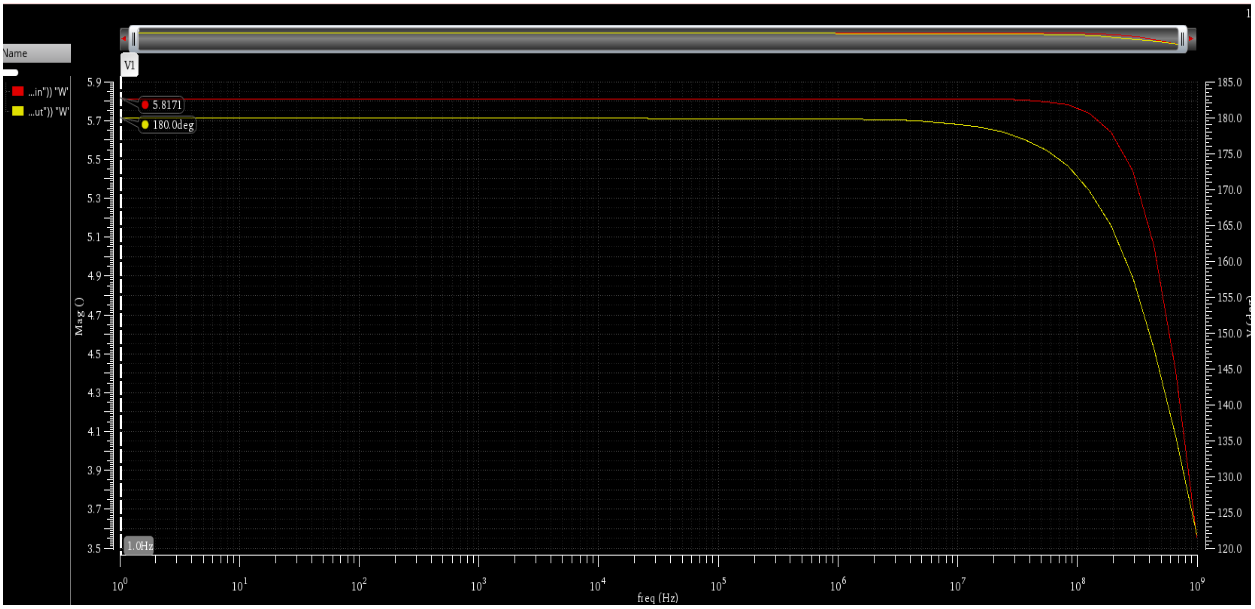
|Av|=gm * RD||r0 = $1.004 * 10^{-3} * \frac{6*10^3*168.55*10^3}{6*10^3+168.55*10^3}$ = 5.817

the amplifier gain << the intrinsic gain , because Rd is much less than r0 so it dominates .

6 Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz). Report the gain vs frequency. Annotate the DC gain and make sure it meets the spec .



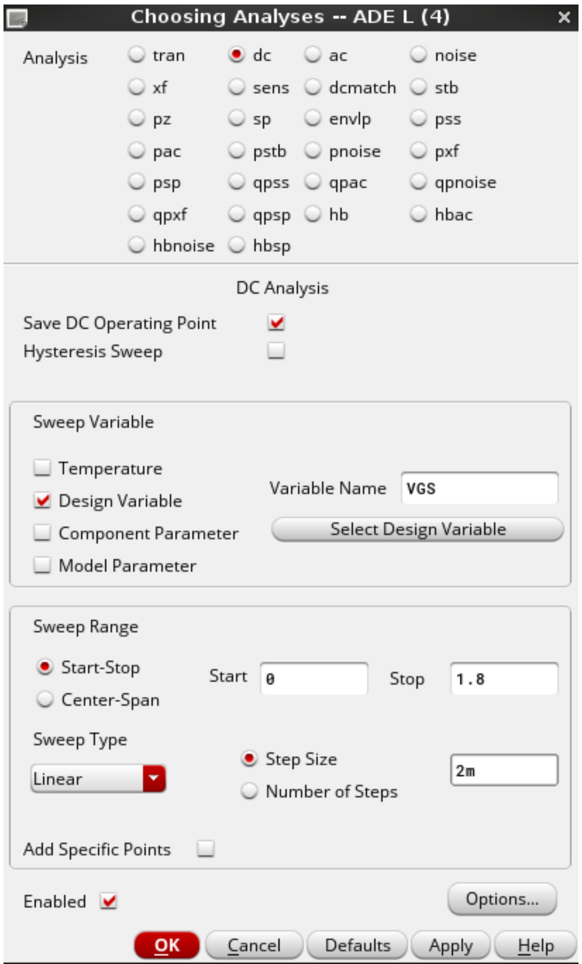
	expr	(VF("/Vout") / VF("/vin"))
	expr	phase((VF("/Vout") / VF("/vin")))



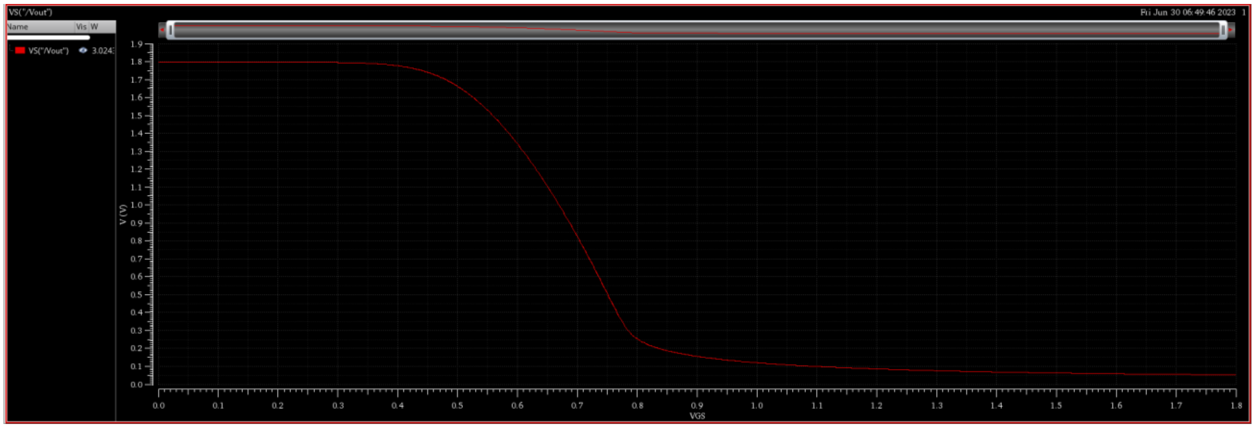
DC gain (when frequency is 1hz) is 5.8171 and also there is a 180-degree phase shift, which meets the specs, we note that when the frequency is too high (more than 10^7) the gain drops.

Gain Non-Linearity

1 Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to VDD with 2mV step.

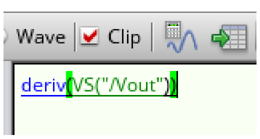


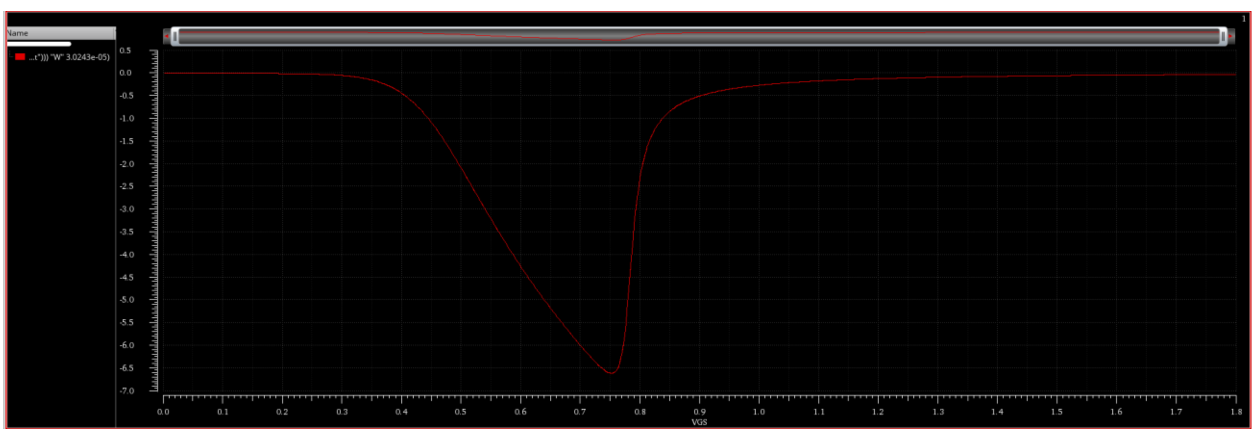
2 Report VOUT vs VIN. Is the relation linear? Why?



The relation is not linear, because VOUT depends on ID (VOUT = VDD – ID * RD), and ID depends on VGS(input) which approximately has quadratic relation with VGS(input) in saturation, and actually Vout variation depends on Vin variation with the slope of this plot which is the gain which is a function of VGS(input), and gain is not linear as it is a function of gm,r0 which are by the way functions of Vin.

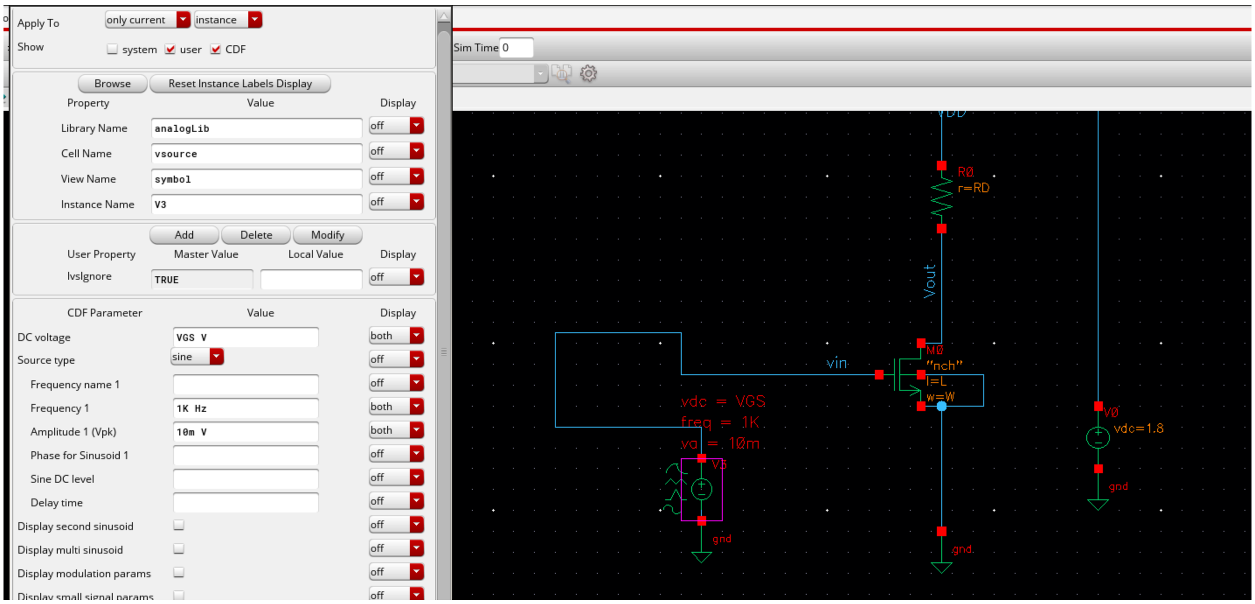
3 Calculate the derivative of VOUT using calculator. Plot the derivative vs VIN. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?



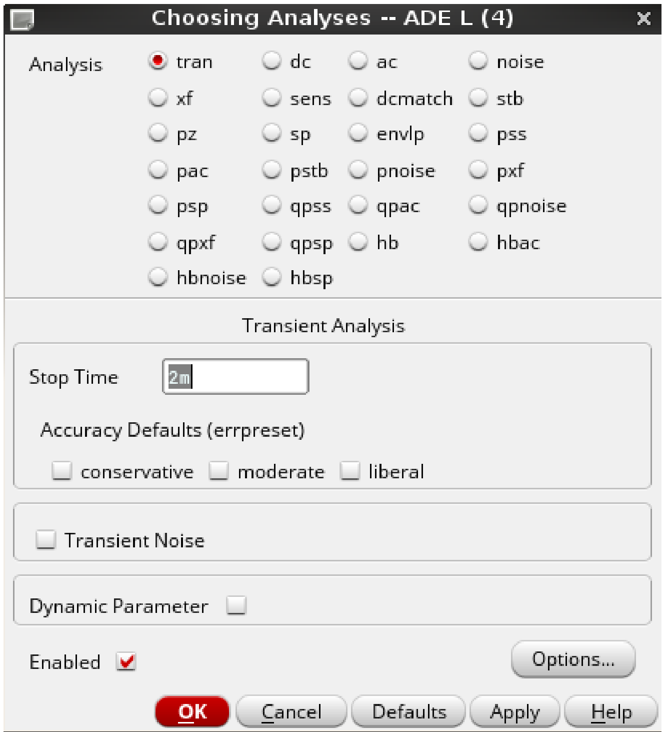


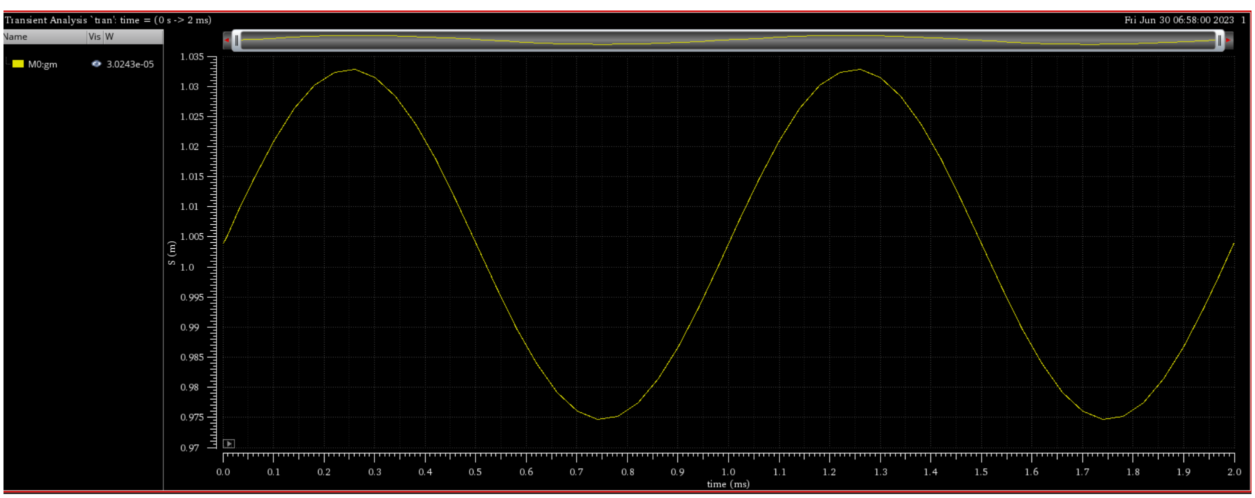
No, gain is not linear because it is a function of gm, r0 (|Av|=gm(RD||r0)) which are actually functions of VGS(Vin) (in case of r0 changing Vin changes Id with it, r0 is the slope of id vs Vout(Vds), so r0 also depends on the change of Vin) then the gain depends on Vin (the input) which make it non linear.

4 SET THE PROPERTIES OF THE VOLTAGE SOURCE TO APPLY A TRANSIENT STIMULUS (SINE WAVE OF 1KHZ FREQUENCY AND 10MV AMPLITUDE SUPERIMPOSED ON THE DC INPUT VOLTAGE).

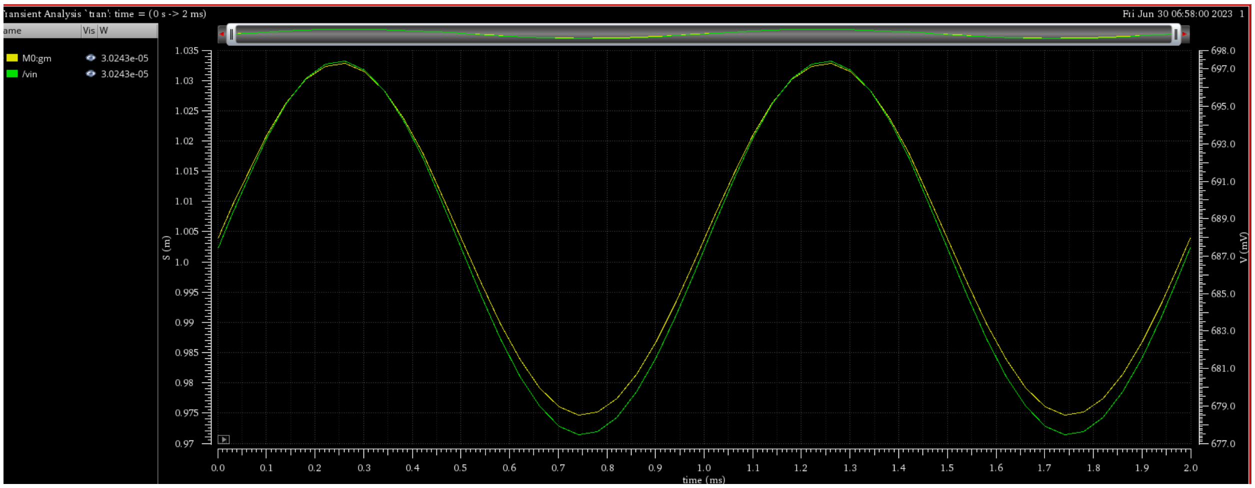


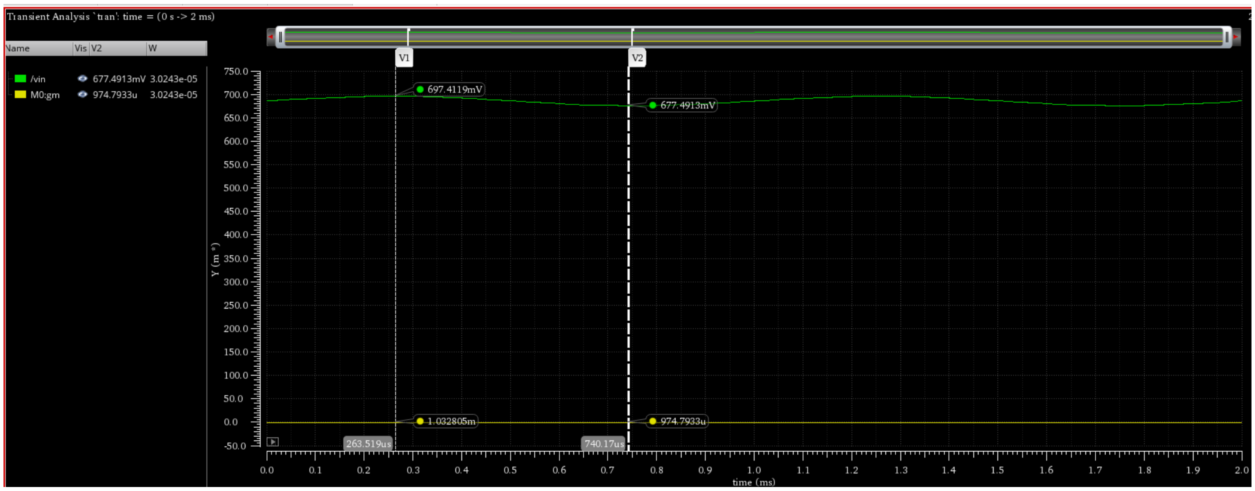
5 Create a new simulation configuration. Run transient simulation for 2ms. Plot gm vs time. Does gm vary with the input signal? What does that mean?





gm vs time





Yes, gm varies with the input signal, as it is the slope of id vs Vgs (vin) , so when the input signal oscillates it changes gm with it, **<u>so the gain is not constant as gain = gm *Rout</u>** , so the small signal linearization model is just an approximation as we consider gm a constant, but that small error is actually acceptable as gm change is very small and could be neglected.

6 IS THIS AMPLIFIER LINEAR? COMMENT.

NO , this amplifier 's not linear because the gain is not constant but depends on Vin, because the gain depends on gm and (gm = f(Vin)) and for linear gain, Av should not be f(Vin) but we can solve it by increasing the source resistance.