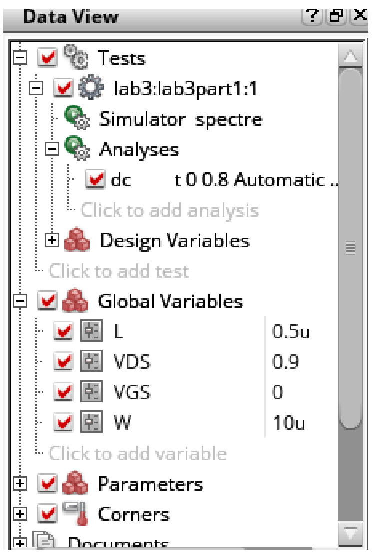
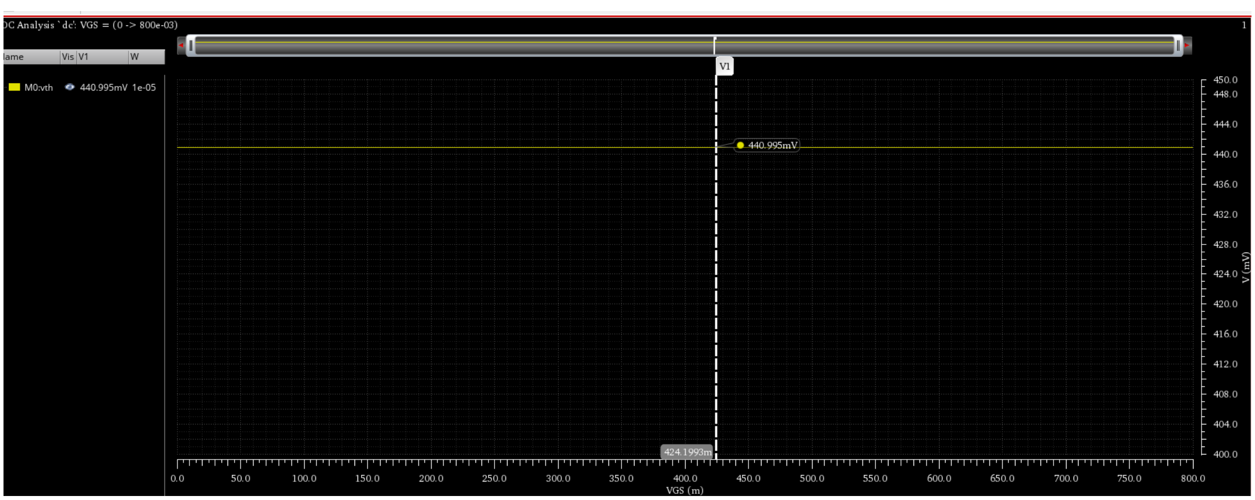
PART 1: Sizing Chart

1 Create a testbench for NMOS transistor as shown below (we will use NMOS only in this lab). Use $W = 10\mu m$ (we will understand why shortly) and $L = 0.5\mu m$ (the same L selected before) .

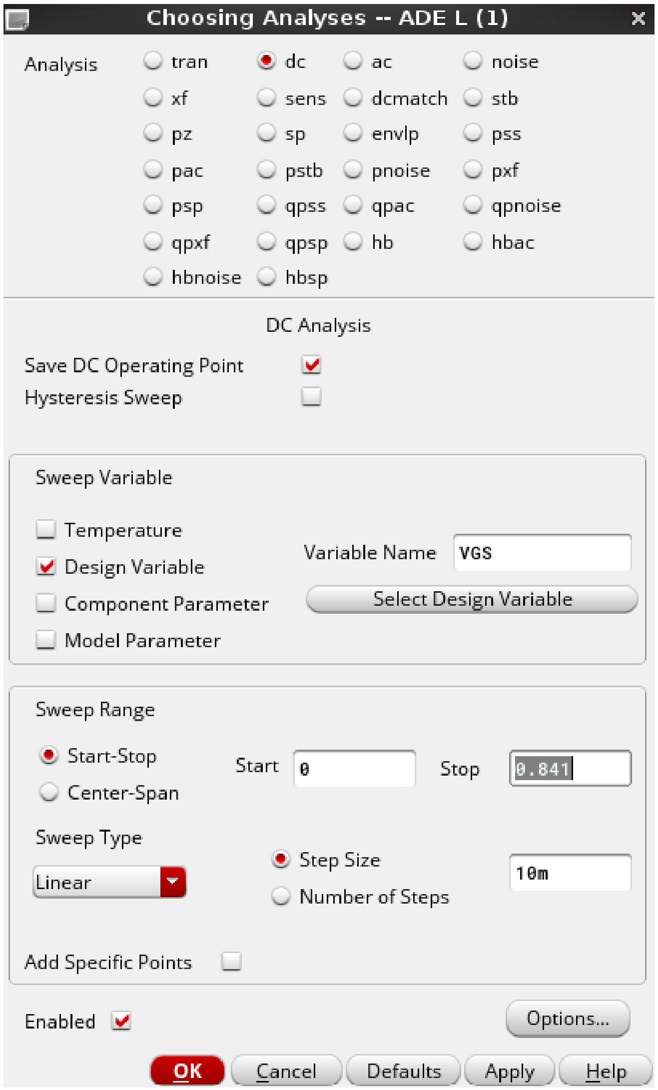


2 Sweep VGS from 0 to ≈ $VTH + 0.4V$ with 10mV step. Set $VDS = VDD/2$.



Vth for Nmos is ~ 441mv

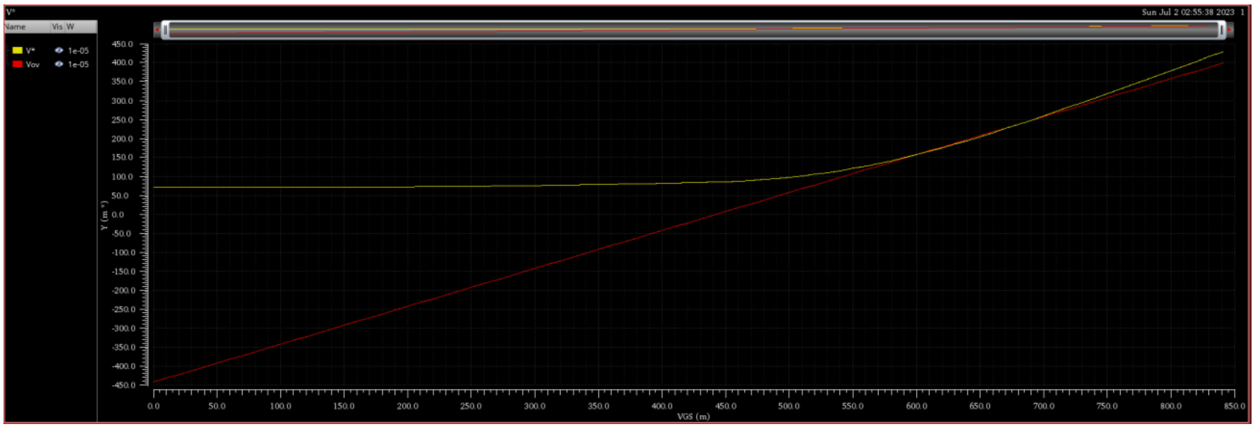
We well sweep VGS from 0 to ≈ 0.4 + 0.441 = 0.841v



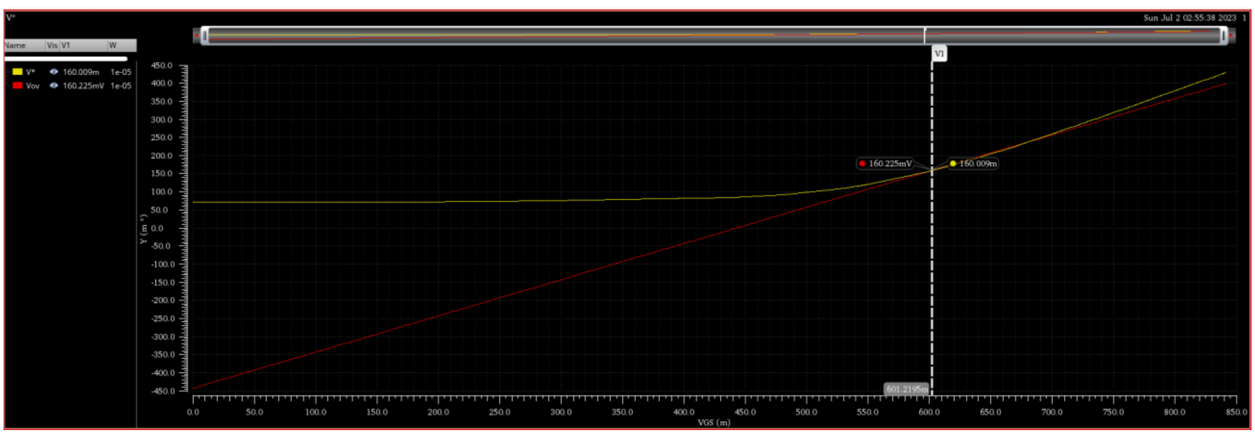
3 COMPARE $V* = 2ID/gm$ AND $Vov = VGS - VTH$ BY PLOTTING THEM OVERLAID. USE THE CALCULATOR TO CREATE EXPRESSIONS FOR $V*$ AND Vov. EXPORT THE EXPRESSIONS TO ADEXL.

Test	Name	Type	Details	EvalType	Plot	Save	Spec	Weight	Units	Digits	Notation	Suffix
lab3:lab		signal		point	☐	☐						
lab3:...	V*	expr	((2 * OS("/M0" "id")) /...	point	☑	☐						
lab3:...	Vov	expr	(OS("/M0" "vgs") - OS...	point	☑	☐						

4 Plot $V*$ and Vov overlaid vs VGS. Make sure the Y-axis of both curves has the same range.

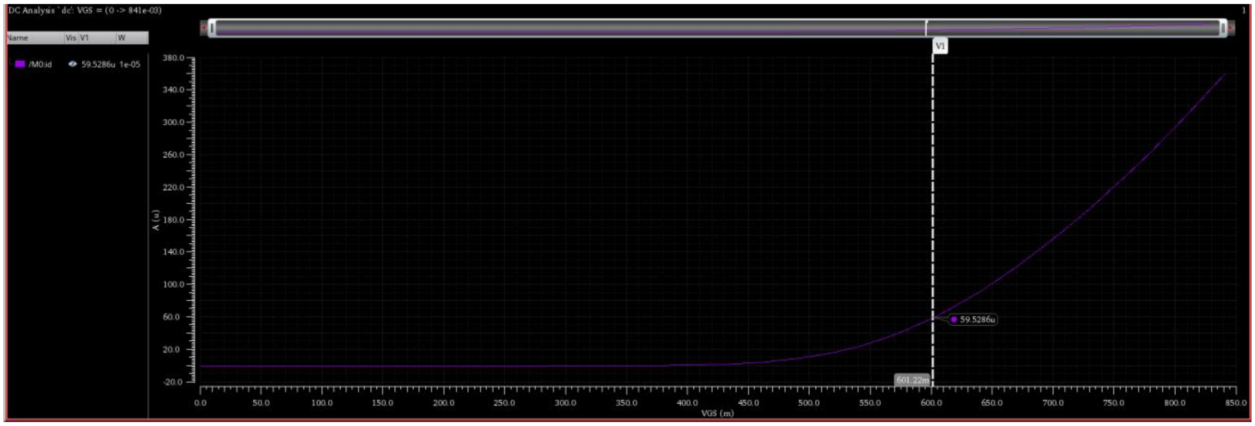


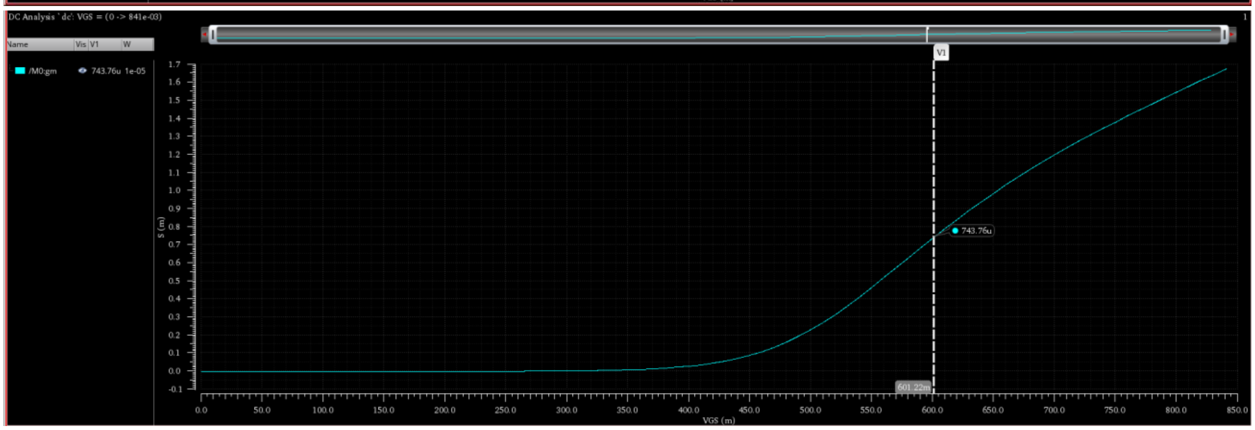
5 On the $V*$ and Vov chart locate the point at which $V* = VQ*$. Find the corresponding $VovQ$ and $VGSQ$ (Use V* = 160 mV).

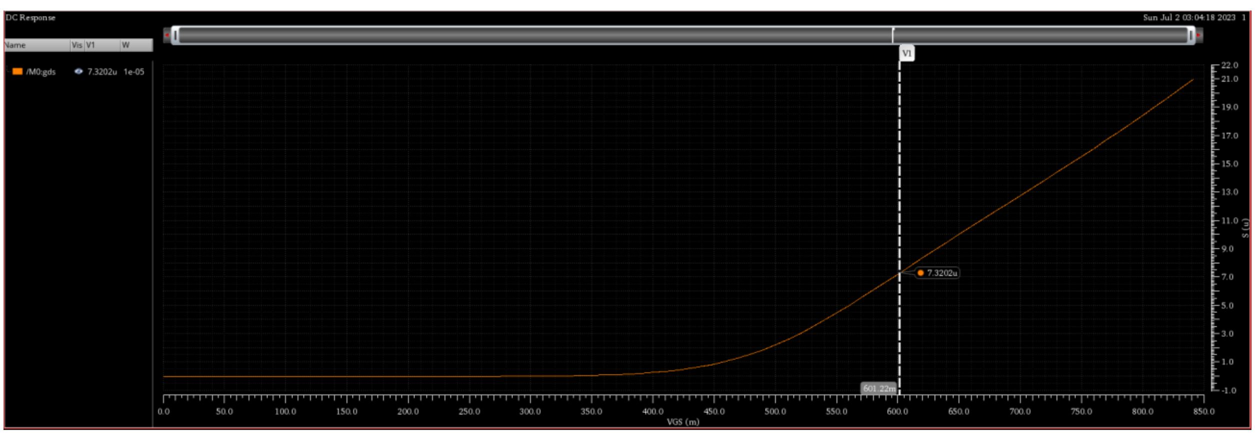


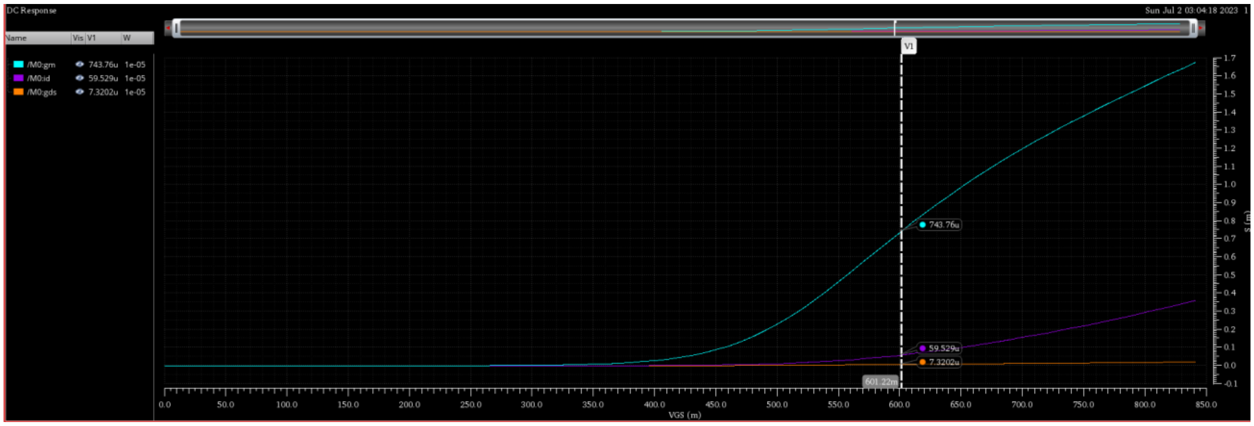
Vovq =160.225m && VGSq=601.22m

6 Plot ID, gm, and gds vs VGS. Find their values at $VGSQ$. Let's name these values IDX, gmX, and $gdsX$.









IDX =59.529 uA, gmX=743.76 u, $gdsX$=7.3202 u

7 CALCULATE **W**

$$Wnmos = \frac{10\mathrm{u} * 15\mathrm{u}}{59.529\mathrm{u}} = 2.51978 \sim 2.52u$$

- Use V* = 160 mV and ID = 15 uA.

8 CALCULATE gmQ AND $gdsQ$ USING RATIO AND PROPORTION

$$gmq(nmos) = \frac{2.52u * 743.76\mathrm{u}}{10\mathrm{u}} = 187.42u$$

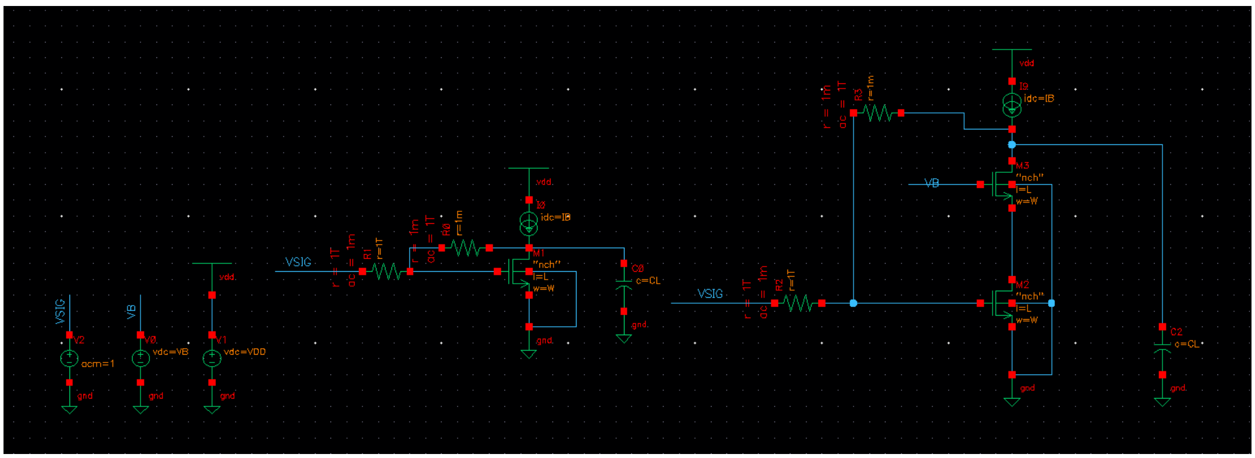
$$gdsq(nmos) = \frac{2.52u * 7.3202\,u}{10u} = 1.844u$$

PART 2: CS Amplifier

OP Analysis

1 CREATE A NEW CELL AND SCHEMATIC. CONSTRUCT THE CIRCUIT SHOWN BELOW. USE $IB = \cancel{20}\ (15)\ \mu A$, $L = 0.5\mu m$, W AS SELECTED IN PART 1, AND $CL = 1pF$.

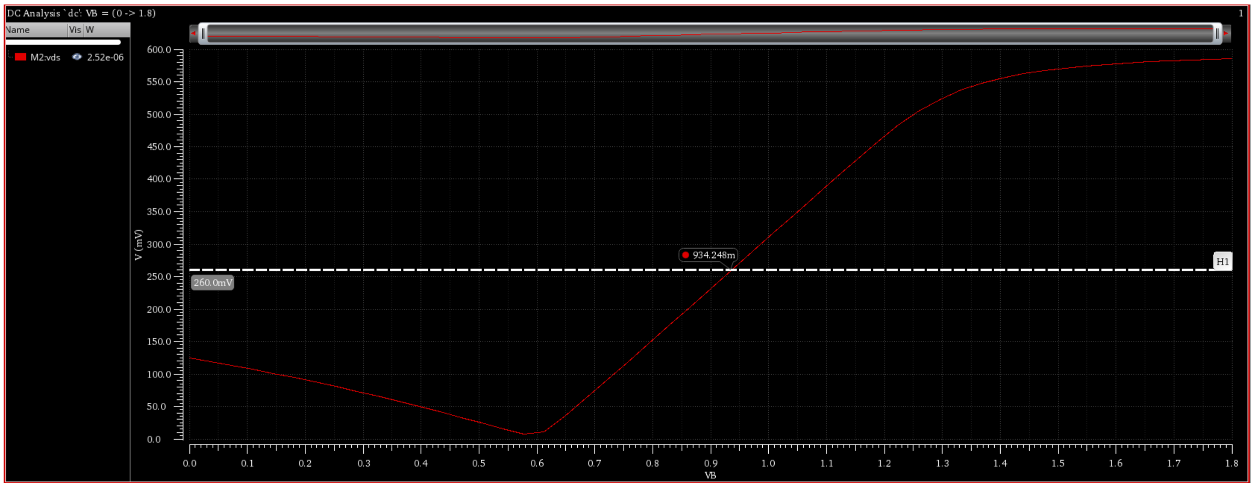
- Use V* = 160 mV and ID = 15 uA.



Global Variables

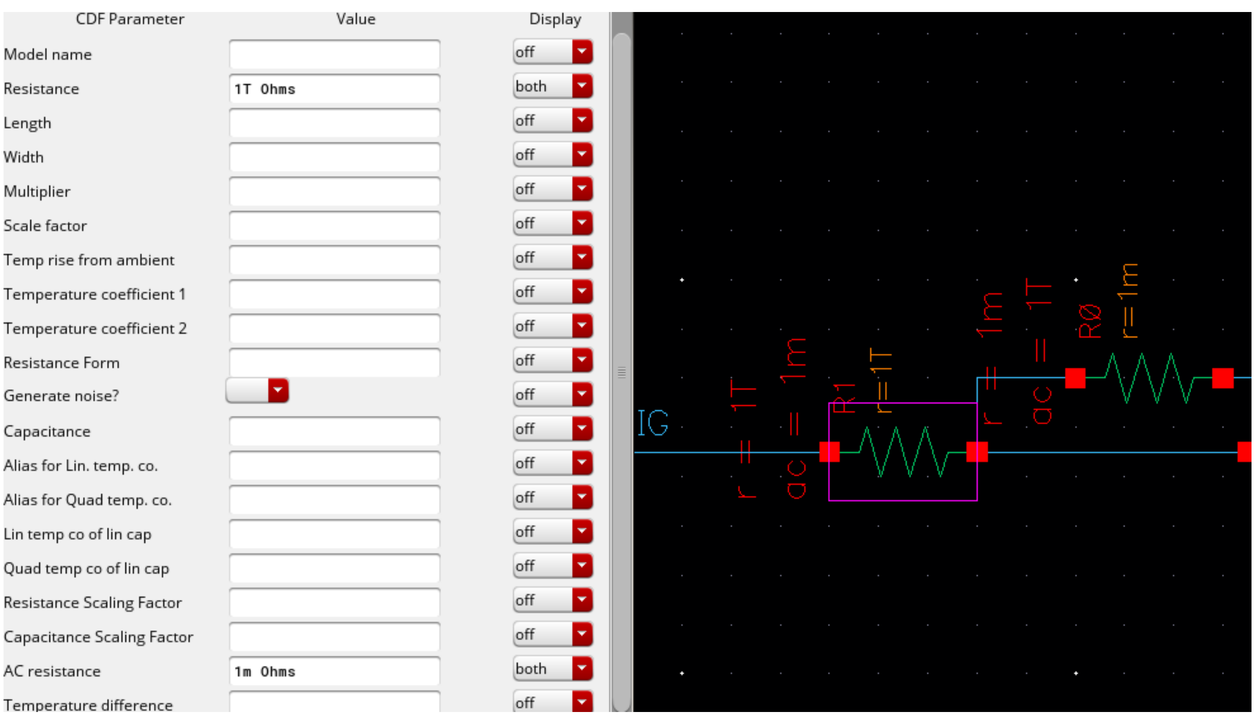
CL	1p
IB	15u
L	0.5u
VB	0
VDD	1.8
W	2.52u

2 CHOOSE VB (THE CASCODE DEVICE BIAS VOLTAGE) SUCH THAT M2 HAS $VDS \approx V* + 100mV$ (YOU MAY SWEEP VB AND PLOT VDS VS VB TO HELP YOU CHOOSE A GOOD VALUE FOR VB).

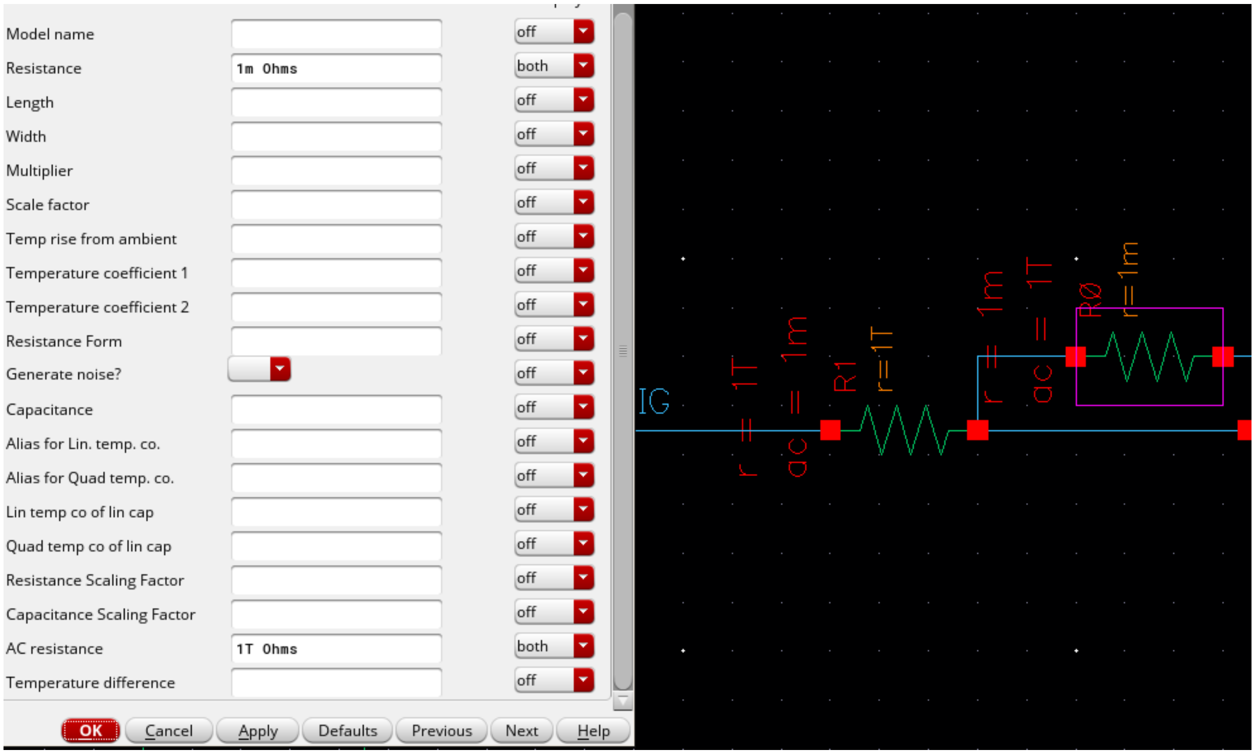


VB=934.248m

3 BIAS TRANSISTORS IN SATURATION



input resistance 1T DC and 1m AC

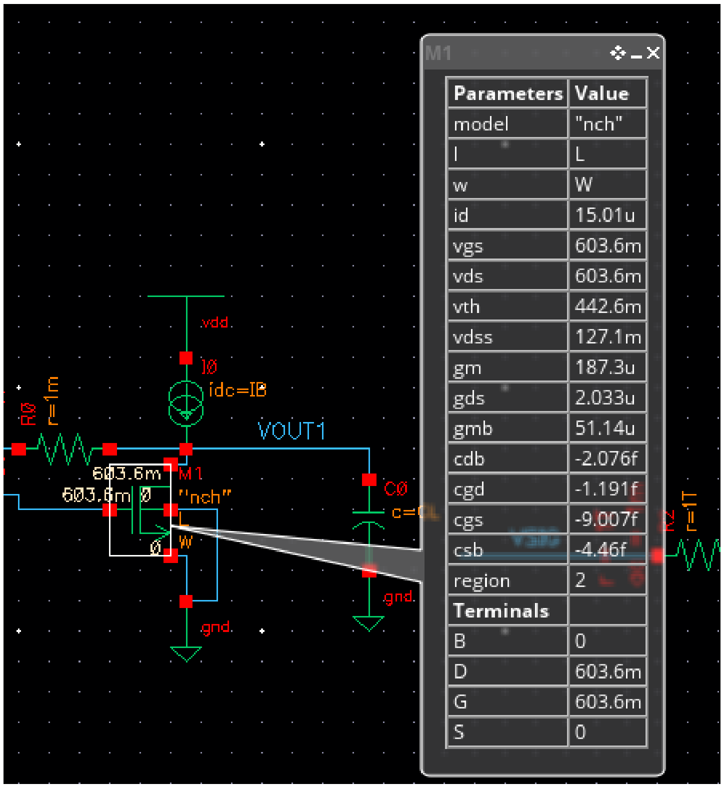


feedback resistance 1m DC and 1T AC

4 Simulate the DC OP point of the above CS and cascode amplifiers. Report a snapshot showing the following parameters for M1, M2 and M3 in addition to DC node voltages clearly annotated

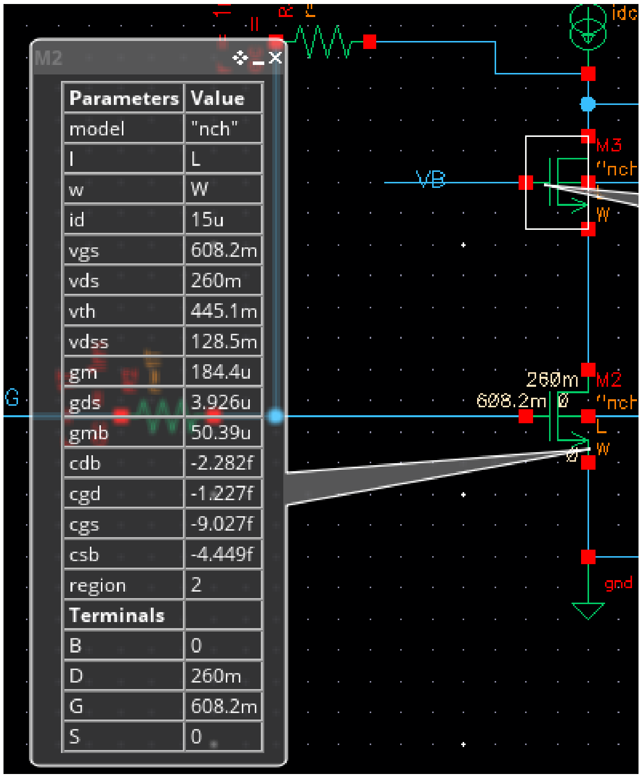
4.1 M1

lab3:lab3part2:1	ID_M1	15.01u			
lab3:lab3part2:1	VGS_M1	603.6m			
lab3:lab3part2:1	VDS_M1	603.6m			
lab3:lab3part2:1	VTH_M1	442.6m			
lab3:lab3part2:1	VDSAT_M1	127.1m			
lab3:lab3part2:1	GM_M1	187.3u			
lab3:lab3part2:1	GDS_M1	2.033u			
lab3:lab3part2:1	GMB_M1	51.14u			
lab3:lab3part2:1	CDB_M1	-2.076f			
lab3:lab3part2:1	CGD_M1	-1.191f			
lab3:lab3part2:1	CGS_M1	-9.007f			
lab3:lab3part2:1	CSB_M1	-4.46f			
lab3:lab3part2:1	Region_M1	2			



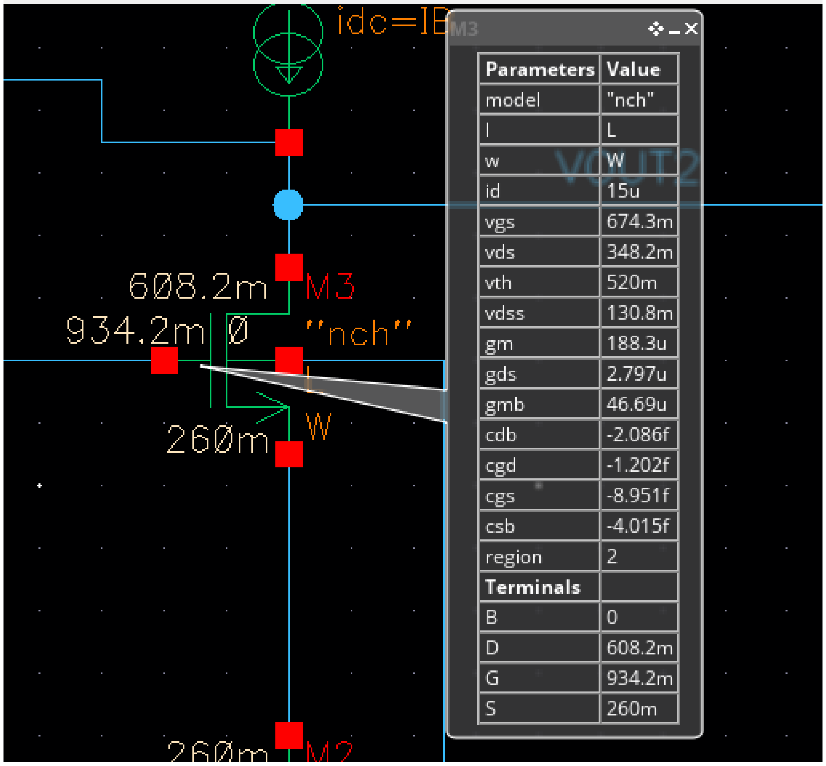
4.2 M2

lab3:lab3part2:1	ID_M2	15u			
lab3:lab3part2:1	VDS_M2	260m			
lab3:lab3part2:1	VTH_M2	445.1m			
lab3:lab3part2:1	VDSAT_M2	128.5m			
lab3:lab3part2:1	GM_M2	184.4u			
lab3:lab3part2:1	GDS_M2	3.926u			
lab3:lab3part2:1	GMB_M2	50.39u			
lab3:lab3part2:1	CDB_M2	-2.282f			
lab3:lab3part2:1	CGD_M2	-1.227f			
lab3:lab3part2:1	CGS_M2	-9.027f			
lab3:lab3part2:1	CSB_M2	-4.449f			
lab3:lab3part2:1	VGS_M2	608.2m			
lab3:lab3part2:1	Region_m2	2			



4.3 M3

lab3:lab3part2:1	ID_M3	15u			
lab3:lab3part2:1	VGS_M3	674.3m			
lab3:lab3part2:1	VDS_M3	348.2m			
lab3:lab3part2:1	VTH_M3	520m			
lab3:lab3part2:1	VDSAT_M3	130.8m			
lab3:lab3part2:1	GM_M3	188.3u			
lab3:lab3part2:1	GDS_M3	2.797u			
lab3:lab3part2:1	GMB_M3	46.69u			
lab3:lab3part2:1	CDB_M3	-2.086f			
lab3:lab3part2:1	CGD_M3	-1.202f			
lab3:lab3part2:1	CGS_M3	-8.951f			
lab3:lab3part2:1	CSB_M3	-4.015f			
lab3:lab3part2:1	Region_M3	2			



5 CHECK THAT ALL TRANSISTORS OPERATE IN SATURATION.

Cadence Hint: The "region" meaning is as follows: (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown).

Region is 2 in the three transistors, so they are all in saturation, or we can analysis it:

M1 : Vov = VGS – VTH = 161mV ,, VDS = 603.6mV So: VDS > Vov (SAT)
M2 : Vov = VGS – VTH = 163.1mV ,, VDS = 260mV So: VDS > Vov (SAT)
M3: Vov = VGS – VTH = 154.3mV ,, VDS = 348.2mV So: VDS > Vov (SAT)

6 DO ALL TRANSISTORS HAVE THE SAME VTH? WHY?

No, they don't have the same threshold voltage, because of body effect as they don't have the same V_{SB} .

7 WHAT IS THE RELATION (≪, <, =, >, ≫) BETWEEN GM AND GDS?

gm >> gds

8 WHAT IS THE RELATION ($\ll$, <, =, >, $\gg$) BETWEEN GM AND GMB?

gm > gmb

9 WHAT IS THE RELATION ($\ll$, <, =, >, $\gg$) BETWEEN CGS AND CGD?

CGS > CGD

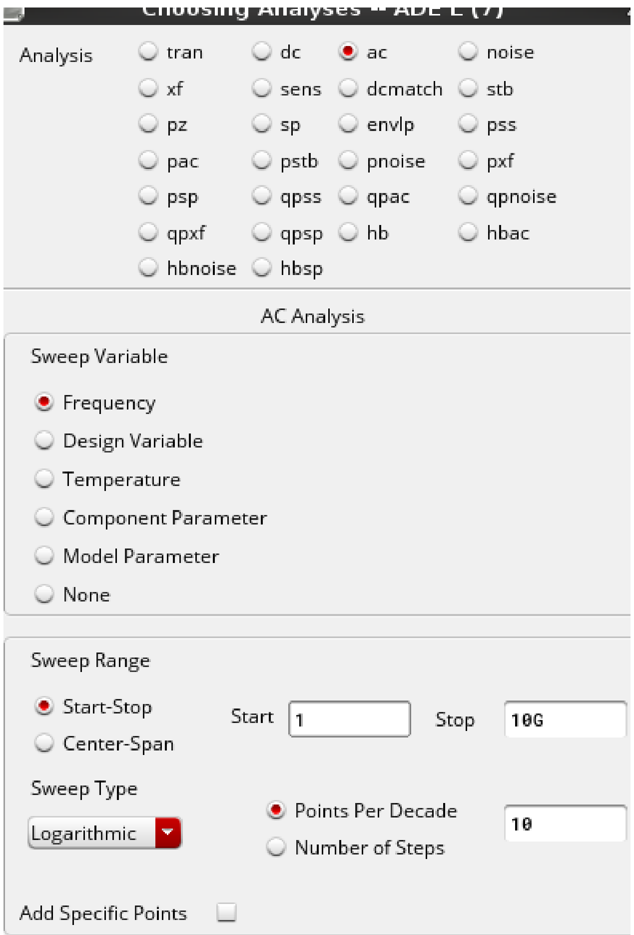
10 WHAT IS THE RELATION ($\ll$, <, =, >, $\gg$) BETWEEN CSB AND CDB?

CSB > CDB

WE TOOK ABSLUITE VALUES

AC Analysis

1 Create a new simulation configuration. Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.

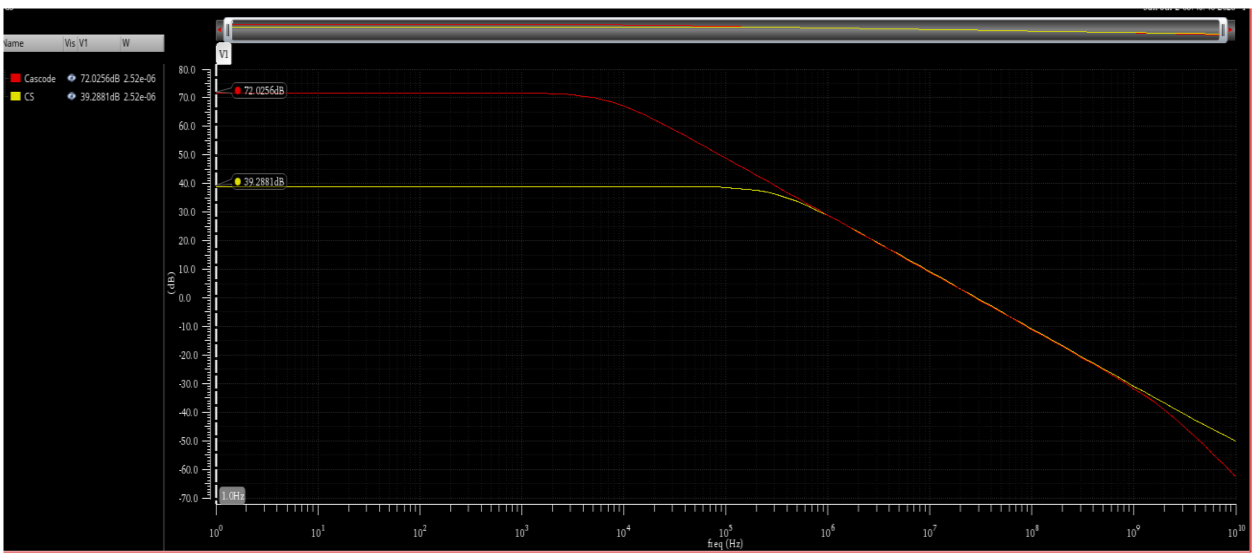


2 USE CALCULATOR TO CREATE EXPRESSIONS FOR CIRCUIT PARAMETERS (DC GAIN, BW, GBW, AND UGF) AND EXPORT THEM TO ADEXL.

lab3:lab3part2:1	dB20(VF("/VOUT1"))				
lab3:lab3part2:1	ymax(dB20(VF("/VOUT1")))	39.29			
lab3:lab3part2:1	ymax(mag(VF("/VOUT1")))	92.13			
lab3:lab3part2:1	bandwidth(VF("/VOUT1") 3 "l...	322k			
lab3:lab3part2:1	gainBwProd(VF("/VOUT1"))	29.74M			
lab3:lab3part2:1	dB20(VF("/VOUT2"))				
lab3:lab3part2:1	ymax(dB20(VF("/VOUT2")))	72.03			
lab3:lab3part2:1	ymax(mag(VF("/VOUT2")))	3.993k			
lab3:lab3part2:1	bandwidth(VF("/VOUT2") 3 "l...	7.211k			
lab3:lab3part2:1	gainBwProd(VF("/VOUT2"))	28.86M			

lab3:lab3part2:1	unityGainFreq(VF("/VOUT1"))	30M			
lab3:lab3part2:1	unityGainFreq(VF("/VOUT2"))	29.13M			

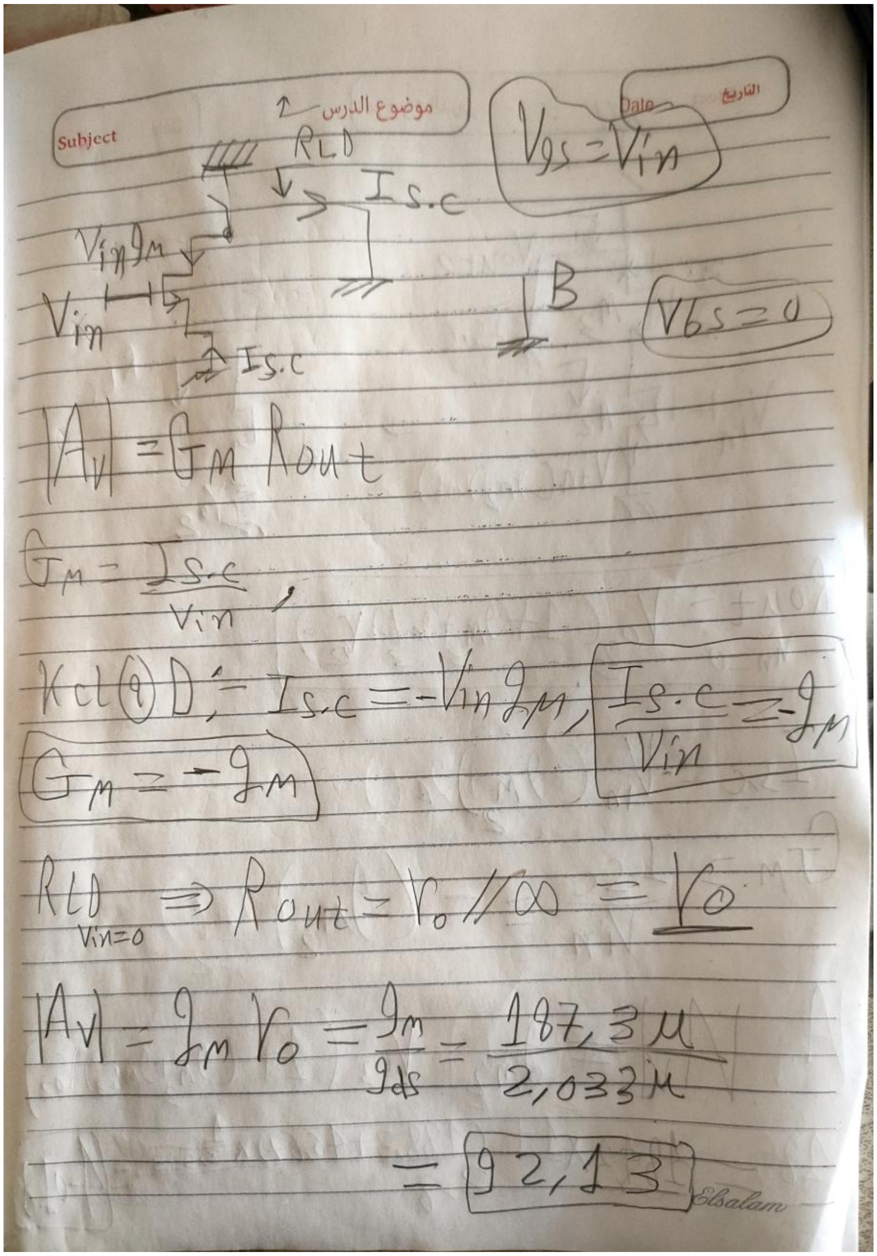
3 REPORT THE BODE PLOT (MAGNITUDE) OF CS AND CASCODE APPENDED ON THE SAME PLOT



4 USING SMALL SIGNAL PARAMETERS FROM OP SIMULATION, PERFORM HAND ANALYSIS TO CALCULATE DC GAIN, BW, AND GBW OF BOTH CIRCUITS.

- Ignore any requirement in the lab regarding the "analytical" calculation of the frequency response parameters.

In CS : **dc gain =gm*r0=**$\frac{gm}{gds}$=$\frac{187.3u}{2.033u}=\mathbf{92.13}$



$V_{gs} = V_{in}$

$V_{BS} = 0$

$|A_V| = G_M R_{out}$

$G_M = \frac{I_{s.c}}{V_{in}}$,

KCL @ D: $-I_{s.c} = -V_{in} g_m$, $\boxed{\frac{I_{s.c}}{V_{in}} = -g_m}$

$\boxed{G_M = -g_m}$

R_{LD} (Vin=0) $\Rightarrow R_{out} = r_o // \infty = \underline{r_o}$

$|A_V| = g_m r_o = \frac{g_m}{g_{ds}} = \frac{187,3\mu}{2,033\mu}$

$= \boxed{92,13}$

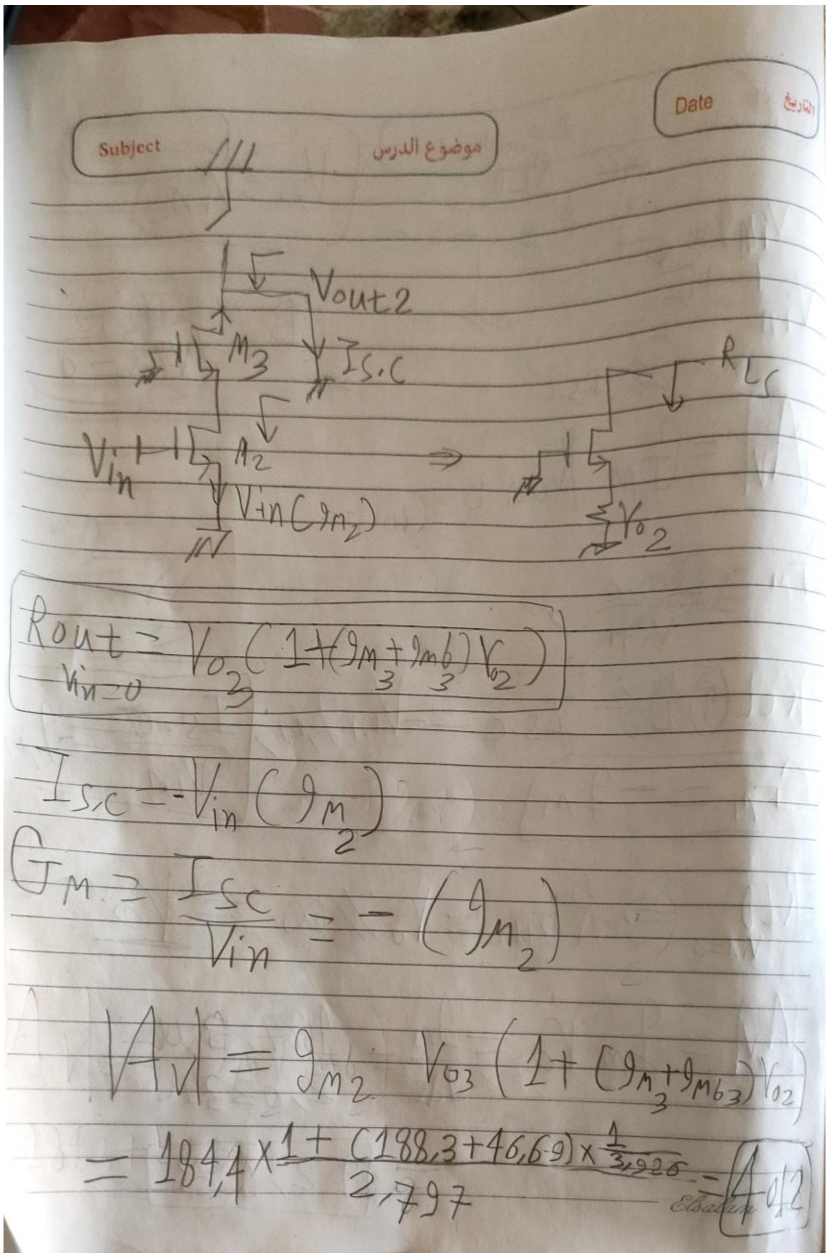
Elsalam

In Cascode : dc gain = Rout * GM

ROUT= r03(1+(gm3+gmb3)*r02) $=\frac{1}{2.797u}(1+(188.3u+46.69u)*\frac{1}{3.926u})=21.757\ \frac{1}{u}$

GM=- gm2=-184.4u

|Dc gain| = GM*ROUT= 184.4* 21.757 = 4012



5 REPORT A TABLE COMPARING THE DC GAIN, BW, UGF, AND GBW OF BOTH CIRCUITS FROM SIMULATION AND HAND ANALYSIS.

lab3:lab3part2:1	unityGainFreq(VF("/VOUT1"))	30M			
lab3:lab3part2:1	unityGainFreq(VF("/VOUT2"))	29.13M			

	Simulation		hand analysis.	
	CS	Cascode	CS	Cascode
DC GAIN	92.13	3993	92.13	4012
BW	322k	7.211k		
UGF	30M	29.13M		
GBW	29.74M	28.86M		

6 COMMENT ON THE RESULTS.

Dc gain in Cascode is much bigger than the gain in CS as it boosts Rout (Gm isn't boosted), and if we compared the hand analysis with the simulation results, we will see they are almost the same (error less than 1%).

Bw cs >> BW cascode , UGF cs > UGF cascode , GBW cs > GBW cascode.