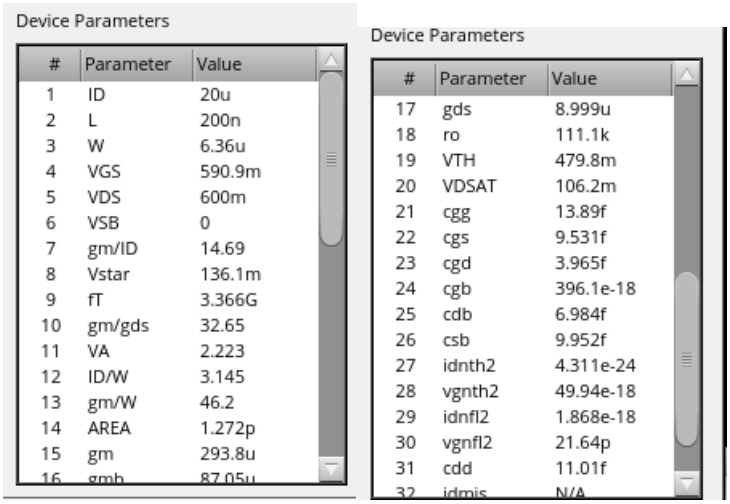
Part1 is not required as the doctor said.

PART2

1 DESIGN V1, INITIAL DESIGN OF OTA

1.1 INPUT PAIR



Device Parameters

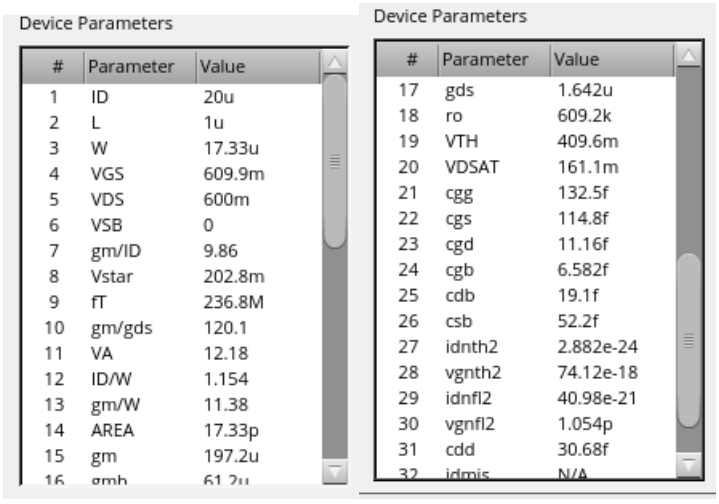
#	Parameter	Value
1	ID	20u
2	L	200n
3	W	6.36u
4	VGS	590.9m
5	VDS	600m
6	VSB	0
7	gm/ID	14.69
8	Vstar	136.1m
9	fT	3.366G
10	gm/gds	32.65
11	VA	2.223
12	ID/W	3.145
13	gm/W	46.2
14	AREA	1.272p
15	gm	293.8u
16	gmb	87.05u

Device Parameters

#	Parameter	Value
17	gds	8.999u
18	ro	111.1k
19	VTH	479.8m
20	VDSAT	106.2m
21	cgg	13.89f
22	cgs	9.531f
23	cgd	3.965f
24	cgb	396.1e-18
25	cdb	6.984f
26	csb	9.952f
27	idnth2	4.311e-24
28	vgnth2	49.94e-18
29	idnfl2	1.868e-18
30	vgnfl2	21.64p
31	cdd	11.01f
32	idmis	N/A

LIN=200n, WIN=6.36u

1.2 PMOS CURRENT SOURCE TRANSISTORS



Device Parameters

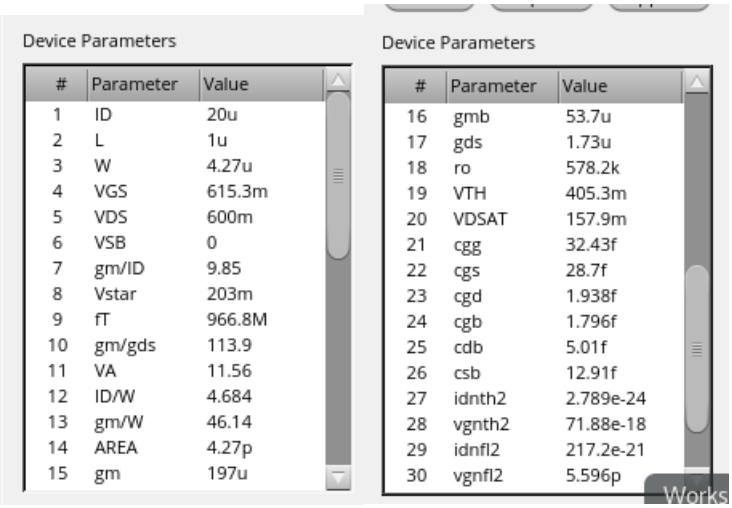
#	Parameter	Value
1	ID	20u
2	L	1u
3	W	17.33u
4	VGS	609.9m
5	VDS	600m
6	VSB	0
7	gm/ID	9.86
8	Vstar	202.8m
9	fT	236.8M
10	gm/gds	120.1
11	VA	12.18
12	ID/W	1.154
13	gm/W	11.38
14	AREA	17.33p
15	gm	197.2u
16	gmb	61.2u

Device Parameters

#	Parameter	Value
17	gds	1.642u
18	ro	609.2k
19	VTH	409.6m
20	VDSAT	161.1m
21	cgg	132.5f
22	cgs	114.8f
23	cgd	11.16f
24	cgb	6.582f
25	cdb	19.1f
26	csb	52.2f
27	idnth2	2.882e-24
28	vgnth2	74.12e-18
29	idnfl2	40.98e-21
30	vgnfl2	1.054p
31	cdd	30.68f
32	idmis	N/A

LSCP=1u, WSCP=17.33u

1.3 NMOS CURRENT SOURCE TRANSISTORS



Device Parameters

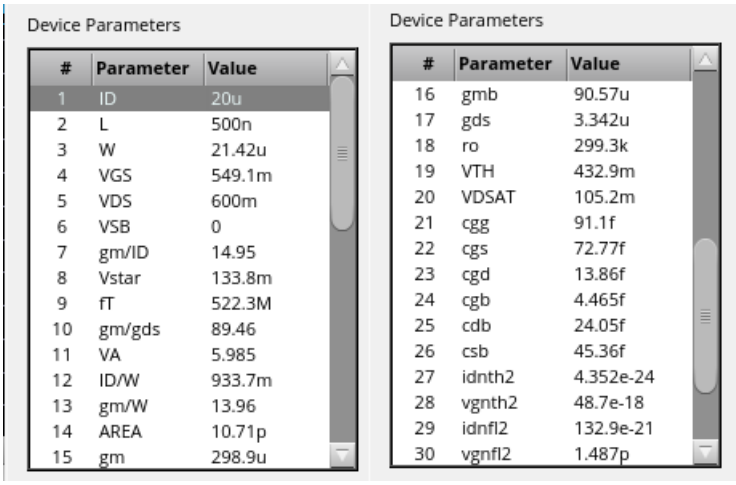
#	Parameter	Value
1	ID	20u
2	L	1u
3	W	4.27u
4	VGS	615.3m
5	VDS	600m
6	VSB	0
7	gm/ID	9.85
8	Vstar	203m
9	fT	966.8M
10	gm/gds	113.9
11	VA	11.56
12	ID/W	4.684
13	gm/W	46.14
14	AREA	4.27p
15	gm	197u

Device Parameters

#	Parameter	Value
16	gmb	53.7u
17	gds	1.73u
18	ro	578.2k
19	VTH	405.3m
20	VDSAT	157.9m
21	cgg	32.43f
22	cgs	28.7f
23	cgd	1.938f
24	cgb	1.796f
25	cdb	5.01f
26	csb	12.91f
27	idnth2	2.789e-24
28	vgnth2	71.88e-18
29	idnfl2	217.2e-21
30	vgnfl2	5.596p

LSCN=1u, WSCN=4.27u

1.4 CASCODE PMOS



Device Parameters

#	Parameter	Value
1	ID	20u
2	L	500n
3	W	21.42u
4	VGS	549.1m
5	VDS	600m
6	VSB	0
7	gm/ID	14.95
8	Vstar	133.8m
9	fT	522.3M
10	gm/gds	89.46
11	VA	5.985
12	ID/W	933.7m
13	gm/W	13.96
14	AREA	10.71p
15	gm	298.9u

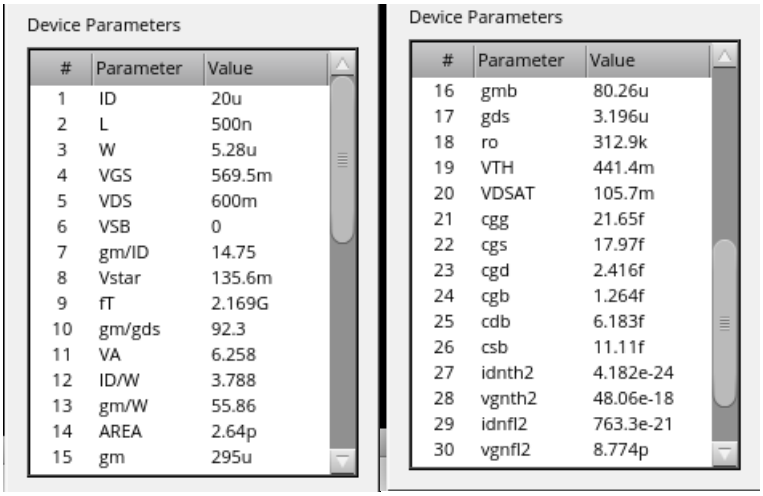
Device Parameters

#	Parameter	Value
16	gmb	90.57u
17	gds	3.342u
18	ro	299.3k
19	VTH	432.9m
20	VDSAT	105.2m
21	cgg	91.1f
22	cgs	72.77f
23	cgd	13.86f
24	cgb	4.465f
25	cdb	24.05f
26	csb	45.36f
27	idnth2	4.352e-24
28	vgnth2	48.7e-18
29	idnfl2	132.9e-21
30	vgnfl2	1.487p

LCASCODP= 500n

WCASCODP= 21.42u

1.5 CASCODE NMOS



Device Parameters

#	Parameter	Value
1	ID	20u
2	L	500n
3	W	5.28u
4	VGS	569.5m
5	VDS	600m
6	VSB	0
7	gm/ID	14.75
8	Vstar	135.6m
9	fT	2.169G
10	gm/gds	92.3
11	VA	6.258
12	ID/W	3.788
13	gm/W	55.86
14	AREA	2.64p
15	gm	295u

Device Parameters

#	Parameter	Value
16	gmb	80.26u
17	gds	3.196u
18	ro	312.9k
19	VTH	441.4m
20	VDSAT	105.7m
21	cgg	21.65f
22	cgs	17.97f
23	cgd	2.416f
24	cgb	1.264f
25	cdb	6.183f
26	csb	11.11f
27	idnth2	4.182e-24
28	vgnth2	48.06e-18
29	idnfl2	763.3e-21
30	vgnfl2	8.774p

LCASCODN= 500n

WCASCODN= 5.28u

1.6 INITAILY:

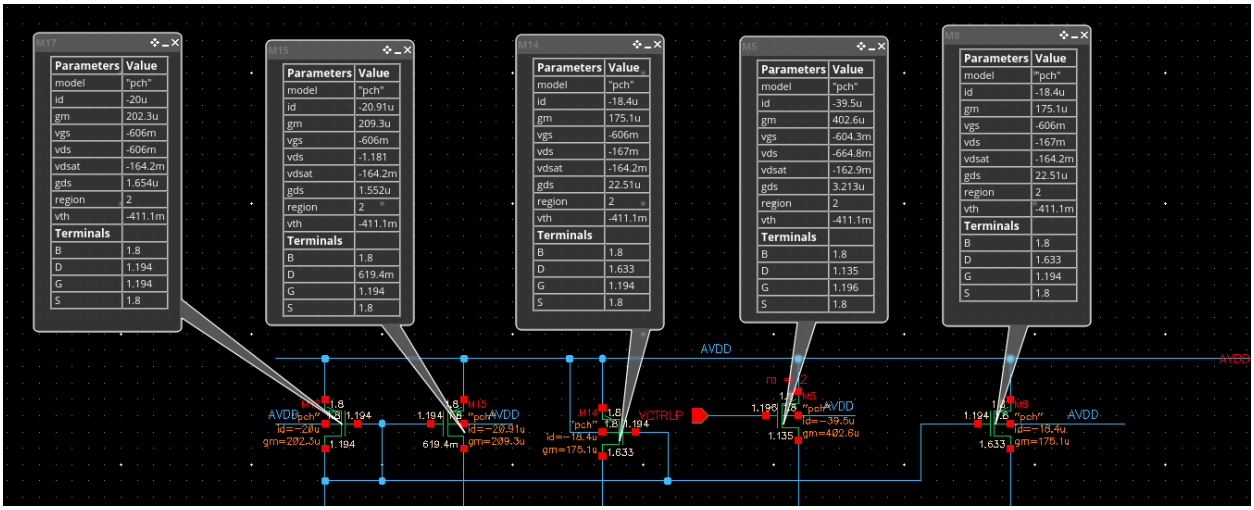
VCASN=vstar(NMOS cs) + vgs(NMOS cascode) = 772.5 m

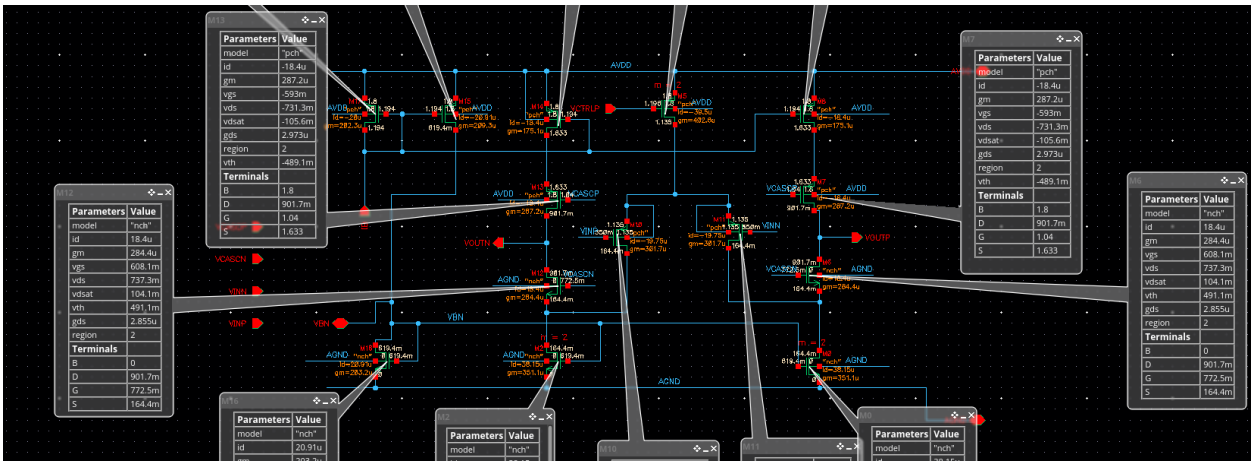
VCASP=vdd- vstar(PMOS cs) - vgs(PMOS cascode) =1.04

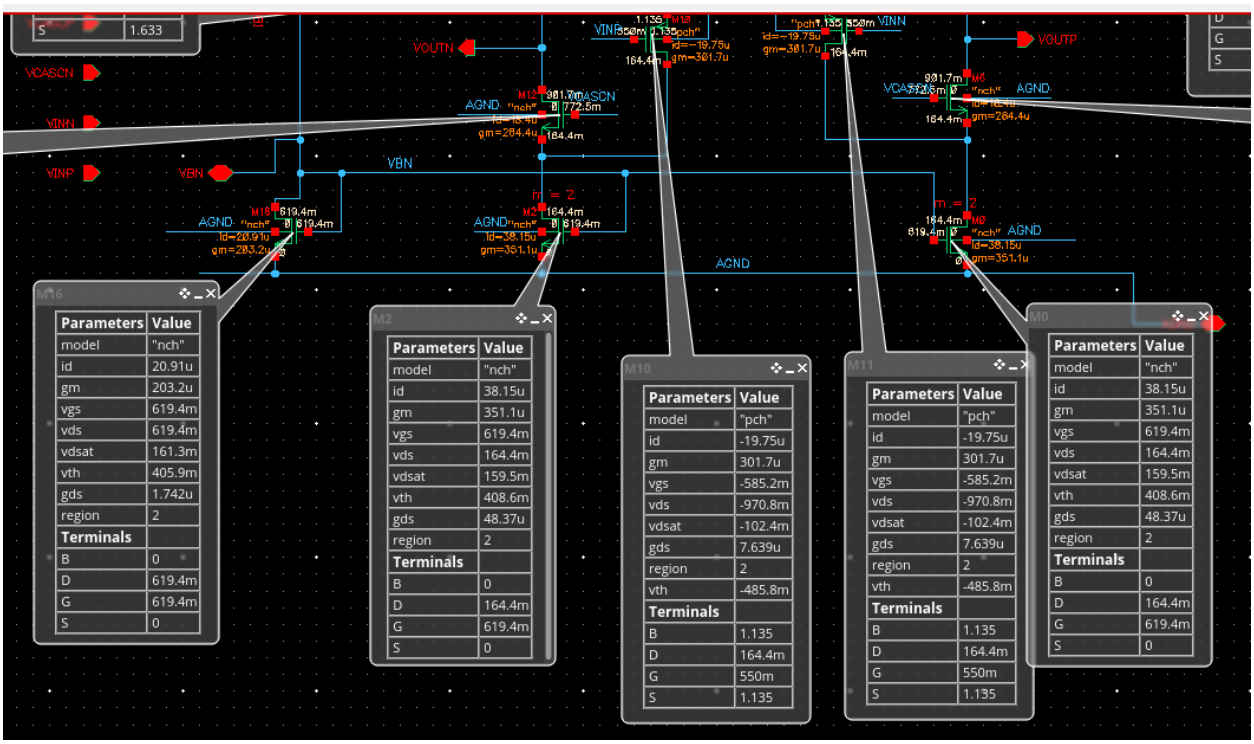
PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

1 DESIGN V2, TUNE THE INITIAL DESIGN

Dc op analysis:



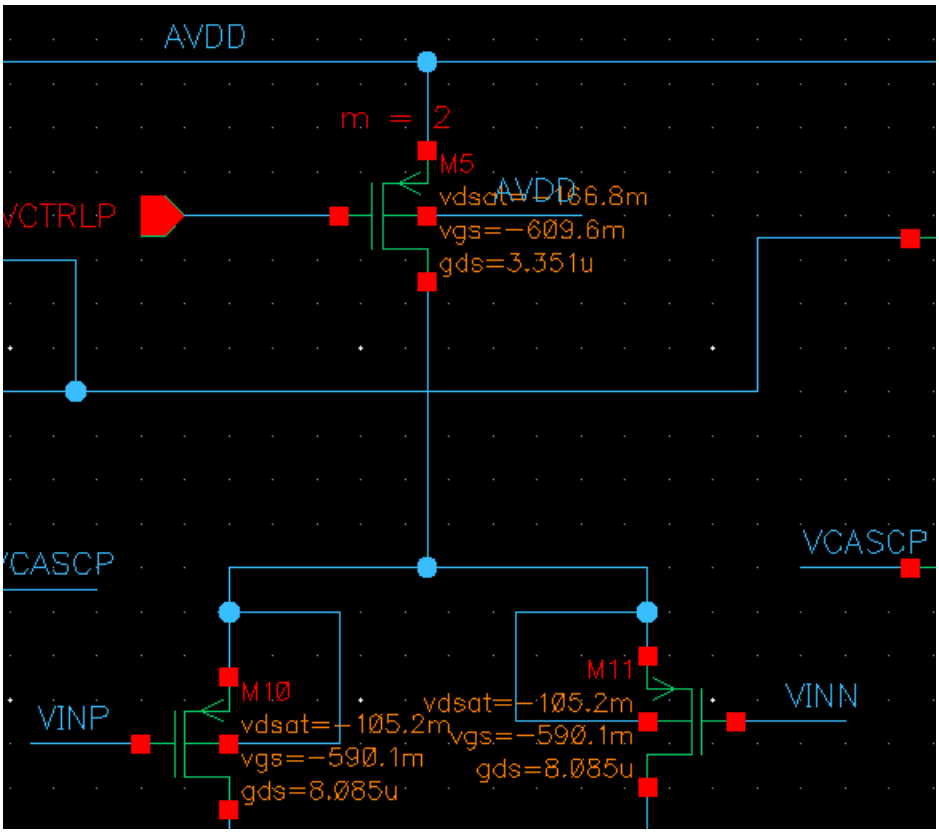




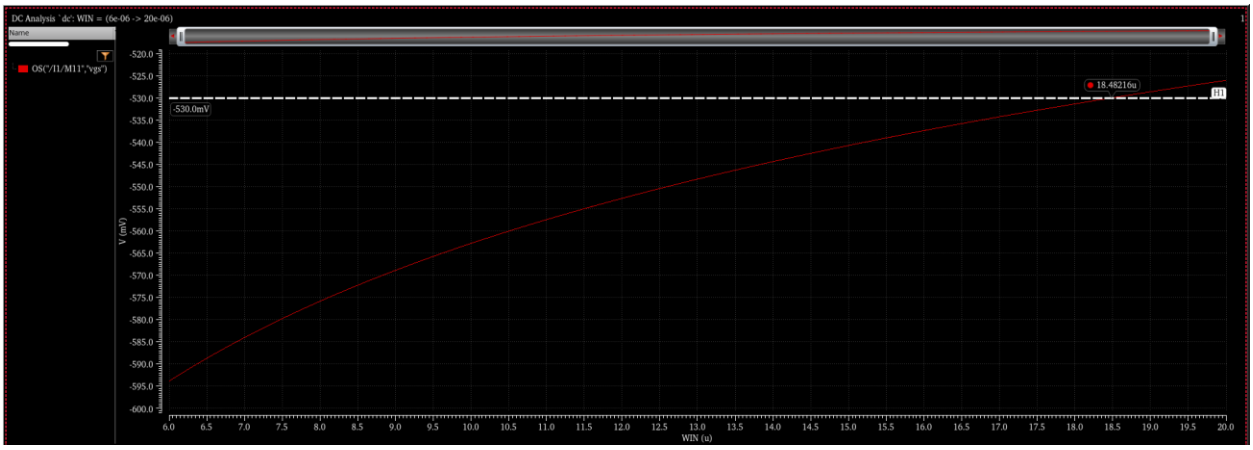
we need to increase Vcasn to equal VGSN + V* so 218m+608.1m=825mv ~ 850mv

Vcasdp=1.8-0.593-2*18.4/175.1=996.8m~990m.

Firstly: CM input range – high spec is violated

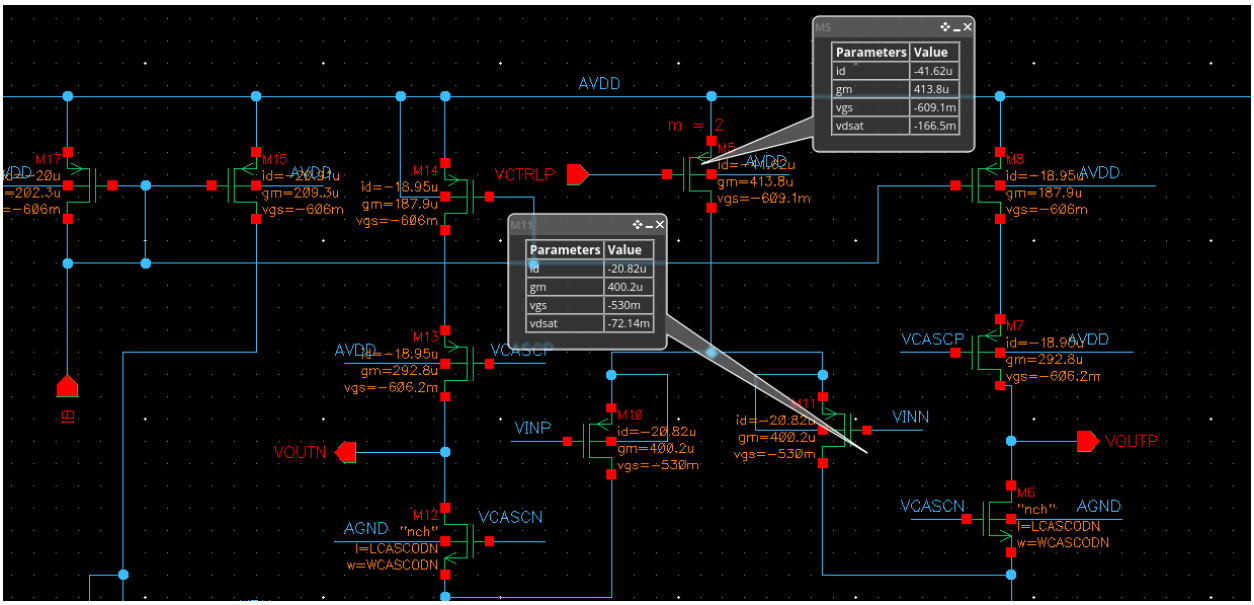


So we wants smaller vgs to achieve the high cmir spec 1.8-1.1-169m=531m ,we swept WIN to get vgs=530m



At the same time higher WIN wouldn’t only solve this violation but, also increasing the gain (gm) and GBW.

WIN=18.48u

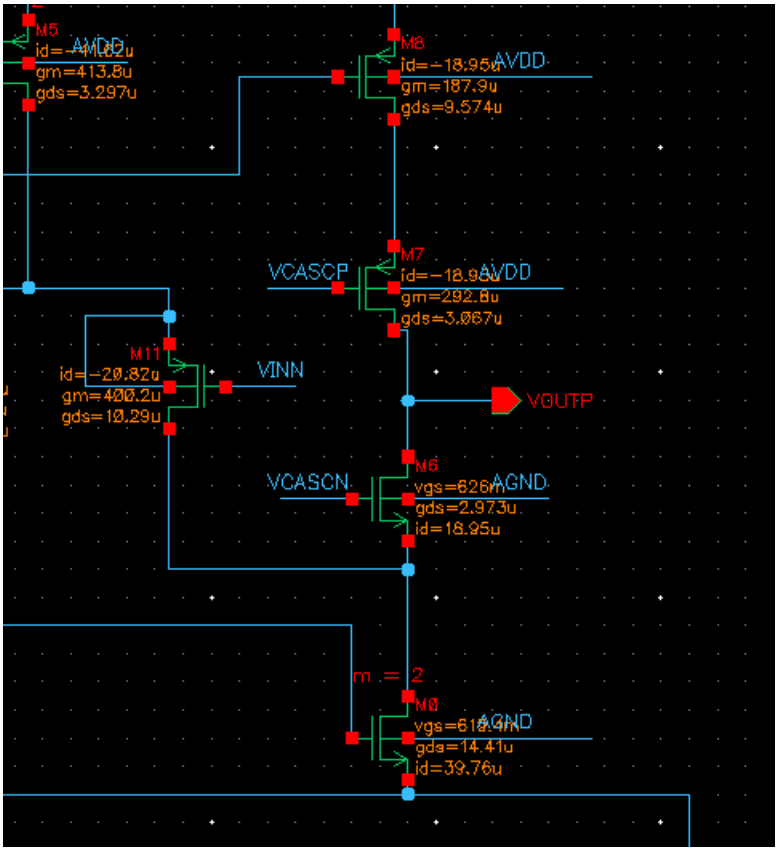


So now vicm (max) =1.8-530m-166.5m=1.103 mv

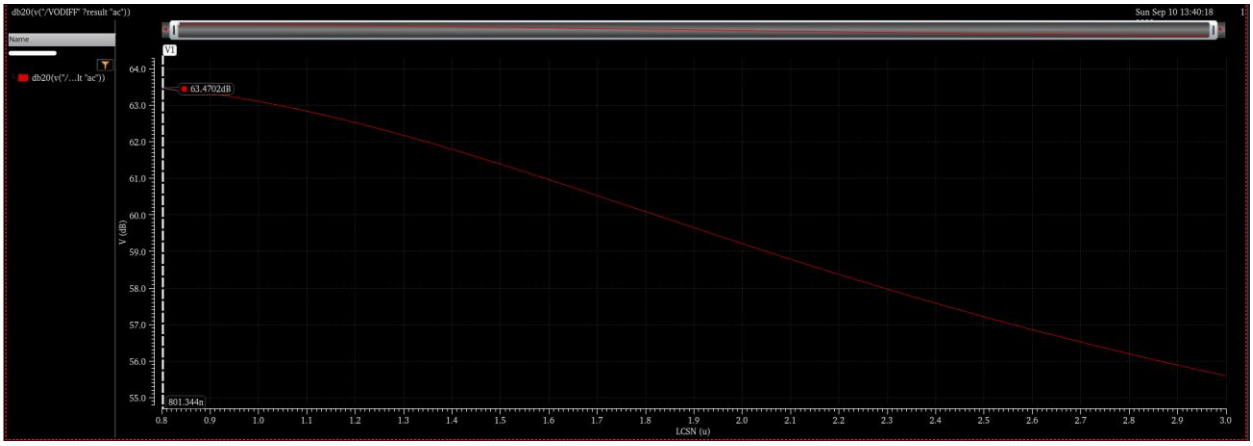
DOING AC ANALYSIS :

MINIPROJECT2_...	db20(v("/VODIFF...				
MINIPROJECT2_...	AO	1.43K			
MINIPROJECT2_...	AO_DB	63.11			
MINIPROJECT2_...	BW	40.16K			
MINIPROJECT2_...	FU	58.16M			
MINIPROJECT2_...	GBW	57.43M			

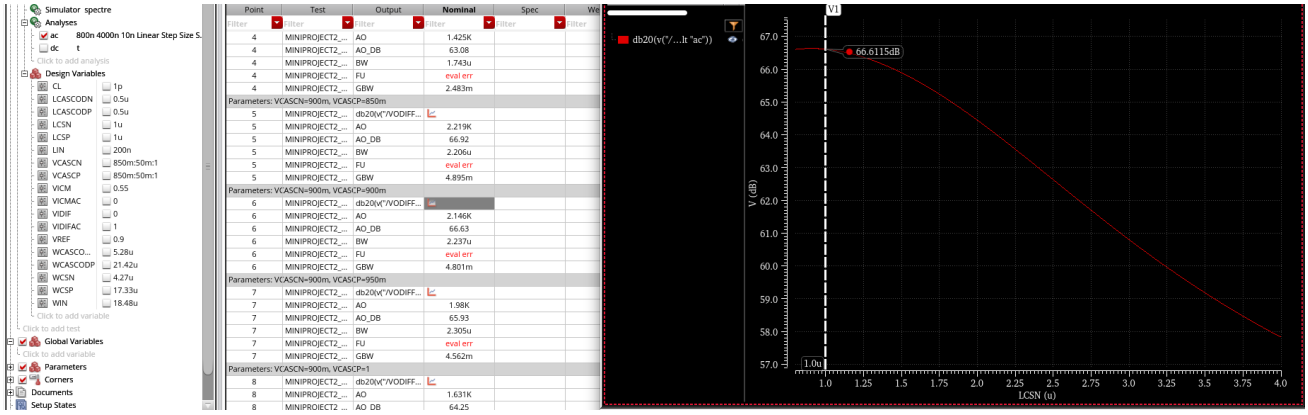
Gm is already very big, increasing it more would drive the transistor to WI so we would increase the gain by increasing ROUT.



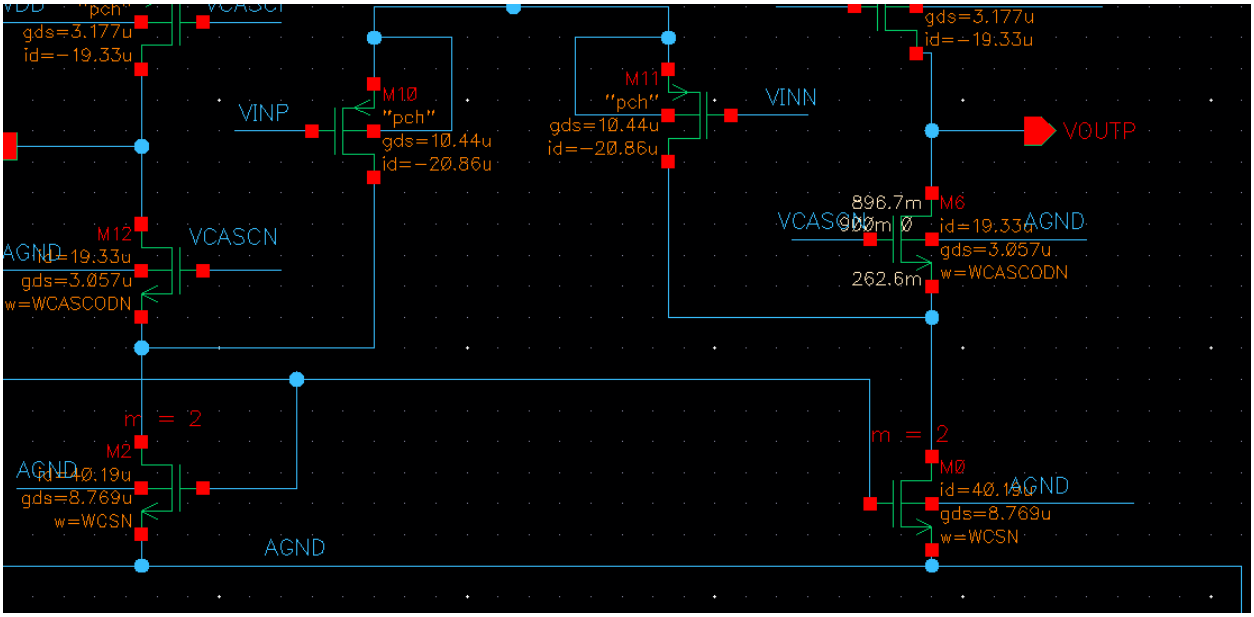
The biggest gds(dominant) is the nmos current source and pmos current source,



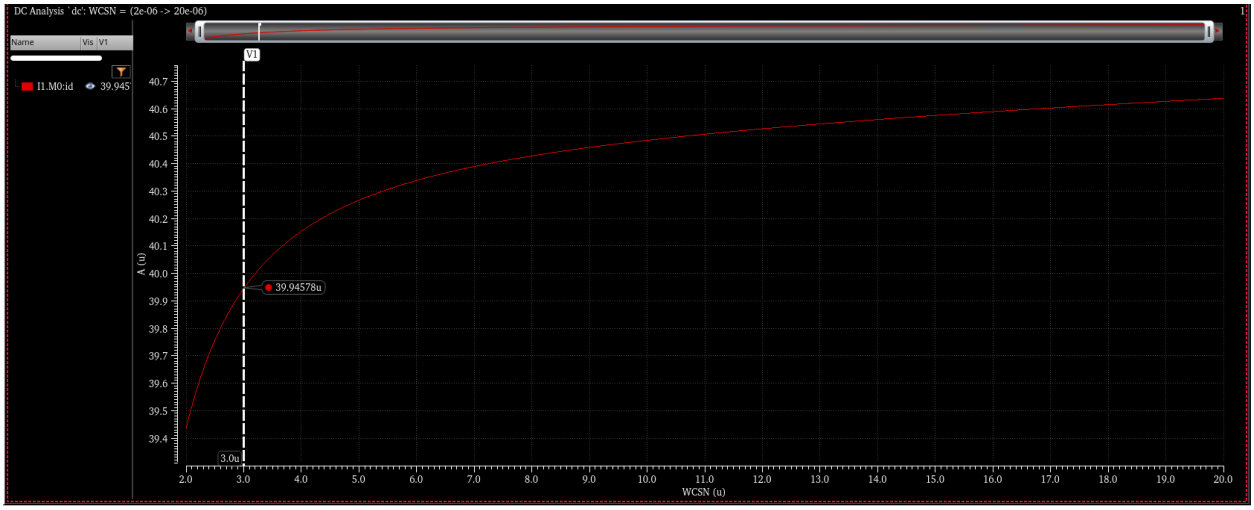
The problem is with the bias we should increase vds on this transistor and drive it deeper into saturation.



β=1/3, so we need at least gain=70db, we chose VCASCN=VCASCP=900m to get the same voltage from the same bias circuit, and we should look for the swing to not be violated.



The current consumption is bigger than 80u, so we need to adjust WCSN.



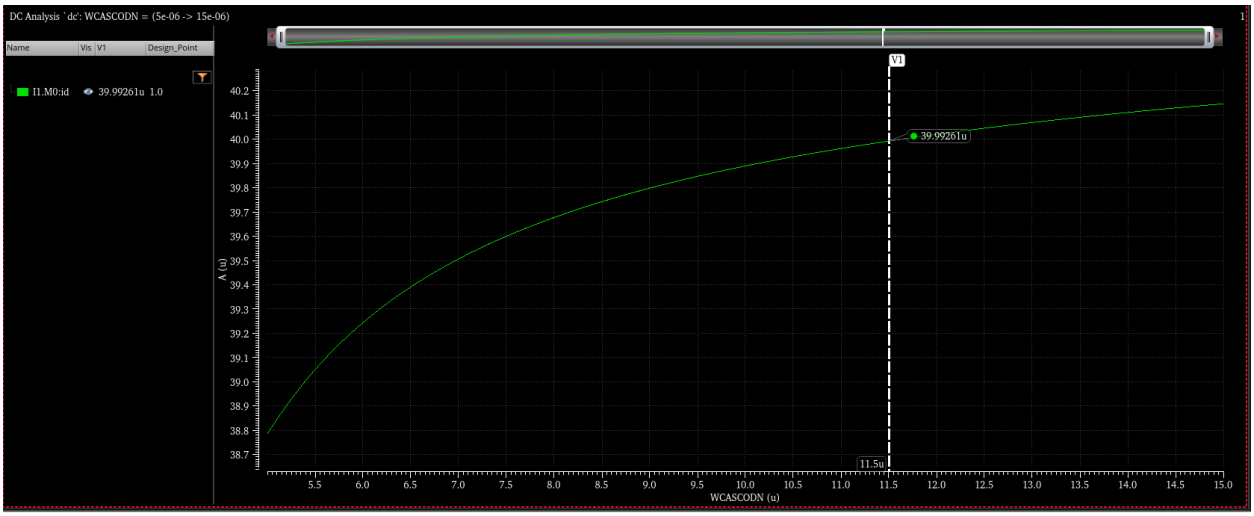
We chose the width to be 3.2u.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
MINIPROJECT2_...	db20(v("/VODIFF...				
MINIPROJECT2_...	AO	1.975K			
MINIPROJECT2_...	AO_DB	65.91			
MINIPROJECT2_...	BW	29.26K			
MINIPROJECT2_...	FU	58.41M			
MINIPROJECT2_...	GBW	57.81M			

To get less current, and to increase the gain, we would decrease Lcsn to 900n.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
MINIPROJECT2_...	db20(v("/VODIFF...				
MINIPROJECT2_...	AO	2.014K			
MINIPROJECT2_...	AO_DB	66.08			
MINIPROJECT2_...	BW	28.71K			
MINIPROJECT2_...	FU	58.42M			
MINIPROJECT2_...	GBW	57.84M			

WE need to maximize the gain as we can so we roughly increased Lcasdn 4 times, and swept the width with current, so we don’t violate it.

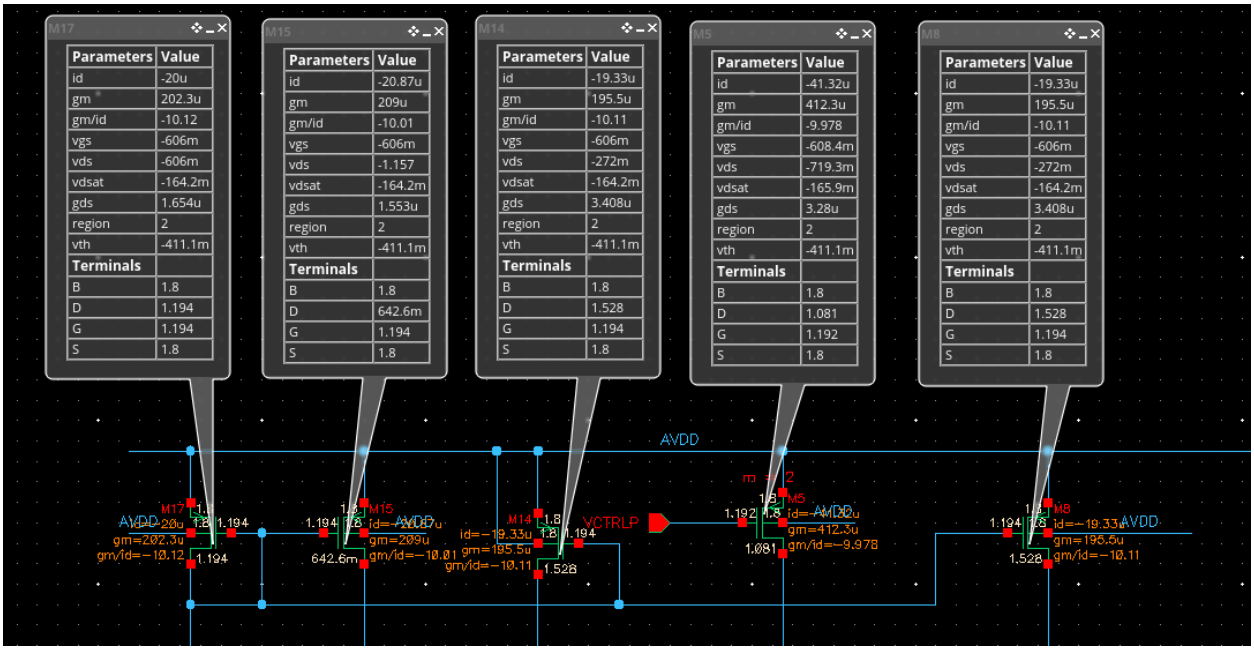


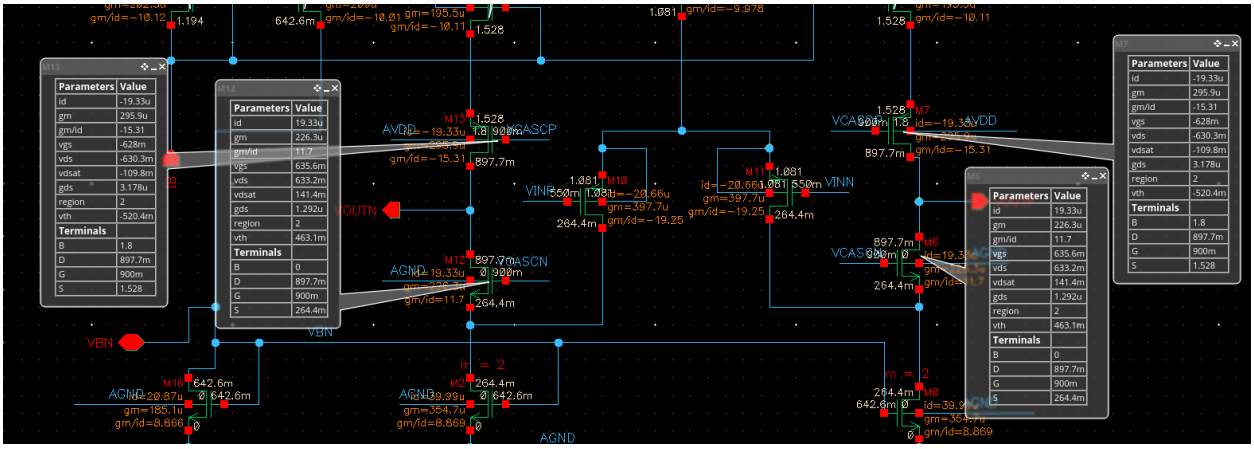
WCASDN=11.5u

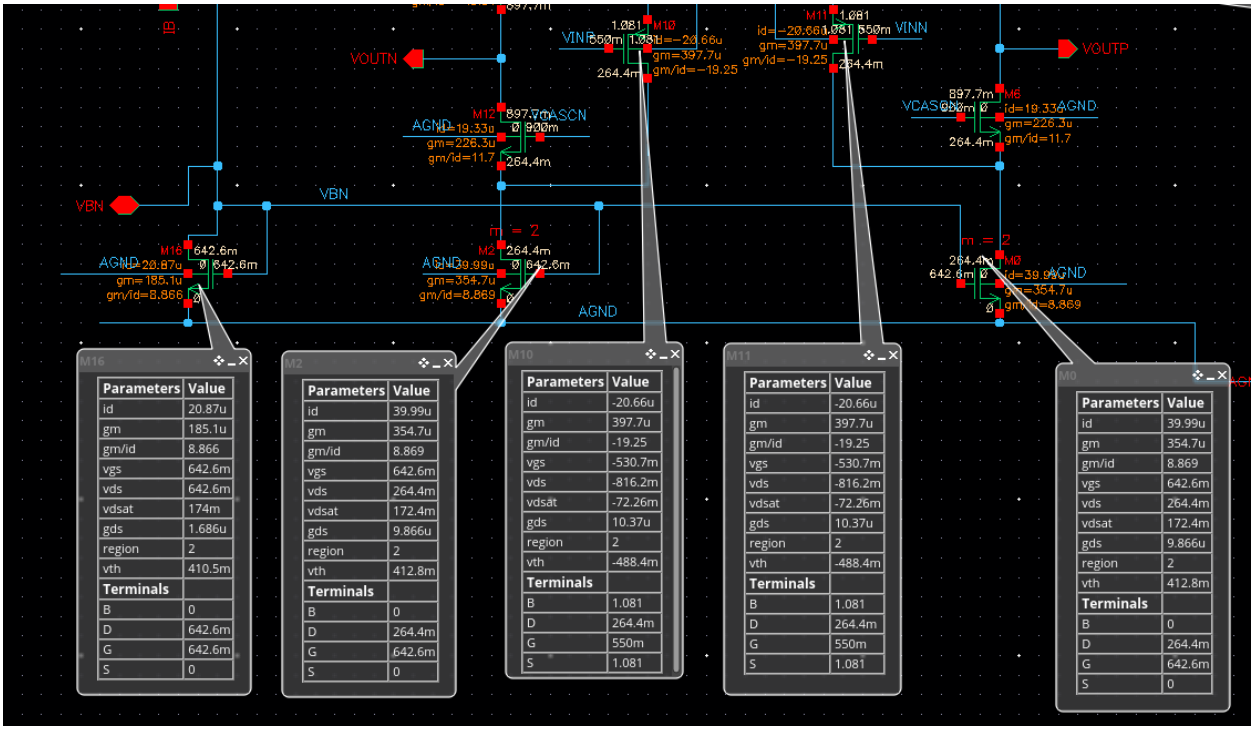
FIRST DESIGN meeting the specs:

Design Variables	
CL	1p
LCASCODN	2u
LCASCODP	0.5u
LCSN	900n
LCSP	1u
LIN	200n
VCASCN	900m
VCASCP	900m
VICM	0.55
VICMAC	0
VIDIF	0
VIDIFAC	1
VREF	900m
WCASCODN	11.5u
WCASCODP	21.42u
WCSN	3.2u
WCSP	17.33u
WIN	18.48u

2 SCHEMATIC OF THE OTA AND BIAS CIRCUIT WITH DC NODE VOLTAGES AND TRANSISTORS OP PARAMETERS (ID, VGS, VDS, VDSAT, VTH, GM, GDS, REGION) CLEARLY ANNOTATED.



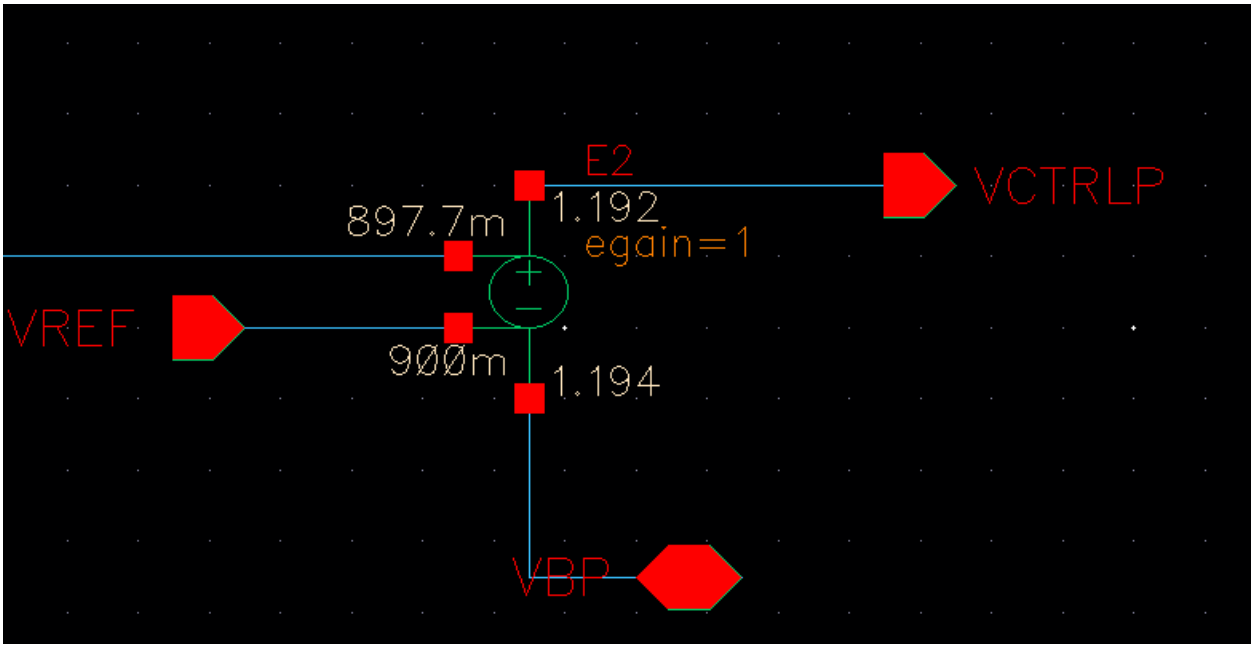




2.1 What is the CM level at the OTA output?

897.7mv

2.2 What are the differential input and output voltages of the error amplifier? What is the relation between them?



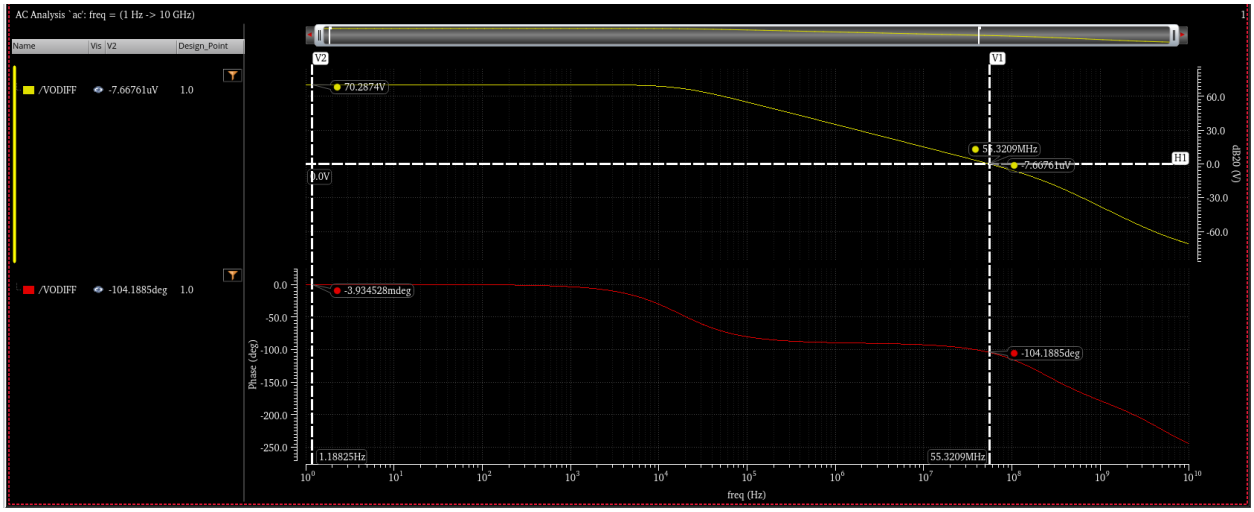
VID=900-897.7=2.3 mv

VOD=1.192-1.194=2 mv

The relation between them is the gain.

3 DIFF SMALL SIGNAL CCS:

3.1 PLOT DIFF GAIN (MAGNITUDE IN DB AND PHASE) VS FREQUENCY.



3.2 CALCULATE CIRCUIT PARAMETERS (DC GAIN, BW, GBW, UGF, AND PM)

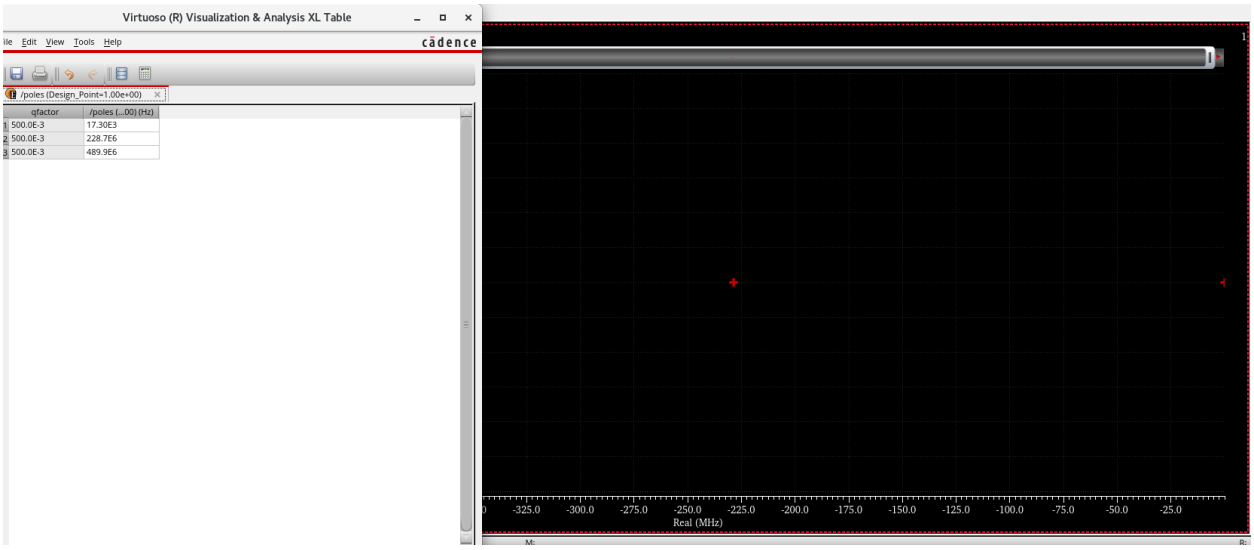
Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
MINIPROJECT2_...	A0	3.269K			
MINIPROJECT2_...	A0_DB	70.29			
MINIPROJECT2_...	BW	17.32K			
MINIPROJECT2_...	FU	55.7M			
MINIPROJECT2_...	GBW	56.62M			
MINIPROJECT2_...	/VODIFF_ac				

Pm from the bode blot above=180-104.2=75.8

3.3 COMPARE SIMULATION RESULTS WITH HAND CALCULATIONS IN A TABLE (USE SS PARAMETERS FROM OP SIMULATION IN YOUR HAND ANALYSIS).

	simulation	hand analysis
DC gain	70.29 db	$Av = gm * ROUT = gm_{11} * [ro_{m7}(gm_{m7} * r0_{m8})// ro_{m6}(gm_{m6} * (ro_{m0}//ro_{m11}))] = 2614 = 68.3db$ As expected, is less because of neglecting body effect
BW	17.32k	$\frac{1}{2\pi RoutC}$ =24k
GBW	56.62M	AV*BW=63M
UGF	55.7M	63M
PM	75.8 From pz analysis: 76.3	$90 - tan^{-1}(\frac{\omega_u}{\omega_{p2}}) = 74.5$

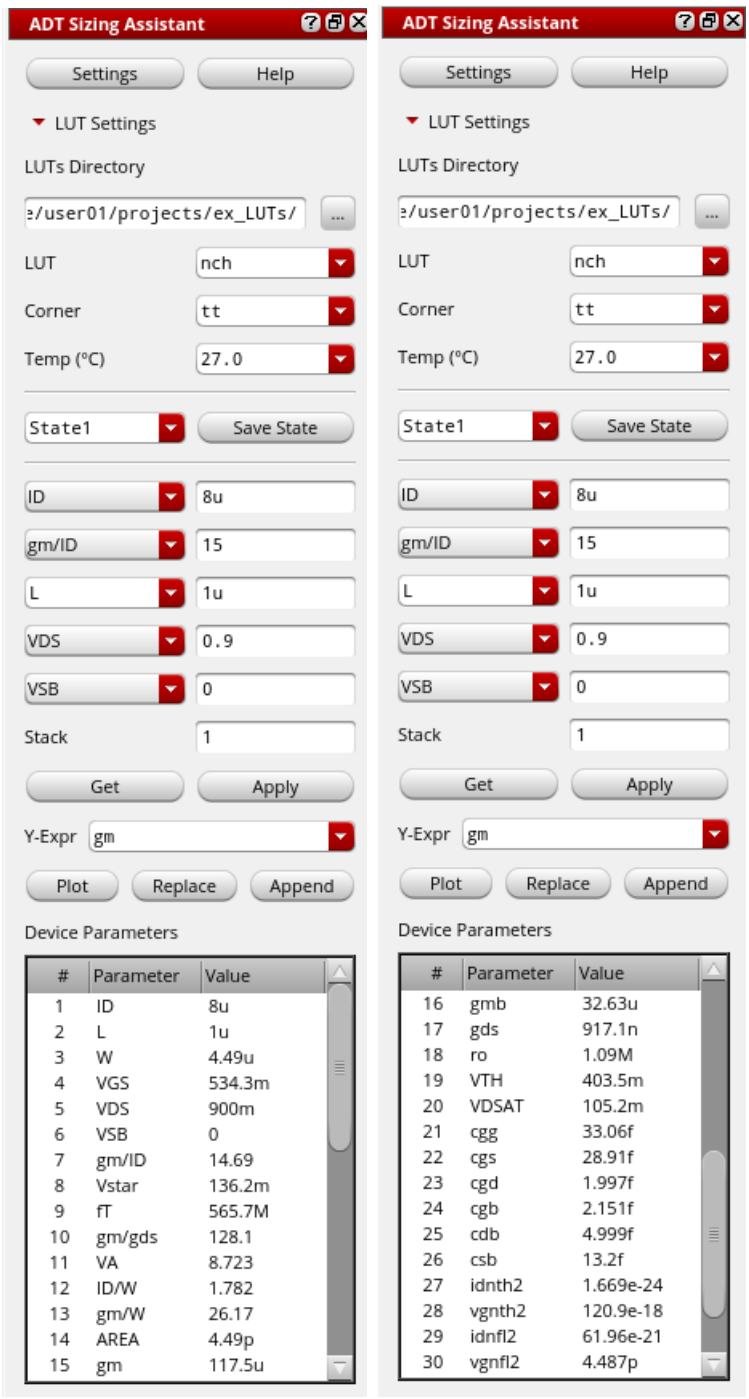
PZ analysis:



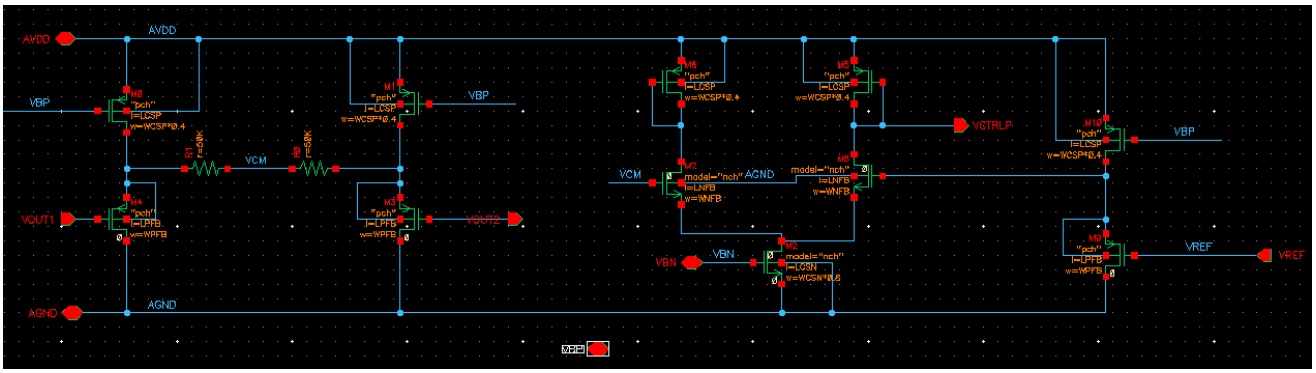
PART 4: Open-Loop OTA Simulation (Actual CMFB)

1 DESIGN OF CMFB CIRCUIT

LPFB

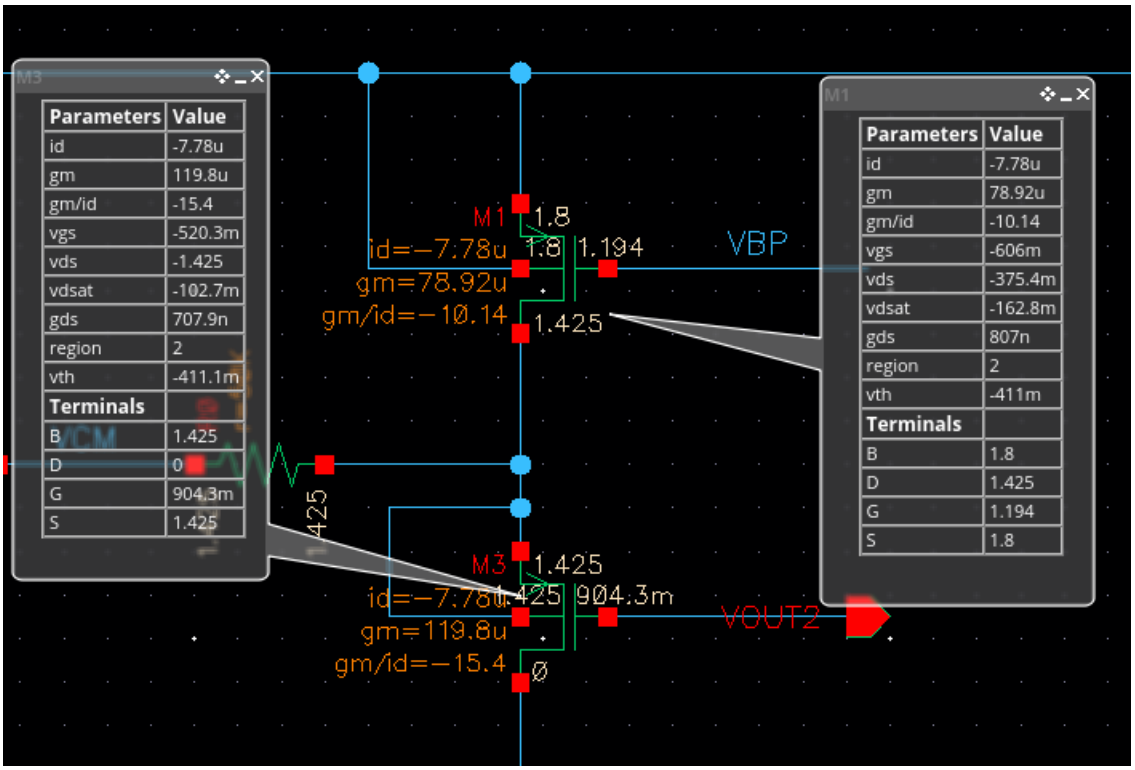

ADT Sizing Assistant
Settings
Help
LUT Settings
LUTs Directory
e/user01/projects/ex_LUTs/
...
LUT
nch
Corner
tt
Temp (°C)
27.0
State1
Save State
ID
8u
gm/ID
15
L
1u
VDS
0.9
VSB
0
Stack
1
Get
Apply
Y-Expr
gm
Plot
Replace
Append
Device Parameters
Parameter Value
1 ID 8u
2 L 1u
3 W 4.49u
4 VGS 534.3m
5 VDS 900m
6 VSB 0
7 gm/ID 14.69
8 Vstar 136.2m
9 fT 565.7M
10 gm/gds 128.1
11 VA 8.723
12 ID/W 1.782
13 gm/W 26.17
14 AREA 4.49p
15 gm 117.5u
ADT Sizing Assistant
Settings
Help
LUT Settings
LUTs Directory
e/user01/projects/ex_LUTs/
...
LUT
nch
Corner
tt
Temp (°C)
27.0
State1
Save State
ID
8u
gm/ID
15
L
1u
VDS
0.9
VSB
0
Stack
1
Get
Apply
Y-Expr
gm
Plot
Replace
Append
Device Parameters
Parameter Value
16 gmb 32.63u
17 gds 917.1n
18 ro 1.09M
19 VTH 403.5m
20 VDSAT 105.2m
21 cgg 33.06f
22 cgs 28.91f
23 cgd 1.997f
24 cgb 2.151f
25 cdb 4.999f
26 csb 13.2f
27 idnth2 1.669e-24
28 vgnth2 120.9e-18
29 idnfl2 61.96e-21
30 vgnfl2 4.487p

LNFB



M0,M1,M10,M5,M6 should be matched to the PMOS current source in the folded.

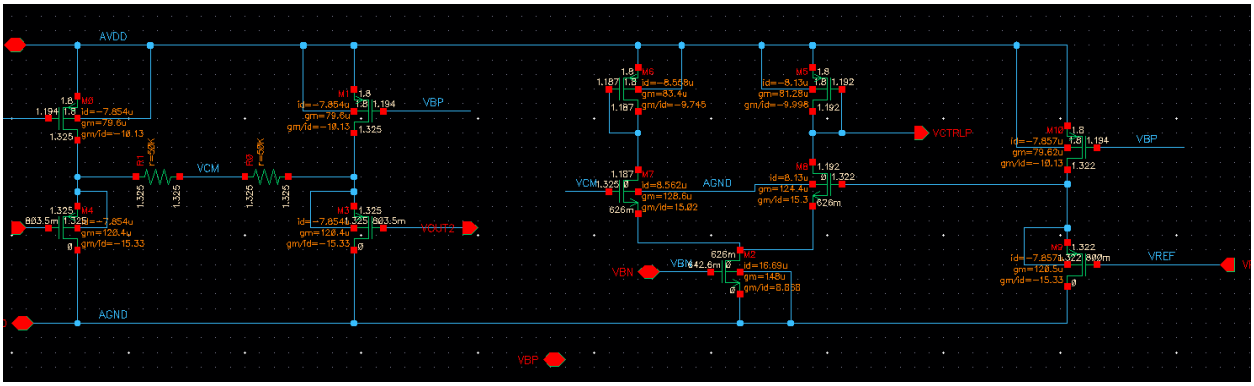
M2 should be matched to the NMOS current source in the folded.



VOUTmax=1116.9mv

So we can’t choose VREF=900mv

, We chose VREF=800mv, to not violate the output swing.

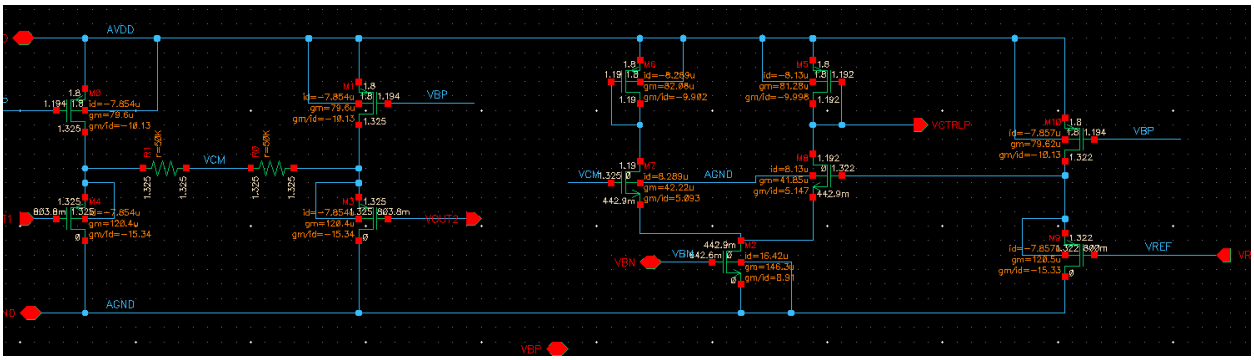


there is a violation to current consumption I=40.255u

, so we can roughly increase LPFP 3 times and decrease WPFP 3

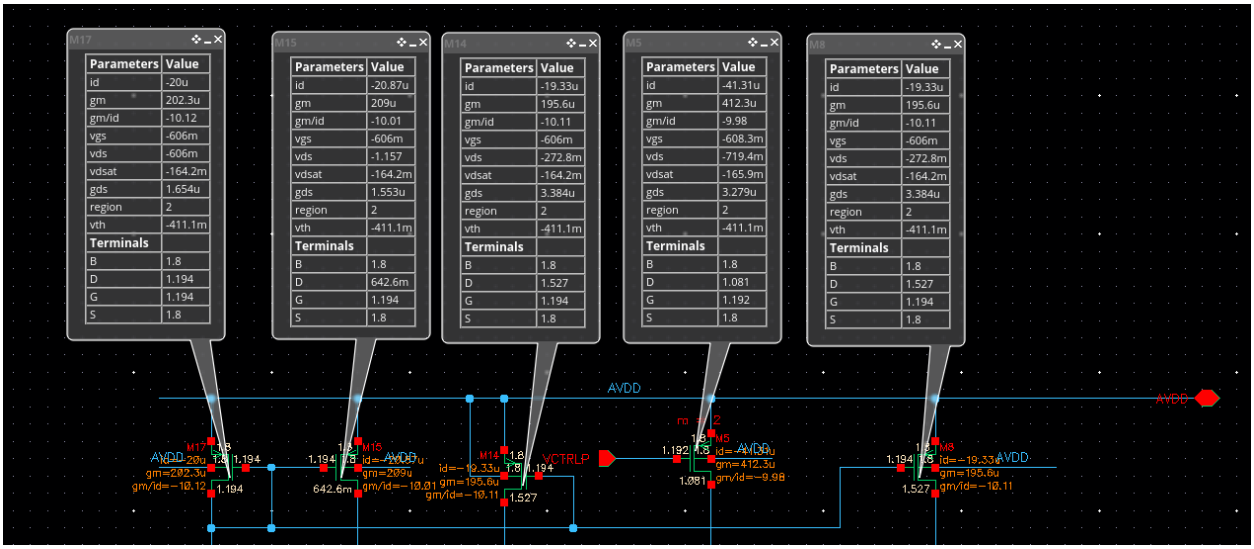
times to keep the same area,

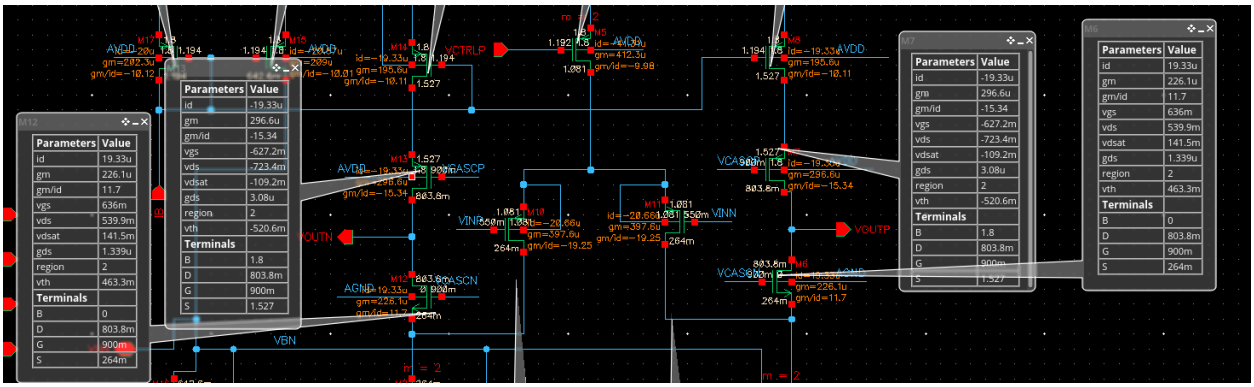
LNFB	3u
LPFB	1u
WNFB	1.496u
WPFB	18.48u

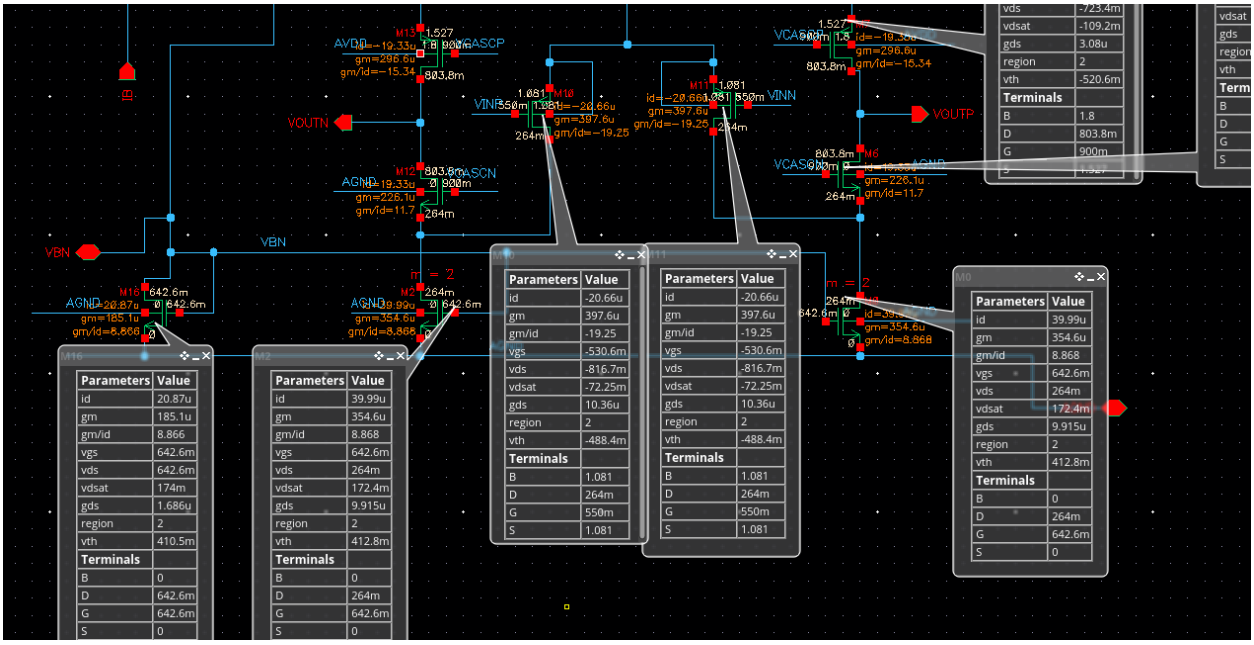


2 SCHEMATIC OF THE OTA AND CMFB CIRCUIT WITH DC NODE VOLTAGES AND TRANSISTORS OP PARAMETERS (ID, VGS, VDS, VDSAT, VTH, GM, GDS, REGION) CLEARLY ANNOTATED.

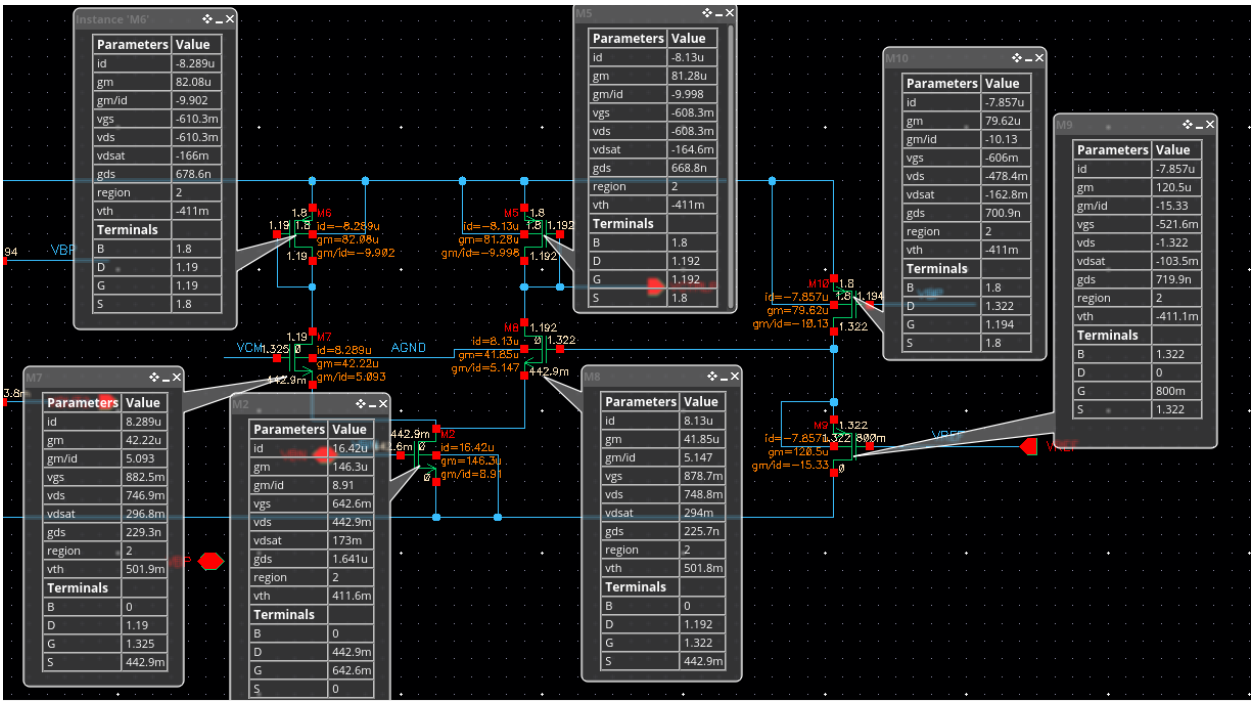
2.1 OTA :

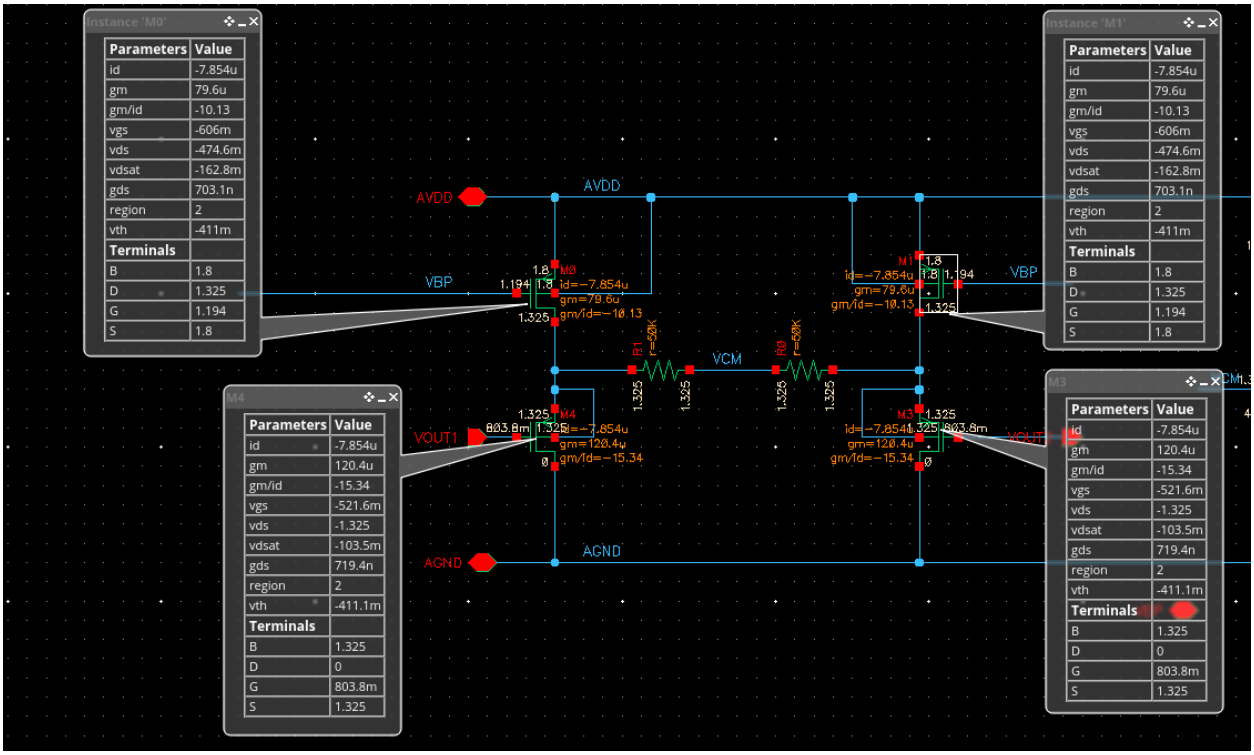




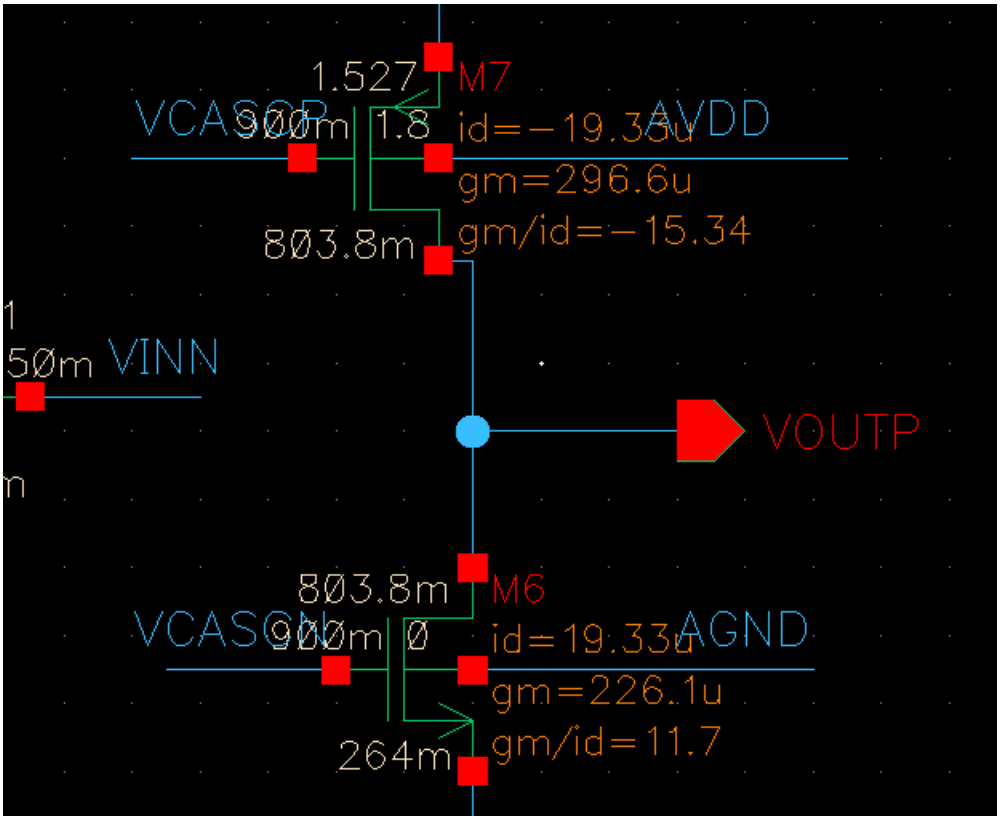

VOUTN
VOUTP
VINP
VINN
VBN
AVDD
AGND
VCASCP
VCASCN
M16
M2
M10
M11
M12
M13
M6
Parameters
Value
id
20.87u
gm
185.1u
gm/id
8.866
vgs
642.6m
vds
642.6m
vdsat
174m
gds
1.686u
region
2
vth
410.5m
Terminals
B
0
D
642.6m
G
642.6m
S
0
id
39.99u
gm
354.6u
gm/id
8.868
vgs
642.6m
vds
264m
vdsat
172.4m
gds
9.915u
region
2
vth
412.8m
id
-20.66u
gm
397.6u
gm/id
-19.25
vgs
-530.6m
vds
-816.7m
vdsat
-72.25m
gds
10.36u
region
2
vth
-488.4m
1.081
264m
550m
1.081
id
-20.66u
gm
397.6u
gm/id
-19.25
vgs
-530.6m
vds
-816.7m
vdsat
-72.25m
gds
10.36u
region
2
vth
-488.4m
1.081
264m
550m
1.081
id
39.99u
gm
354.6u
gm/id
8.868
vgs
642.6m
vds
264m
vdsat
172.4m
gds
9.915u
region
2
vth
412.8m
0
264m
642.6m
0
id
20.87u
gm
185.1u
gm/id
8.866
vgs
642.6m
vds
642.6m
vdsat
174m
gds
1.686u
region
2
vth
410.5m
0
642.6m
642.6m
0
id
39.99u
gm
354.6u
gm/id
8.868
vgs
642.6m
vds
264m
vdsat
172.4m
gds
9.915u
region
2
vth
412.8m
0
264m
642.6m
0
id
-109.2m
gds
3.08u
region
2
vth
-520.6m
1.8
803.8m
900m
id
-109.2m
gds
3.08u
region
2
vth
-520.6m
1.8
803.8m
900m

2.2 CMFB


VBP
VCM
AGND
VREF
M5
M6
M7
M8
M9
M10
Parameters
Value
id
-8.289u
gm
82.08u
gm/id
-9.902
vgs
-610.3m
vds
-610.3m
vdsat
-166m
gds
678.6n
region
2
vth
-411m
Terminals
B
1.8
D
1.19
G
1.19
S
1.8
id
-8.13u
gm
81.28u
gm/id
-9.998
vgs
-608.3m
vds
-608.3m
vdsat
-164.6m
gds
668.8n
region
2
vth
-411m
Terminals
B
1.8
D
1.192
G
1.192
S
1.8
id
-7.857u
gm
79.62u
gm/id
-10.13
vgs
-606m
vds
-478.4m
vdsat
-162.8m
gds
700.9n
region
2
vth
-411m
Terminals
B
1.8
D
1.322
G
1.194
S
1.8
id
-7.857u
gm
120.5u
gm/id
-15.33
vgs
-521.6m
vds
-1.322
vdsat
-103.5m
gds
719.9n
region
2
vth
-411.1m
Terminals
B
1.322
D
0
G
800m
S
1.322
id
8.289u
gm
42.22u
gm/id
5.093
vgs
882.5m
vds
746.9m
vdsat
296.8m
gds
229.3n
region
2
vth
501.9m
Terminals
B
0
D
1.19
G
1.325
S
442.9m
id
16.42u
gm
146.3u
gm/id
8.91
vgs
642.6m
vds
442.9m
vdsat
173m
gds
1.641u
region
2
vth
411.6m
Terminals
B
0
D
442.9m
G
642.6m
S
0
id
8.13u
gm
41.85u
gm/id
5.147
vgs
878.7m
vds
748.8m
vdsat
294m
gds
225.7n
region
2
vth
501.8m
Terminals
B
0
D
1.192
G
1.322
S
442.9m

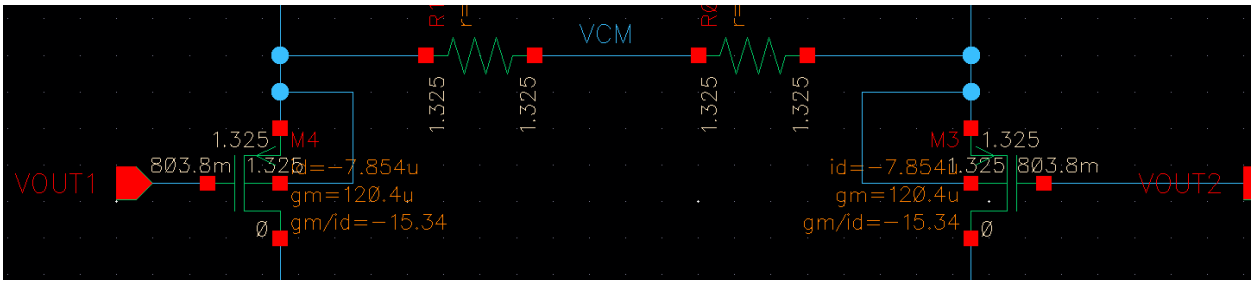


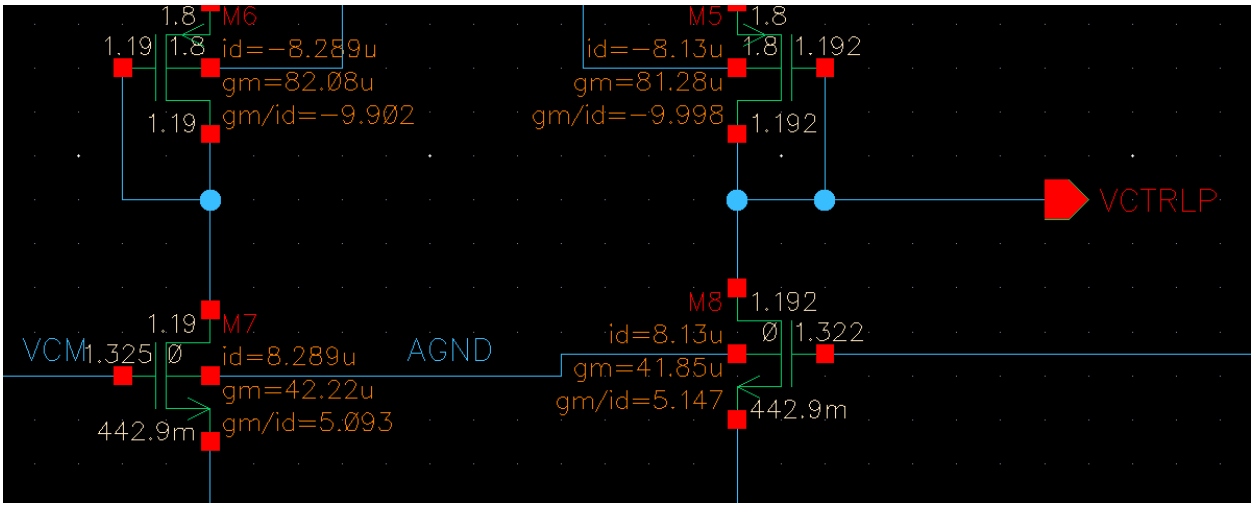
2.3 What is the CM level at the OTA output? Why?



803.8m, as the cmfb loop made the output cm approximately equal to the reference voltage =800mv that we introduced.

2.4 What are the differential input and output voltages of the error amplifier? What is the relation between them?





ΔVIN=1.325-1.322=3.8mv

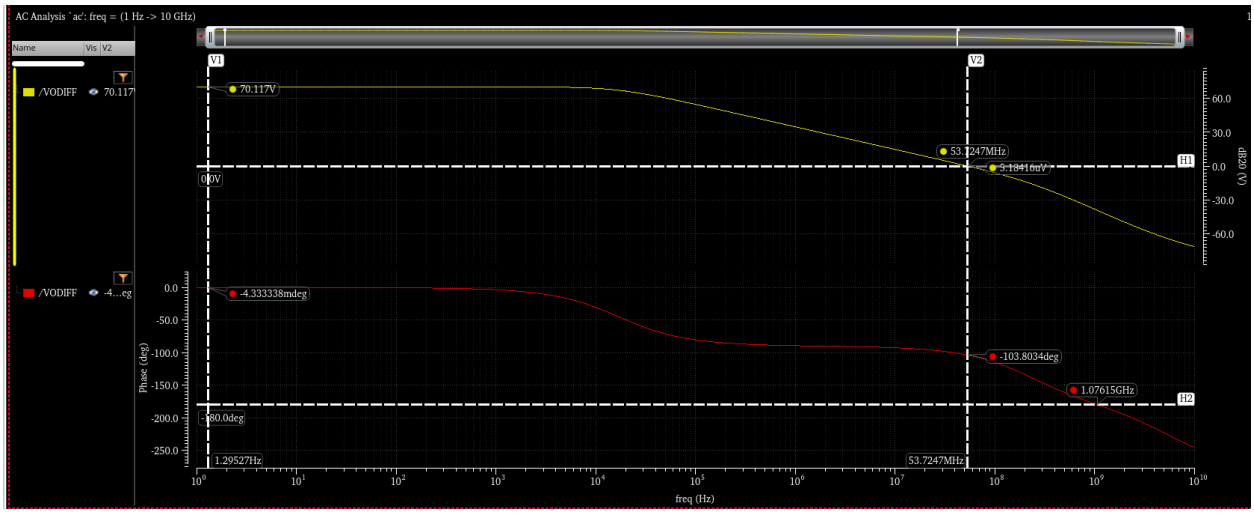
ΔVout=Vout-VoutQ=1.192-1.19=2mv

The relation between them is the error amplifier gain:

$\Delta VOUT = \Delta VIN * Av$, AV=$\frac{gm8}{gm5} = 0.514$

3 DIFF SMALL SIGNAL CCS:

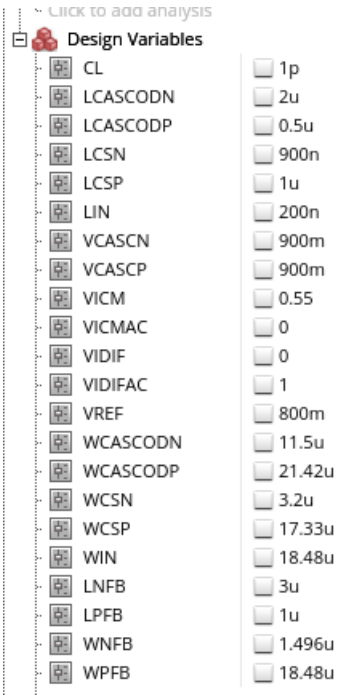
3.1 PLOT DIFF GAIN (MAGNITUDE IN DB AND PHASE) VS FREQUENCY.



3.2 CALCULATE CIRCUIT PARAMETERS (DC GAIN, BW, GBW, UGF, AND PM).

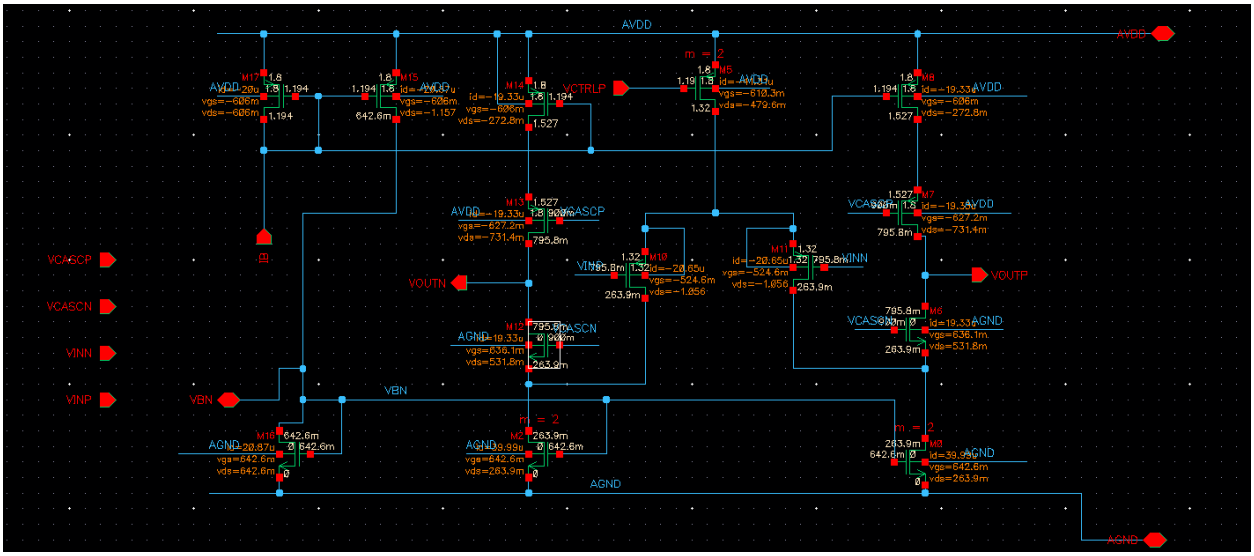
Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
MINIPROJECT2_...	A0	3.205K			
MINIPROJECT2_...	A0_DB	70.12			
MINIPROJECT2_...	BW	17.14K			
MINIPROJECT2_...	FU	54.05M			
MINIPROJECT2_...	GBW	54.94M			

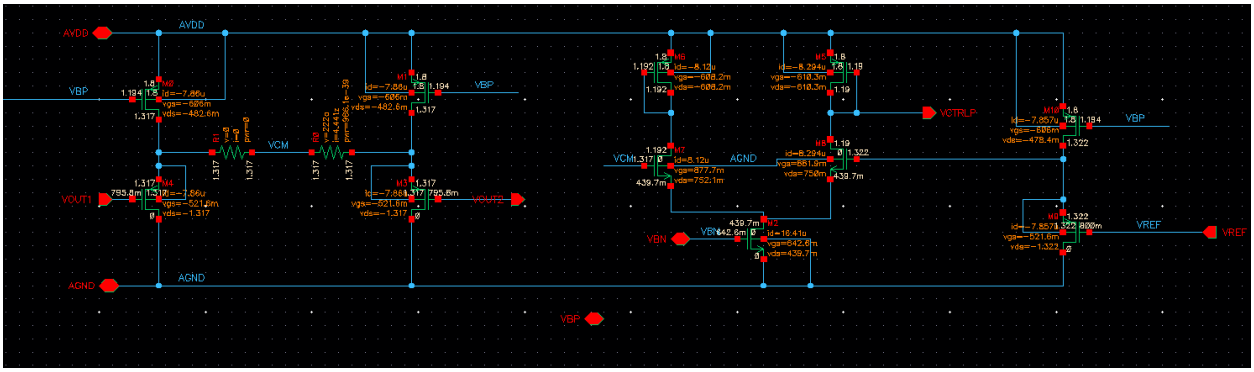
PM=180-103.8=76.2


Click to add analysis
Design Variables
CL 1p
LCASCODN 2u
LCASCODP 0.5u
LCSN 900n
LCSP 1u
LIN 200n
VCASCN 900m
VCASCP 900m
VICM 0.55
VICMAC 0
VIDIF 0
VIDIFAC 1
VREF 800m
WCASCODN 11.5u
WCASCODP 21.42u
WCSN 3.2u
WCSP 17.33u
WIN 18.48u
LNFB 3u
LPFB 1u
WNFB 1.496u
WPFB 18.48u

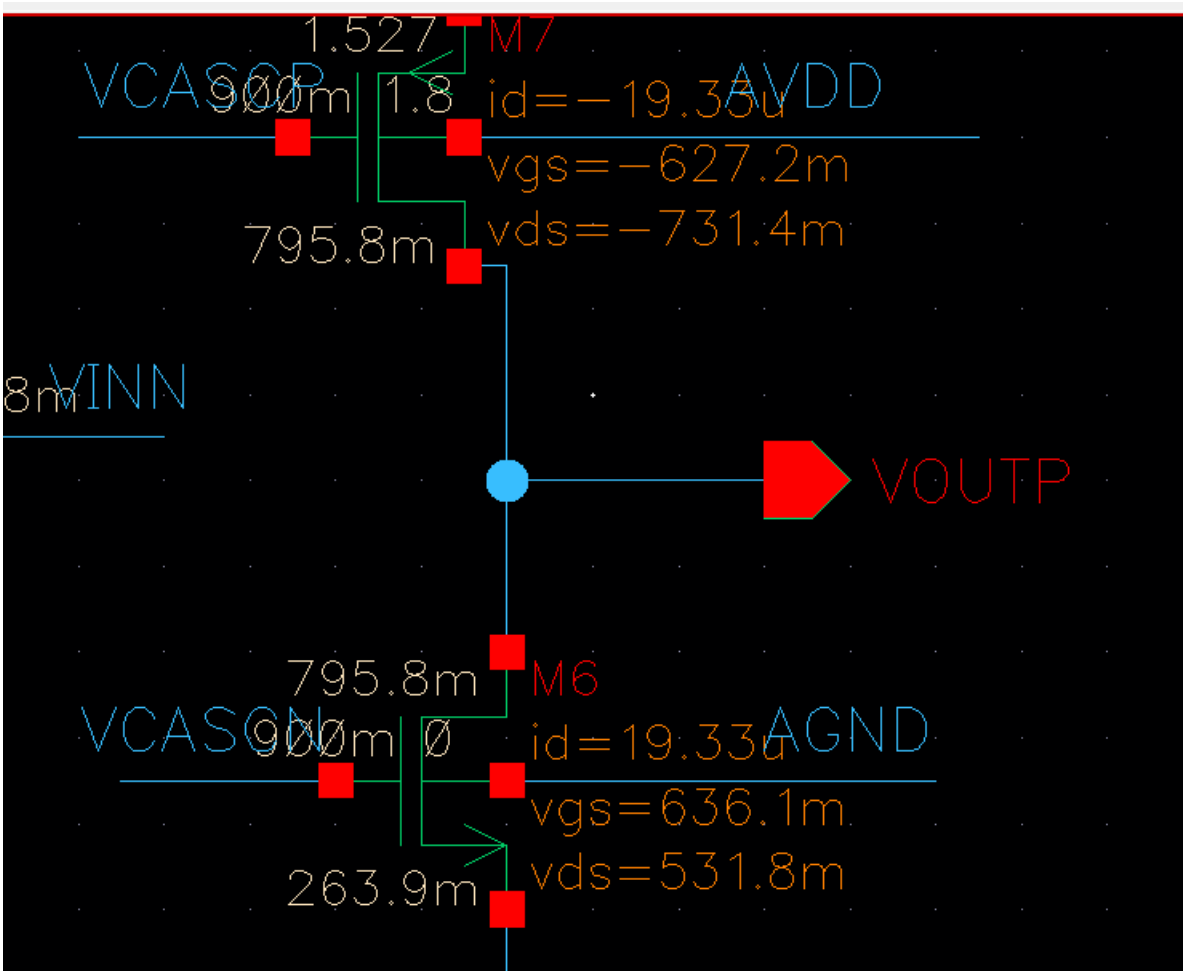
PART 5: Closed Loop Simulation (AC and STB Analysis)

1 SCHEMATIC OF THE OTA AND THE CMFB CIRCUIT WITH DC OP POINT CLEARLY ANNOTATED IN CLOSED-LOOP CONFIGURATION



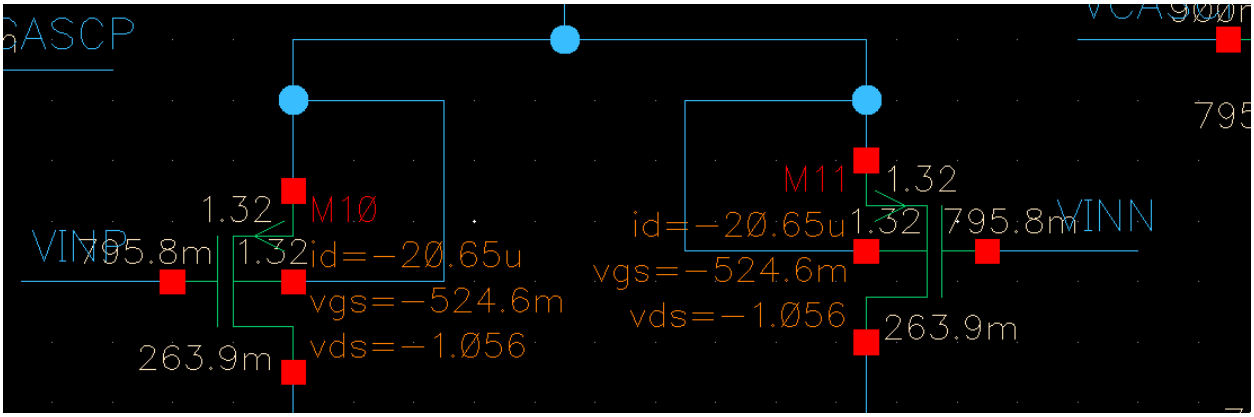


1.1 What is the CM level at the OTA output? Why?



795.8mv, near the ref voltage we introduced 800mv.

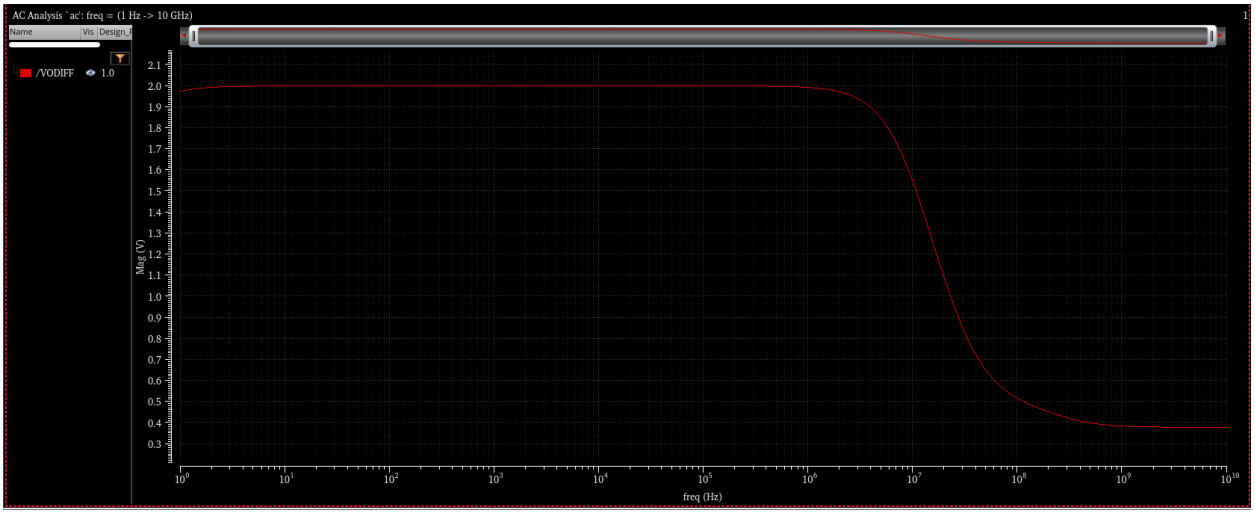
1.2 What is the CM level at the OTA input? Why?



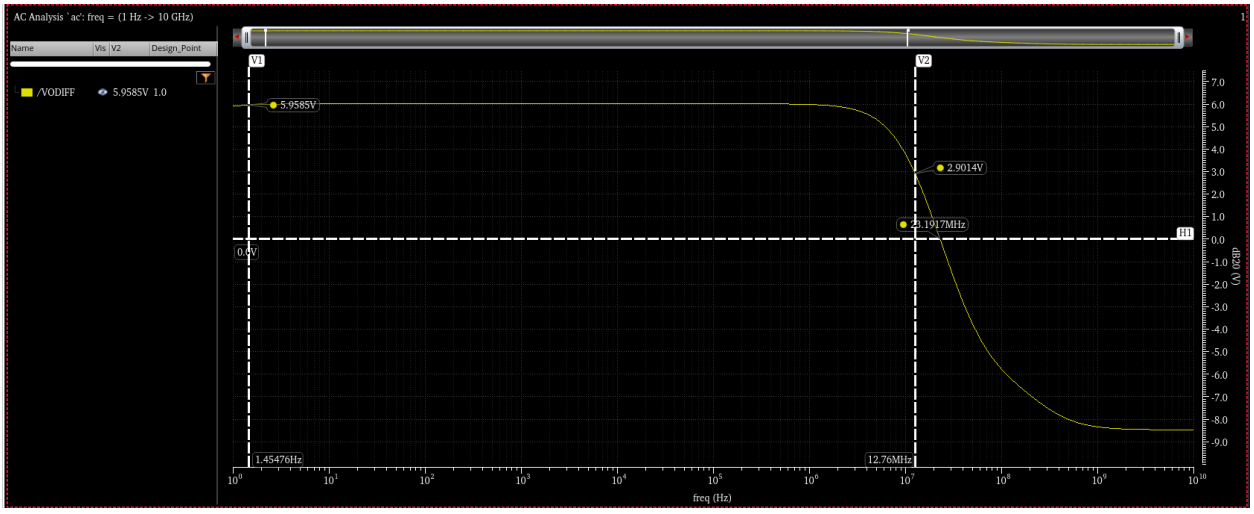
795.8mv equal to Vocm, as we connected VOUTN to VINP and VOUTP to VINN to maintain negative feedback and we set large resistance across the feedback capacitance, so Vicm = Vocm.

2 DIFFERENTIAL CLOSED-LOOP RESPONSE:

2.1 PLOT VODIFF VS FREQUENCY



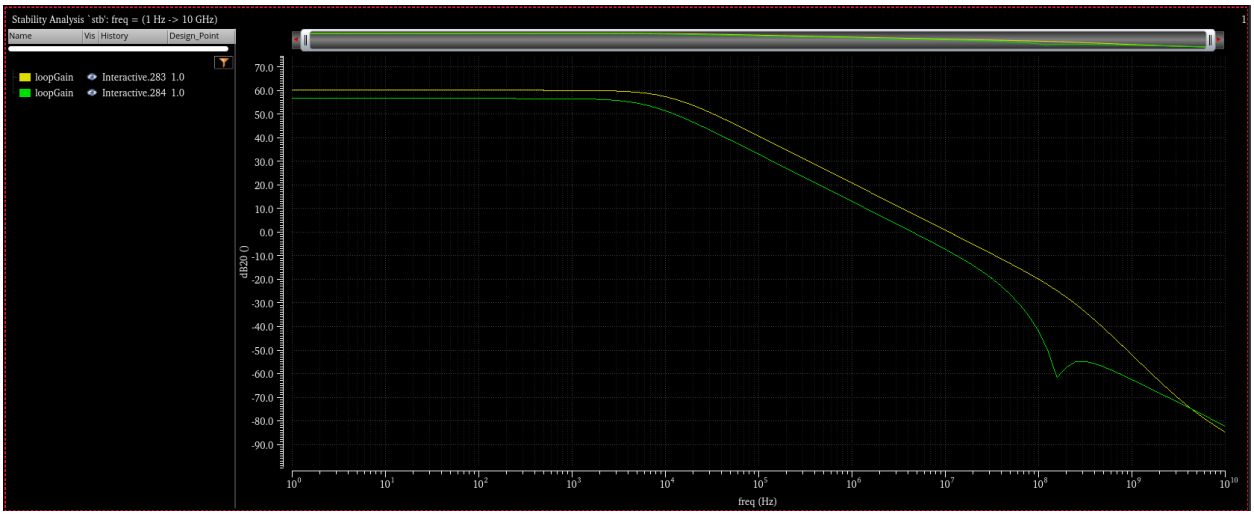
2.2 USE MEASURES OR CURSORS TO CALCULATE CIRCUIT PARAMETERS (DC GAIN, CL BW, CL GBW)



MINIPROJECT2_...	ymax(mag(v("/V...	1.998			
MINIPROJECT2_...	bandwidth(mag(...	12.76M			
MINIPROJECT2_...	gainBwProd(ma...	25.25M			

3 DIFFERENTIAL AND CMFB LOOPS STABILITY (STB ANALYSIS):

3.1 PLOT LOOP GAIN IN DB AND PHASE VS FREQUENCY FOR THE TWO SIMULATIONS OVERLAID



3.2 DIFF:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
MINIPROJECT2_...	loopGain				
MINIPROJECT2_...	/phaseMargin_s...	87.18			
MINIPROJECT2_...	ymax(db20(getD...	60.24			
MINIPROJECT2_...	bandwidth(mag(...	10.65K			
MINIPROJECT2_...	gainBwProd(ma...	10.98M			

3.3 CM:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
MINIPROJECT2_...	loopGain				
MINIPROJECT2_...	/phaseMargin_s...	81.41			
MINIPROJECT2_...	ymax(db20(getD...	56.65			
MINIPROJECT2_...	bandwidth(mag(...	6.652K			
MINIPROJECT2_...	gainBwProd(ma...	4.534M			

3.4 COMPARE GBW AND PM OF DIFF AND CM LOOPS. COMMENT.

	DIFF	CM
GBW	10.98M	4.534M
PM	87.18	81.41

$\boldsymbol{GBW_{diff} > GBW_{cm}, PM_{diff} > PM_{cm},}$ the common mode loop is slower than the differential loop.

3.5 COMPARE DC LG AND GBW OF THE DIFF LOOP WITH THOSE OBTAINED FROM OPEN-LOOP SIMULATION. COMMENT

	DIFF LOOP	Obtained from OPEN-LOOP	Open loop
DC LG	60.24db	AOL*β=3205/3=1068.3 =60.57db	70.12db
GBW	10.98M	54.94/3=18.31M	54.94M

The GBW is much less than the value obtained from open-loop as the beta network we used is capacitance feedback so it affect the bw itself.

PART 6: Closed Loop Simulation (Transient Analysis)

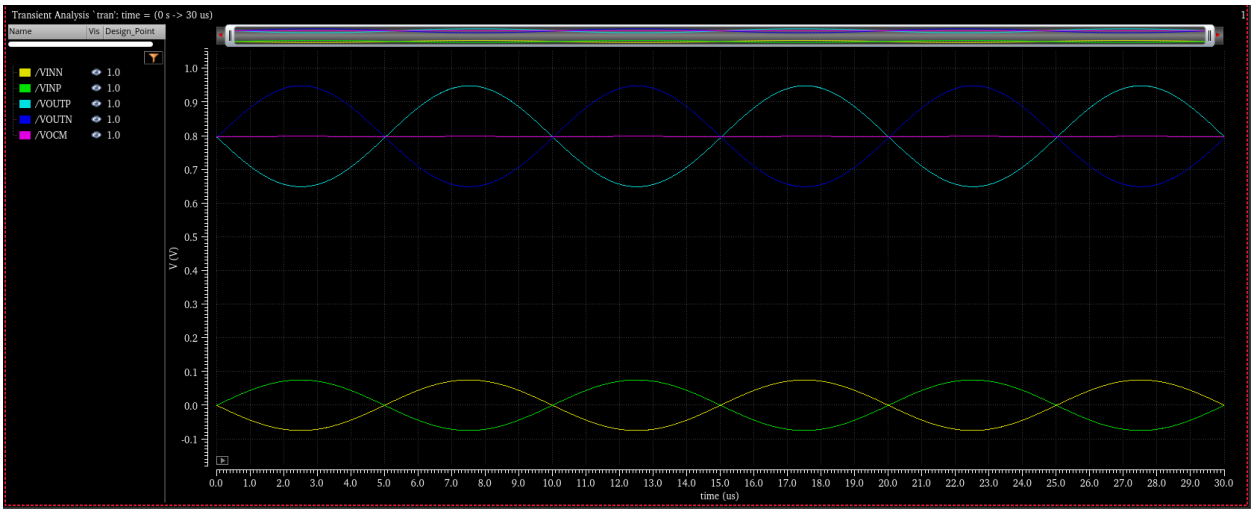
1 Apply a differential input pulse (initial value = 0, pulse value = 100mV, delay = 1us, period = 2us, pulse width = 1us, rise = fall = 10ns), Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

They are both stable, but cm has a small ringing as the cmfb loop is not that fast, but it's stable with adequate pm as it isn't even noticeable in this overlaid plot.

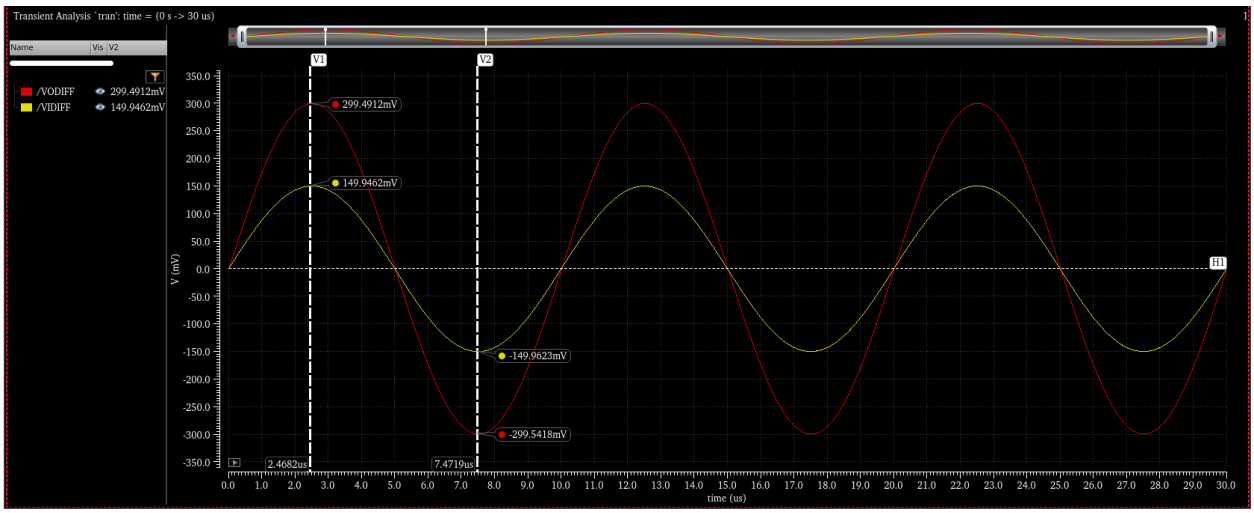
2 Run transient analysis for 3us to test the fully differential capacitive amplifier stability, Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

They are both stable with adequate phase margin.

3 Apply a differential sinusoidal input with freq = 100kHz and amplitude = 150mV, Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure



4 PLOT THE TRANSIENT SIGNALS AT VIDIFF AND VODIFF OVERLAID IN THE SAME FIGURE.



5 CALCULATE THE DIFF INPUT AND OUTPUT PEAK-TO-PEAK SWINGS AND THE CLOSED LOOP GAIN.

MINIPROJECT2_...	ymax(v("/VODIF...	299.6m			
MINIPROJECT2_...	ymin(v("/VODIFF...	-299.6m			
MINIPROJECT2_...	ymax(v("/VIDIFF...	150m			
MINIPROJECT2_...	ymin(v("/VIDIFF"...	-150m			

Δvin=300mv

Δvout=599.2mv

So the closed loop gain $\frac{\Delta vout}{\Delta vin} = 1.997 \sim 2$