

PART 1: Sizing Chart

1 DEVICE SIZING USING SA

The screenshot shows the ADT Sizing Assistant window. It has a title bar with a question mark, lock, and close icon. Below the title bar are 'Settings' and 'Help' buttons. A 'LUT Settings' section is expanded, showing 'LUTs Directory' with a text field containing 'e:/user01/projects/ex_LUTs/' and a browse button. Below this are three dropdown menus for 'LUT' (set to 'pch'), 'Corner' (set to 'tt'), and 'Temp (°C)' (set to '27.0'). A 'State1' dropdown and a 'Save State' button are also present. A series of input fields follow: 'ID' (10u), 'Vstar' (200m), 'L' (1u), 'VDS' (VGS), 'VSB' (0), and 'Stack' (1). 'Get' and 'Apply' buttons are below these fields. A 'Y-Expr' dropdown is set to 'gm'. At the bottom of this section are 'Plot', 'Replace', and 'Append' buttons. The 'Device Parameters' section contains a table with 15 rows of data.

#	Parameter	Value
1	ID	10u
2	L	1u
3	W	8.72u
4	VGS	609.2m
5	VDS	609.2m
6	VSB	0
7	gm/ID	9.896
8	Vstar	202.1m
9	fT	236.1M
10	gm/gds	120.8
11	VA	12.21
12	ID/W	1.147
13	gm/W	11.35
14	AREA	8.72p
15	gm	98.96u

ADT Sizing Assistant

Settings

Help

▼ LUT Settings

LUTs Directory

z:/user01/projects/ex_LUTs/

...

LUT

pch

▼

Corner

tt

▼

Temp (°C)

27.0

▼

State1

▼

Save State

ID

▼

10u

Vstar

▼

200m

L

▼

1u

VDS

▼

VGS

VSB

▼

0

Stack

1

Get

Apply

Y-Expr

gm

▼

Plot

Replace

Append

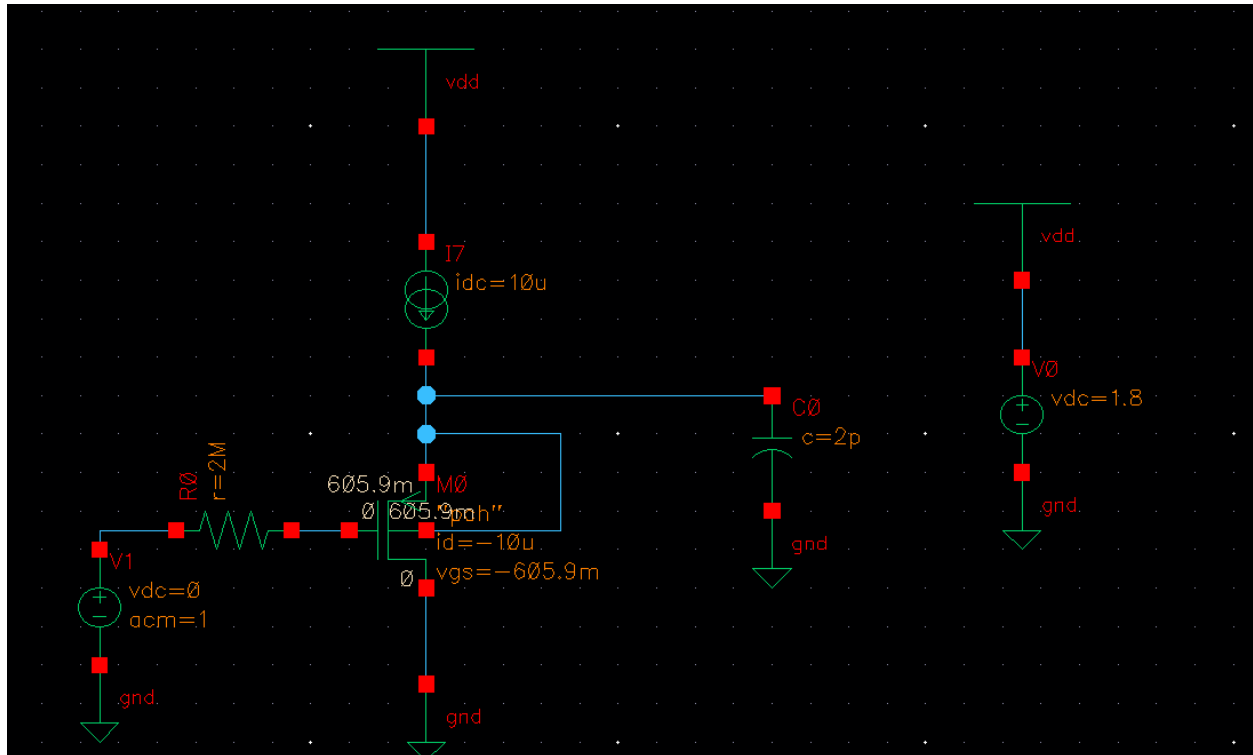
Device Parameters

#	Parameter	Value
15	gm	98.96u
16	gmb	30.71u
17	gds	819.3n
18	ro	1.221M
19	VTH	409.6m
20	VDSAT	160.6m
21	cgg	66.72f
22	cgs	57.78f
23	cgd	5.618f
24	cgb	3.316f
25	cdb	9.598f
26	csb	26.28f
27	idnth2	1.446e-24
28	vgnth2	147.7e-18
29	idnfl2	20.51e-21

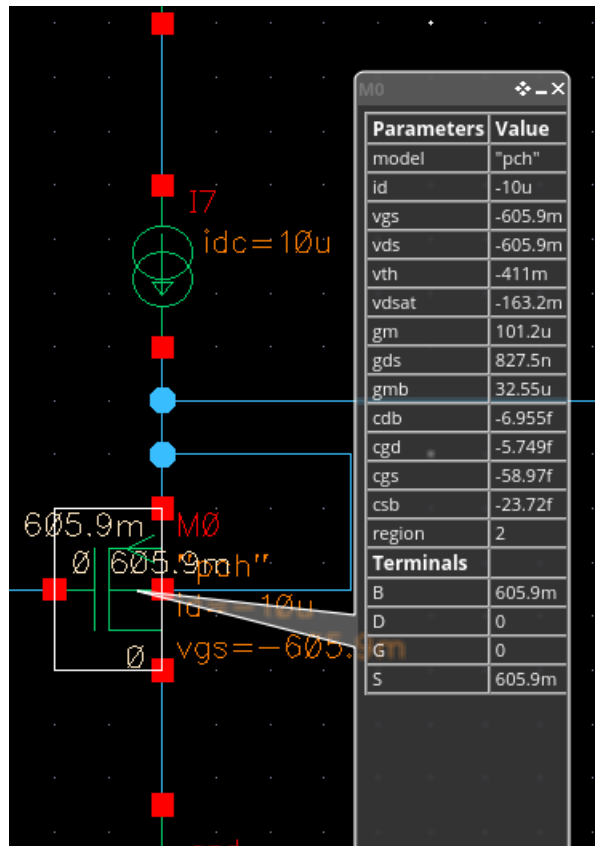
Part 2: CD Amplifier

OP ANALYSIS

1 CREATE A NEW SCHEMATIC FOR THE CD AMPLIFIER



2 SIMULATE THE OP POINT. REPORT A SNAPSHOT CLEARLY SHOWING THE FOLLOWING PARAMETERS



3 CHECK THAT THE TRANSISTOR OPERATES IN SATURATION.

cc wcm

Cadence Hint: The "region" meaning is as follows: (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown).

Region is 2, and $v_{gs} = v_{ds}$ so it is diode connected transistor.

AC ANALYSIS

- 1 PERFORM AC ANALYSIS (1HZ:10GHZ, LOGARITHMIC, 20POINTS/DECADE) TO INVESTIGATE THE FREQUENCY DOMAIN PEAKING.

Choosing Analyses -- ADE Assembler

Analysis

☐ tran

☐ dc

☒ ac

☐ noise

☐ xf

☐ sens

☐ dcmatch

☐ acmatch

☐ stb

☐ pz

☐ lf

☐ sp

☐ envlp

☐ pss

☐ pac

☐ pstb

☐ pnoise

☐ pxf

☐ psp

☐ qpss

☐ qpac

☐ qpnoise

☐ qpxf

☐ qpssp

☐ hb

☐ hbac

☐ hbstb

☐ hbnoise

☐ hbsp

☐ hbxf

AC Analysis

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

Sweep Range

☒ Start-Stop

☐ Center-Span

Start

1

Stop

10G

Sweep Type

Logarithmic

☒ Points Per Decade

☐ Number of Steps

20

Add Specific Points

☐

Add Points By File

☐

Specialized Analyses

None

Enabled

☒

Options...

OK

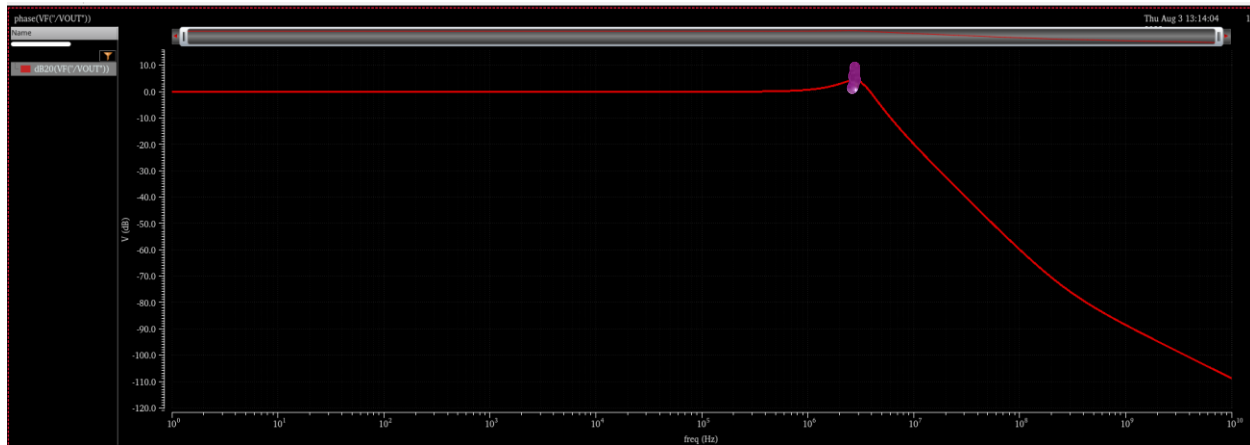
Cancel

Defaults

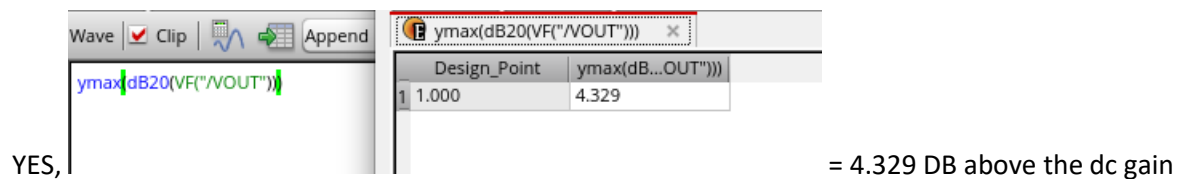
Apply

Help

2 REPORT THE BODE PLOT MAGNITUDE



3 DO YOU NOTICE FREQUENCY DOMAIN PEAKING? HOW MUCH IS THE PEAKING?



4 ANALYTICALLY CALCULATE THE QUALITY FACTOR (USE APPROXIMATE EXPRESSIONS). IS THE SYSTEM UNDERDAMPED OR OVERDAMPED?

$CL=2P$, $Cgs=59\text{ f}$, $Cgd =5.75\text{ f}$

$CL \gg C$ (mos)

So we can use approximate expressions $Q = \sqrt{\frac{gm(Cgs+Cgd)Rsig}{CL}} = 2.56$

But $Rsig$ is so big so

$$Q = \frac{\sqrt{b2}}{b1}$$







$$\sqrt{b2} = \left(\sqrt{\frac{CL(Cgs+Cgd)+CgsCgd}{gm}} \right) Rsig$$

$$b1=CgdRsig + \frac{Cgs+Cl}{gm}$$

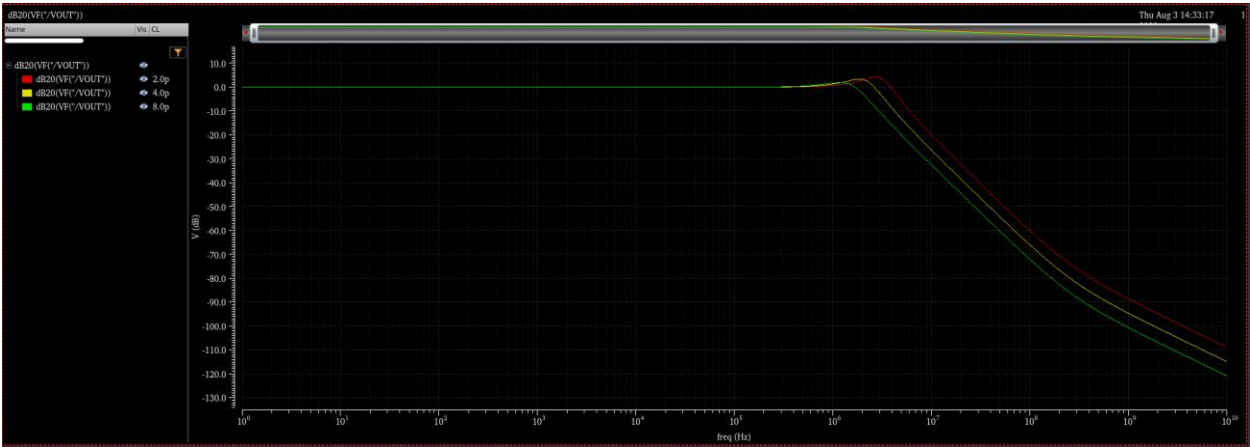
So, Q= 1.59

Q>0.5 SO IT IS underdamped system.

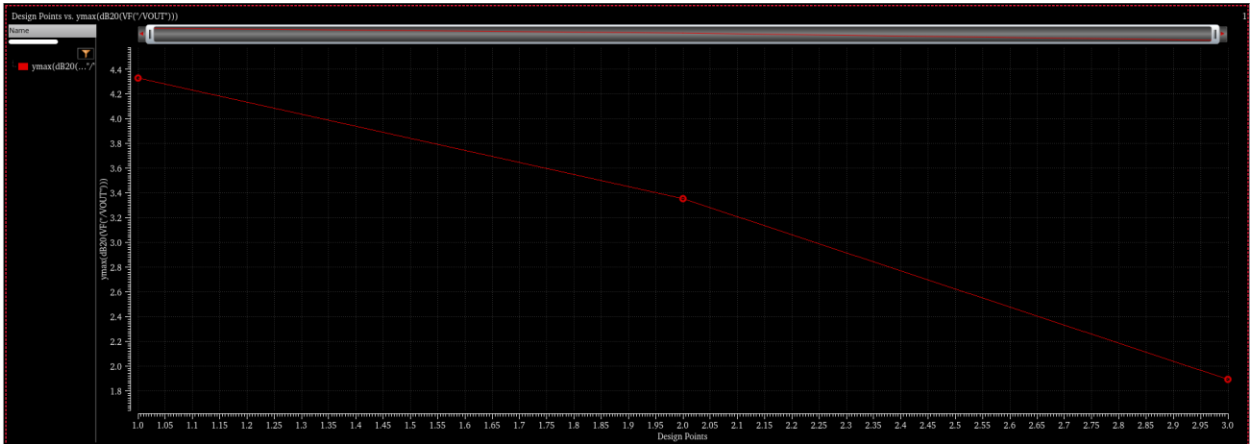
5 [OPTIONAL] PERFORM PARAMETRIC SWEEP: CL = 2p, 4p, 8p.

Parameters: CL=2p			
1	LAB4_lab_1	dB20(VF"/VOU...	
1	LAB4_lab_1	phase(VF"/VOU...	
1	LAB4_lab_1	ymax(dB20(VF("...	4.329
Parameters: CL=4p			
2	LAB4_lab_1	dB20(VF("/VOU...	
2	LAB4_lab_1	phase(VF("/VOU...	
2	LAB4_lab_1	ymax(dB20(VF("...	3.354
Parameters: CL=8p			
3	LAB4_lab_1	dB20(VF("/VOU...	
3	LAB4_lab_1	phase(VF("/VOU...	
3	LAB4_lab_1	ymax(dB20(VF("...	1.892

5.1 REPORT BODE PLOT MAGNITUDE OVERLAID ON SAME PLOT.



5.2 REPORT THE PEAKING VS CL.



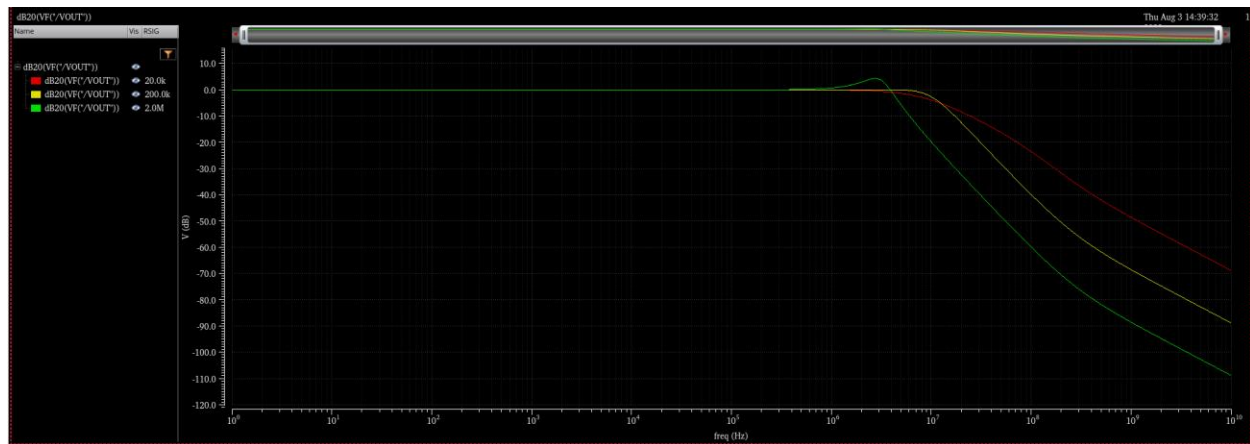
5.3 COMMENT

As we increasing CL, Q decreases so the peaking decreases as ω_{out} becomes more dominant and also ω_o decreases (the frequency at which peaking happens is decreased).

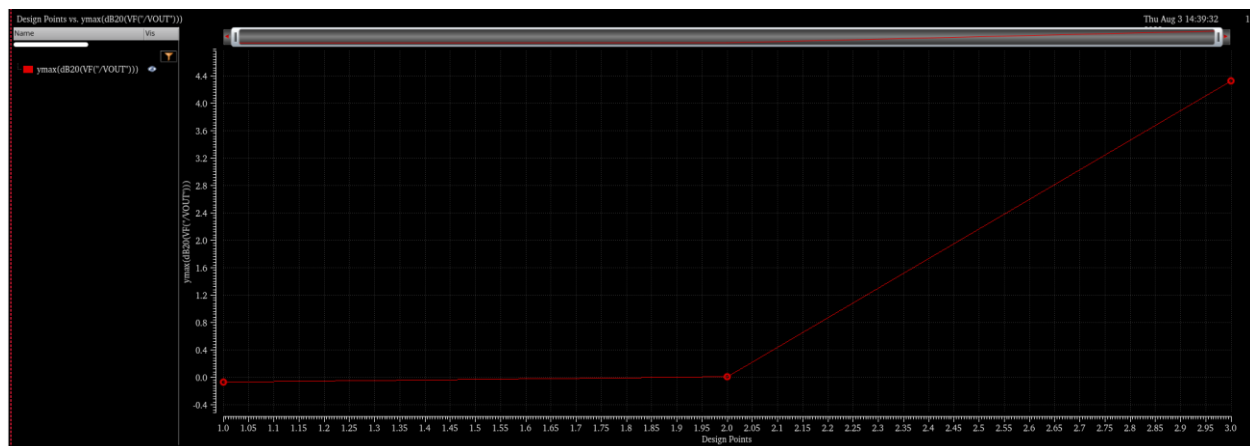
6 [OPTIONAL] PERFORM PARAMETRIC SWEEP: RSIG = 20K, 200K, 2M.

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: RSIG=20K						
1	LAB4_lab_1	dB20(VF"/VOU...				
1	LAB4_lab_1	phase(VF"/VOU...				
1	LAB4_lab_1	ymax(dB20(VF"...	-70.73m			
Parameters: RSIG=200K						
2	LAB4_lab_1	dB20(VF"/VOU...				
2	LAB4_lab_1	phase(VF"/VOU...				
2	LAB4_lab_1	ymax(dB20(VF"...	7.88m			
Parameters: RSIG=2M						
3	LAB4_lab_1	dB20(VF"/VOU...				
3	LAB4_lab_1	phase(VF"/VOU...				
3	LAB4_lab_1	ymax(dB20(VF"...	4.329			

6.1 REPORT BODE PLOT MAGNITUDE OVERLAID ON SAME PLOT



6.2 REPORT THE PEAKING VS RSIG

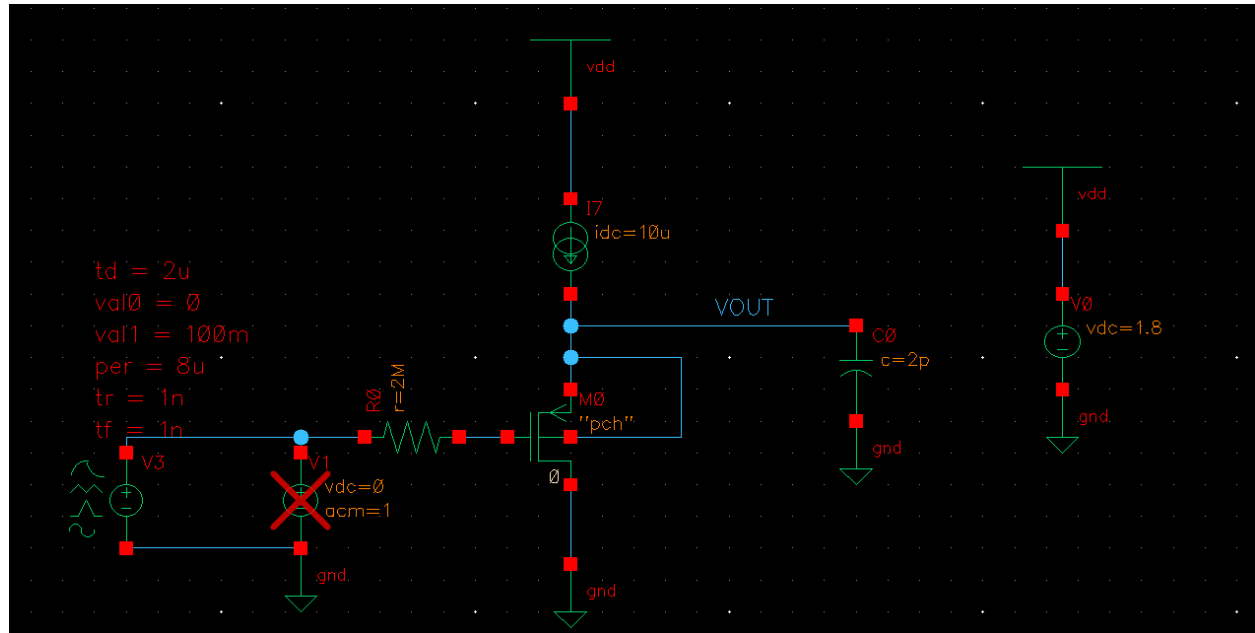


6.3 COMMENT

As increasing R_{sig} , Q increased so the peaking increased but the natural frequency decreased, so if we decreased R_{sig} we will see less peaking and higher ω_o (flatter response) .

Transient Analysis

- 1 USE A PULSE SOURCE AS YOUR TRANSIENT STIMULUS AND SET IT AS FOLLOWS: DELAY TIME = 2US, INITIAL (ZERO VALUE) = 0V, PERIOD = 8US, PULSE (ONE VALUE) = 100mV, FALL TIME = 1NS, RISE TIME = 1NS, PULSE WIDTH = 4US.



2 RUN TRANSIENT ANALYSIS FOR 10US TO INVESTIGATE THE TIME DOMAIN RINGING

Analysis

☒ tran ☐ dc ☐ ac ☐ noise
☐ xf ☐ sens ☐ dcmatch ☐ acmatch
☐ stb ☐ pz ☐ lf ☐ sp
☐ envlp ☐ pss ☐ pac ☐ pstb
☐ pnoise ☐ pxf ☐ psp ☐ qpss
☐ qpac ☐ qpnoise ☐ qpxf ☐ qpssp
☐ hb ☐ hbac ☐ hbstb ☐ hbnoise
☐ hbbsp ☐ hbxf

Transient Analysis

Stop Time

Accuracy Defaults (errpreset)
☐ conservative ☒ moderate ☐ liberal

☐ Transient Noise

Dynamic Parameter ☐

Enabled ☒

Options...

OK Cancel Defaults Apply Help

Transient Options

Time Step Algorithm State File Output EM/IR Output Fault

SIMULATION INTERVAL PARAMETERS

start

outputstart

TIME STEP PARAMETERS

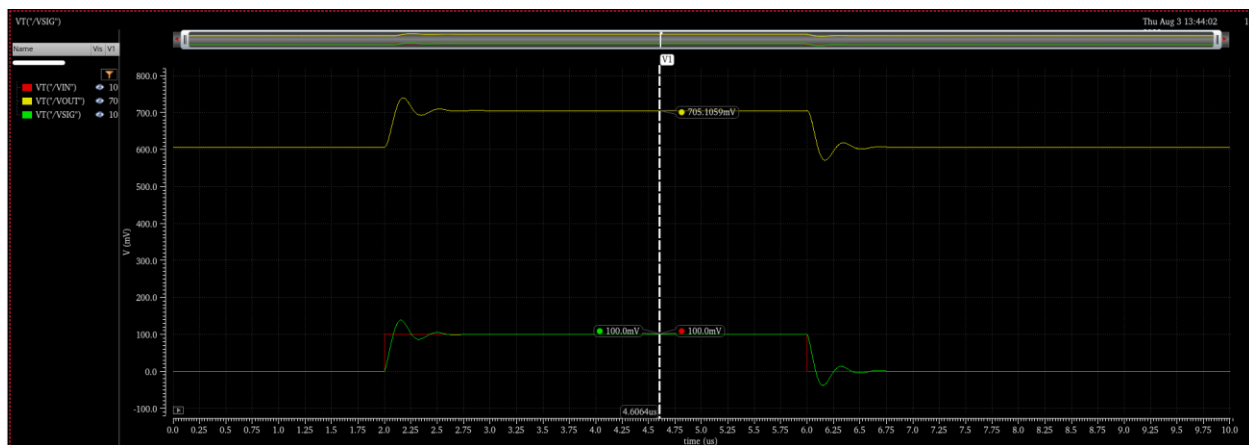
step

maxstep

minstep

OK Cancel

3 REPORT VIN AND VOUT OVERLAID VS TIME.



4 CALCULATE THE DC VOLTAGE DIFFERENCE (DC SHIFT) BETWEEN VIN AND VOUT.

4.1 WHAT IS THE RELATION BETWEEN THE DC SHIFT AND VGS OF THE TRANSISTOR?

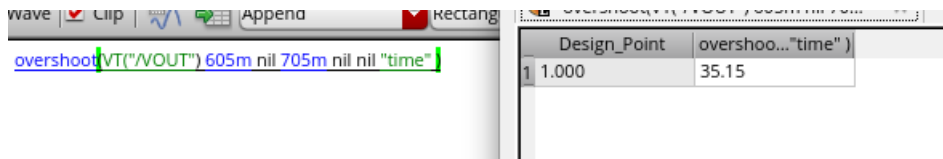
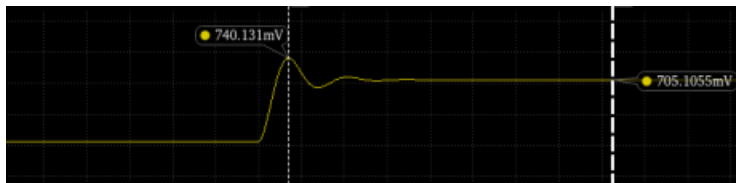
the DC shift = VGS of the transistor=605mv

4.2 HOW TO SHIFT THE SIGNAL DOWN INSTEAD OF SHIFTING IT UP?

By using NMOS.

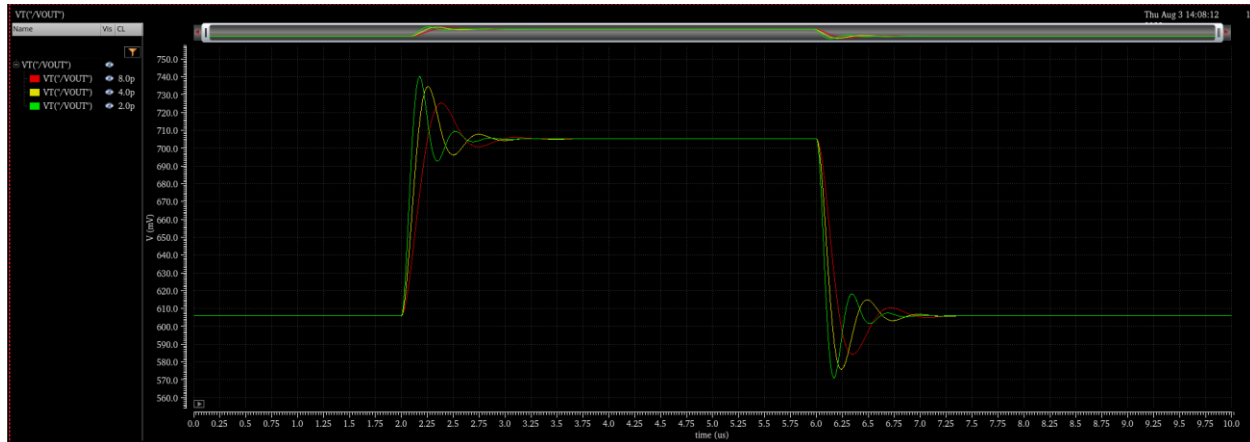
5 DO YOU NOTICE TIME DOMAIN RINGING? HOW MUCH IS THE OVERSHOOT?

YES, $overshoot = e^{\frac{-\pi}{4 \cdot (Q)^2 - 1}} = 35.3$ (if we didn't use the approximated Q)



6 [OPTIONAL] PERFORM PARAMETRIC SWEEP: CL = 2p, 4p, 8p.

6.1 REPORT VOUT VS TIME OVERLAID ON SAME PLOT.



6.2 REPORT THE OVERSHOOT VS CL.

Parameters: CL=2p					
1	LAB4_lab_1	VT("/VOUT")			
1	LAB4_lab_1	VT("/VIN")			
1	LAB4_lab_1	VT("/VSIG")			
1	LAB4_lab_1	overshoot(VT("/...))		35.15	
Parameters: CL=4p					
2	LAB4_lab_1	VT("/VOUT")			
2	LAB4_lab_1	VT("/VIN")			
2	LAB4_lab_1	VT("/VSIG")			
2	LAB4_lab_1	overshoot(VT("/...))		29.58	
Parameters: CL=8p					
3	LAB4_lab_1	VT("/VOUT")			
3	LAB4_lab_1	VT("/VIN")			
3	LAB4_lab_1	VT("/VSIG")			
3	LAB4_lab_1	overshoot(VT("/...))		20.29	



6.3 COMMENT

AS CL increases, the overshoot decreases

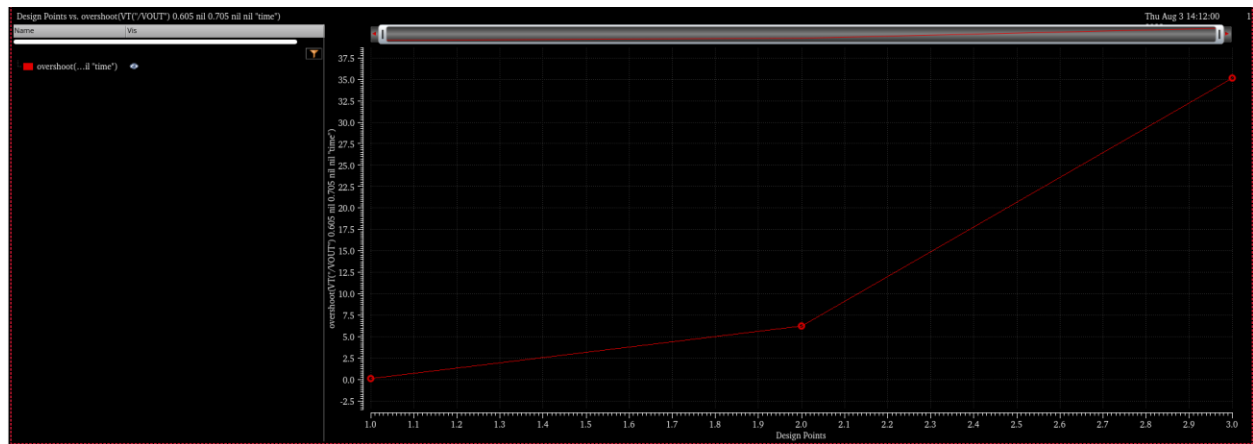
7 [OPTIONAL] PERFORM PARAMETRIC SWEEP: RSIG = 20K, 200K, 2M

7.1 REPORT VOUT VS TIME OVERLAID ON SAME PLOT.



7.2 REPORT THE OVERSHOOT VS RSIG

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: RSIG=20K						
1	LAB4_lab_1	VT("/VOUT")				
1	LAB4_lab_1	VT("/VIN")				
1	LAB4_lab_1	VT("/VSIG")				
1	LAB4_lab_1	overshoot(VT("/V...	106.2m			
Parameters: RSIG=200K						
2	LAB4_lab_1	VT("/VOUT")				
2	LAB4_lab_1	VT("/VIN")				
2	LAB4_lab_1	VT("/VSIG")				
2	LAB4_lab_1	overshoot(VT("/V...	6.235			
Parameters: RSIG=2M						
3	LAB4_lab_1	VT("/VOUT")				
3	LAB4_lab_1	VT("/VIN")				
3	LAB4_lab_1	VT("/VSIG")				
3	LAB4_lab_1	overshoot(VT("/V...	35.15			

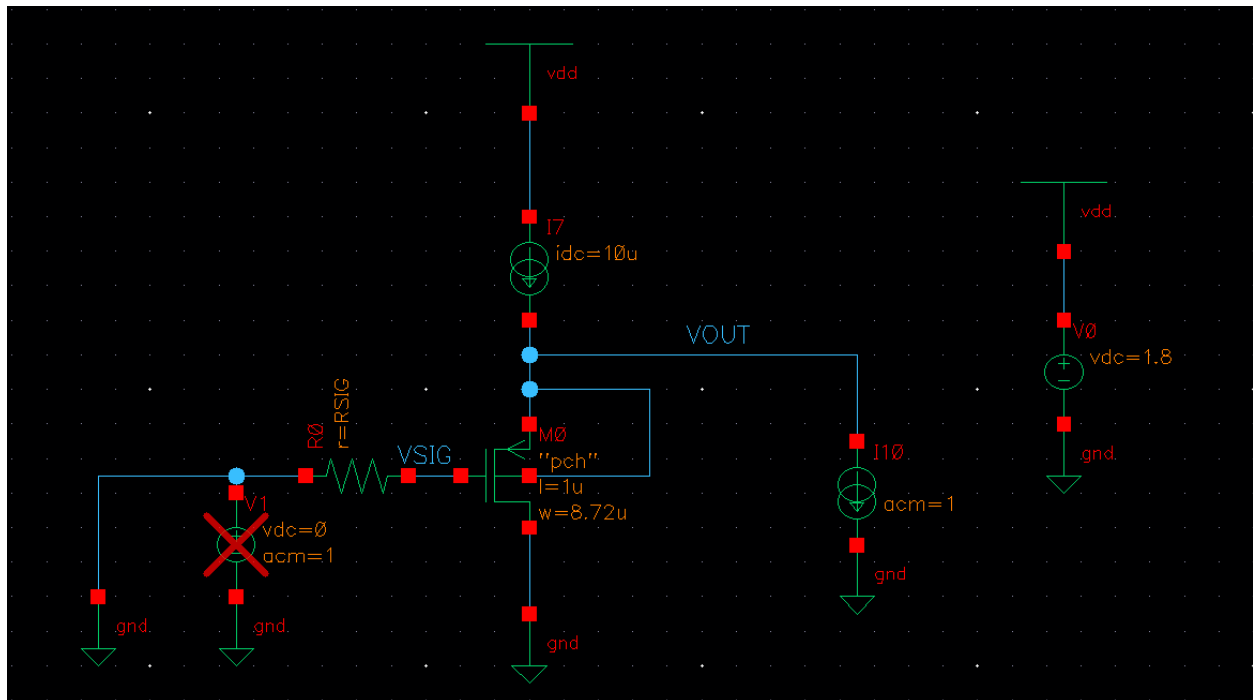


7.3 COMMENT

AS R_{sig} increases, the overshoot increases and at low impedance we can see there is almost no overshoot.

Z_{out} (Inductive Rise)

- 1 WE WANT TO SIMULATE THE CD AMPLIFIER OUTPUT IMPEDANCE.
REPLACE C_L WITH AN AC CURRENT SOURCE WITH MAGNITUDE = 1.
REMOVE THE AC INPUT SIGNAL.



- 2 PERFORM AC ANALYSIS (1Hz:10GHz, LOGARITHMIC, 10POINTS/DECADE). THE VOLTAGE ACROSS THE AC CURRENT SOURCE IS ITSELF THE OUTPUT IMPEDANCE.
-

Choosing Analyses -- ADE Assembler

Analysis

☐ tran

☐ dc

☒ ac

☐ noise

☐ xf

☐ sens

☐ dcmatch

☐ acmatch

☐ stb

☐ pz

☐ lf

☐ sp

☐ envlp

☐ pss

☐ pac

☐ pstb

☐ pnoise

☐ pxf

☐ psp

☐ qpss

☐ qpac

☐ qpnoise

☐ qpxf

☐ qpsp

☐ hb

☐ hbac

☐ hbstb

☐ hbnoise

☐ hbasp

☐ hbxf

AC Analysis

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

Sweep Range

☒ Start-Stop

☐ Center-Span

Start

1

Stop

10G

Sweep Type

Logarithmic

☒ Points Per Decade

10

☐ Number of Steps

Add Specific Points

☐

Add Points By File

☐

Specialized Analyses

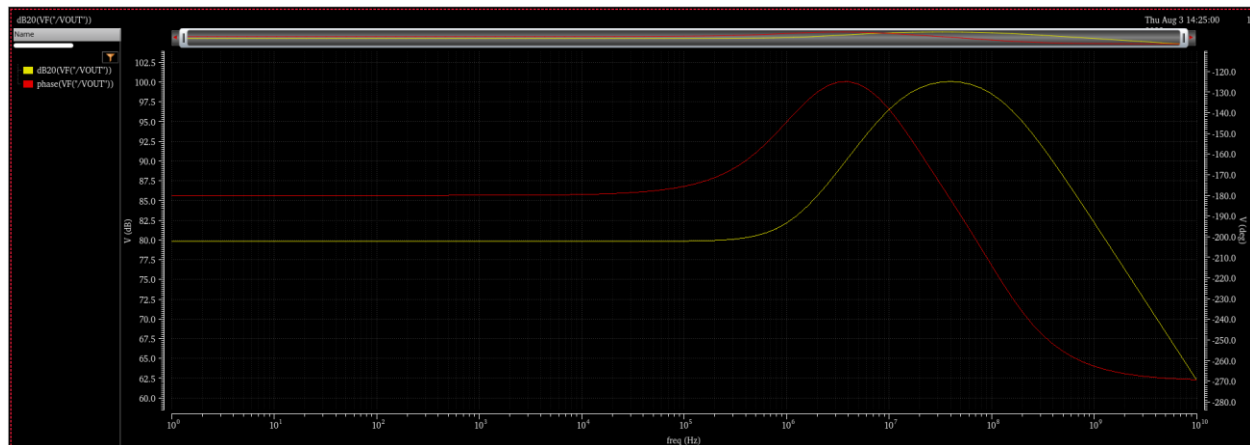
None

Enabled

☒

Options...

3 PLOT THE OUTPUT IMPEDANCE (MAGNITUDE AND PHASE) VS FREQUENCY. DO YOU NOTICE AN INDUCTIVE RISE? WHY?



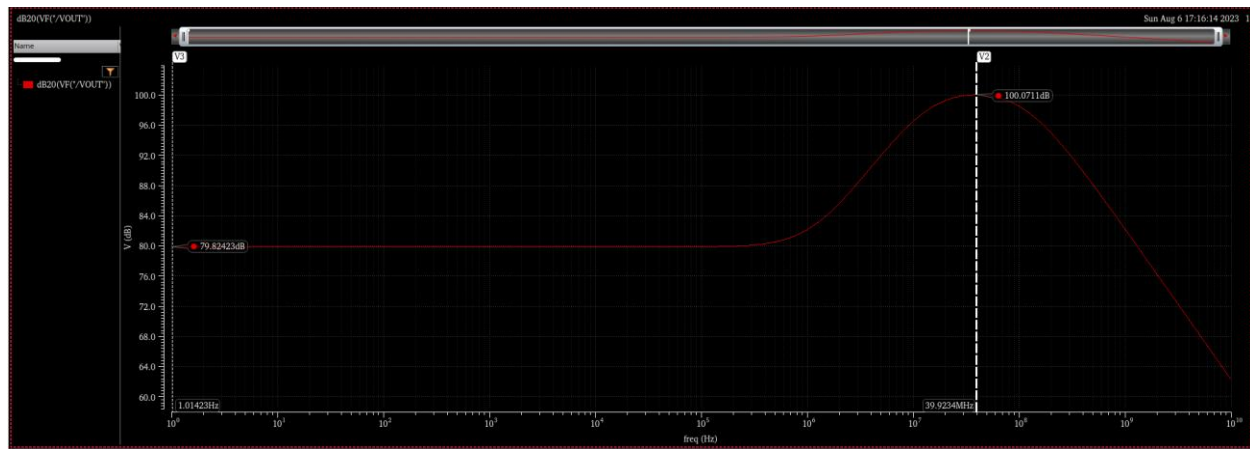
Yes, as $\omega z < \omega p$, because $1/g_m < R_{sig}$, so the zero causes a 20dB/dec rise like inductor (with increasing frequency the impedance increases).

4 DOES Z_{out} FALL AT HIGH FREQUENCY? WHY?

Yes, AS at high frequency a pole with C_{gs} appears after the pole with c_{gd} and because of these two poles after the zero we have a fall with -20 db/dec at high frequency.

5 ANALYTICALLY CALCULATE THE ZEROS, POLES, AND MAGNITUDE AT LOW/HIGH FREQUENCY FOR Z_{out} . COMPARE WITH SIMULATION RESULTS IN A TABLE.

Poles (Hz)			
	Real	Imaginary	Qfactor
1	-1.34828e+07	0.00000e+00	5.00000e-01
2	-1.15850e+08	0.00000e+00	5.00000e-01
Zeros (Hz) at $V(V_{OUT},0)/I_{12}$			
	Real	Imaginary	Qfactor
1	-1.17422e+06	0.00000e+00	5.00000e-01



subject - 1 موضوع الدرس

$$S_z = \frac{-1}{R_{sig} C_{gs}} = -8,47 \text{ MVad/s}$$

$$\Rightarrow f_z = 1,34 \text{ MHz}$$

$$S_{P1} = \frac{-(g_m + g_{ds})}{R_{sig} g_{ds} C_{gs} + C_{gs}} = -651,6 \text{ MVad/s}$$

$$\Rightarrow f_{P1} = 103,7 \text{ MHz}$$

$$S_{P2} = \frac{-1}{R_{sig} C_{gd}} = -86,97 \text{ MVad/s}$$

$$\Rightarrow f_{P2} = 13,8 \text{ MHz}$$

AT low fVer $Z_{out} = \frac{1}{\frac{1}{g_m} \parallel Y_o}$

$$\text{So } Z_{out} = 9,8 \text{ k}\Omega$$

$$20 \log(9,8 \text{ K}) = 79,8 \text{ Db}$$

AT High fVer $Z_{out} = R_{sig} \parallel Y_o = 753,2 \text{ K}\Omega$

$$20 \log(753,2 \text{ K}) = 117,54 \text{ Db}$$

El Salam

	Analytical	Sim
Zero	1.34 MHZ	1.17 MHZ
Pole1	13.8 MHZ	13.48 MHZ
Pole2	103.7 MHZ	115.85 MHZ
Zout LF	79.8 DB	79.8 DB
Zout Hf	117.54 DB	100.07 DB