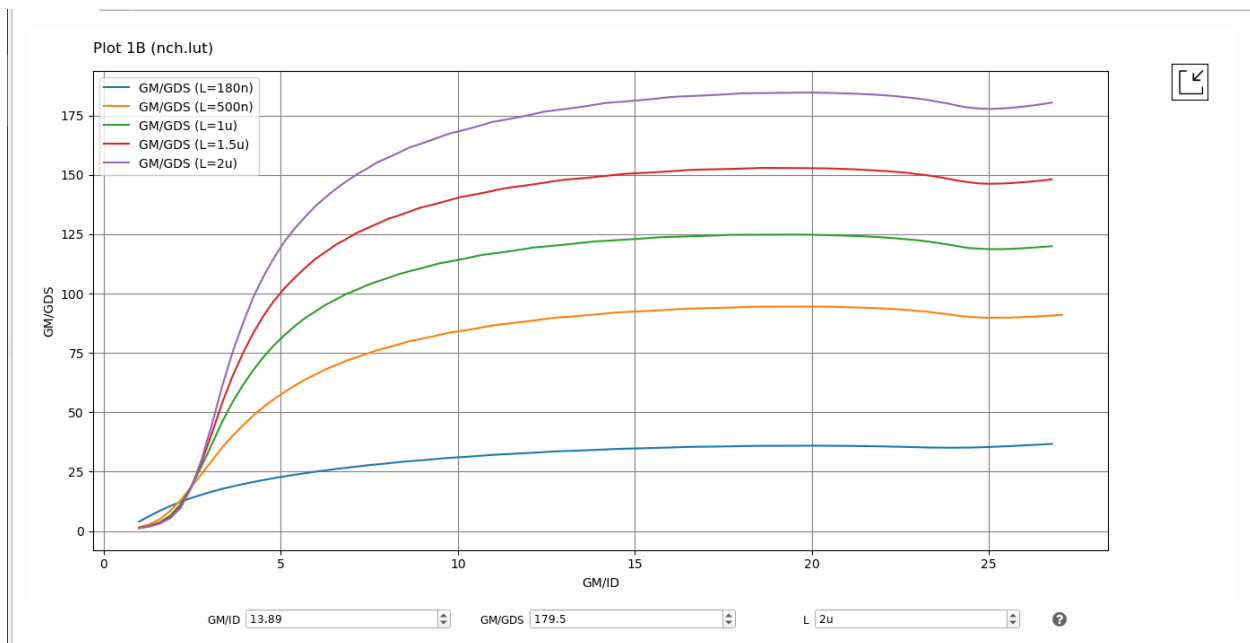


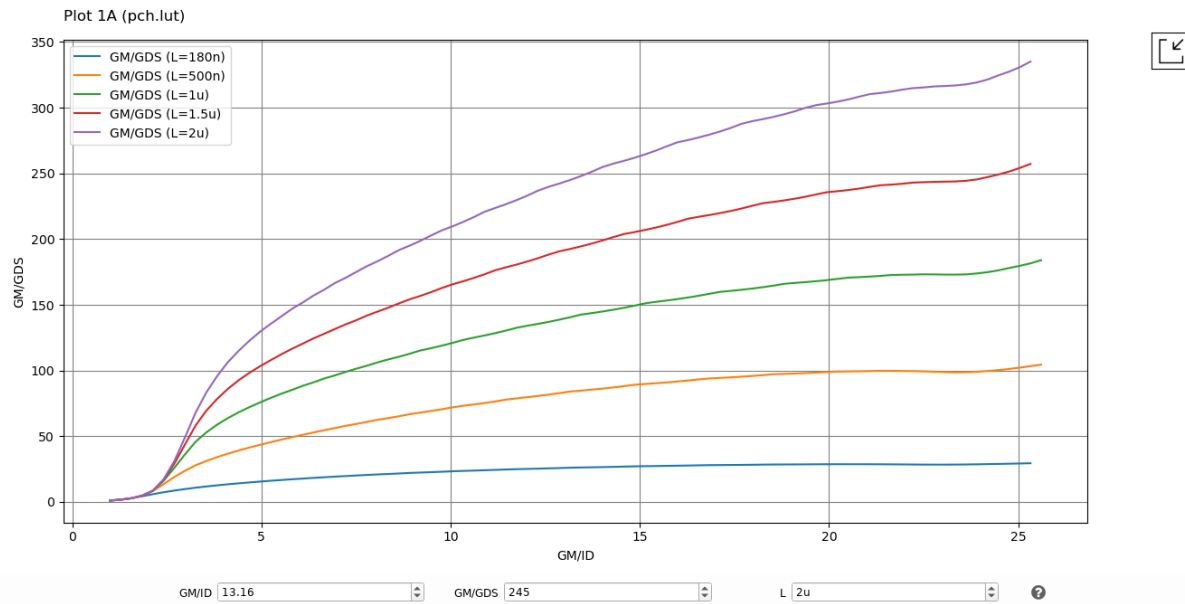
# Part1

- 1 USING ADT DEVICE XPLORE, PLOT THE FOLLOWING DESIGN CHARTS VS  $GM/ID$  FOR BOTH PMOS AND NMOS. SET  $V_{DS} = V_{DD}/3$  AND  $L = 0.18\mu, 0.5\mu, 1\mu, 2\mu$

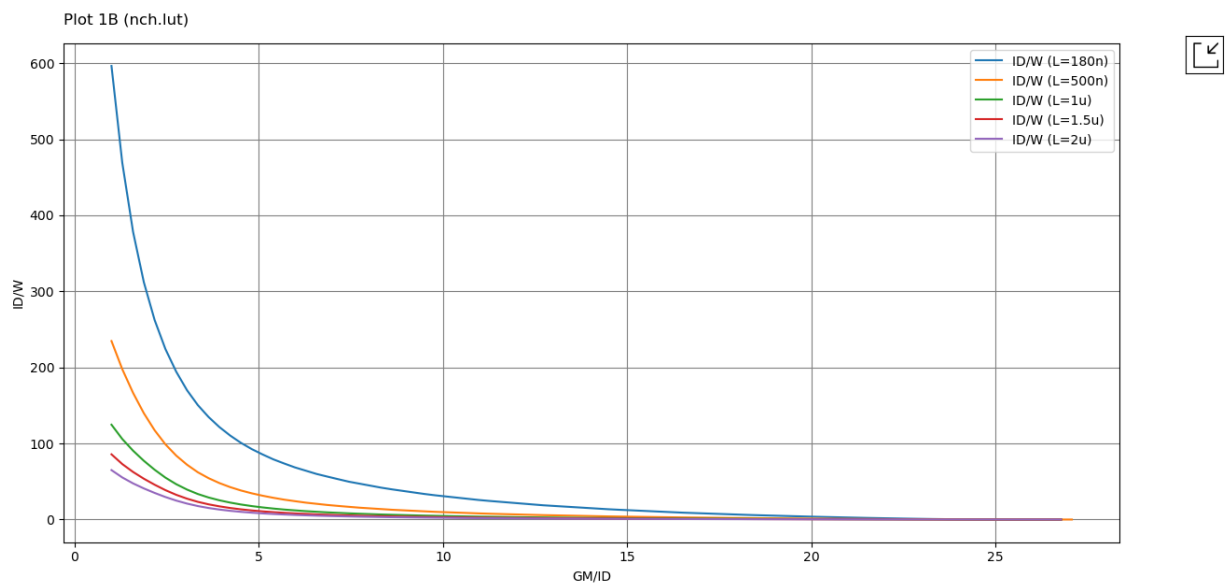
## 1.1 $GM/G_{DS}$ NMOS



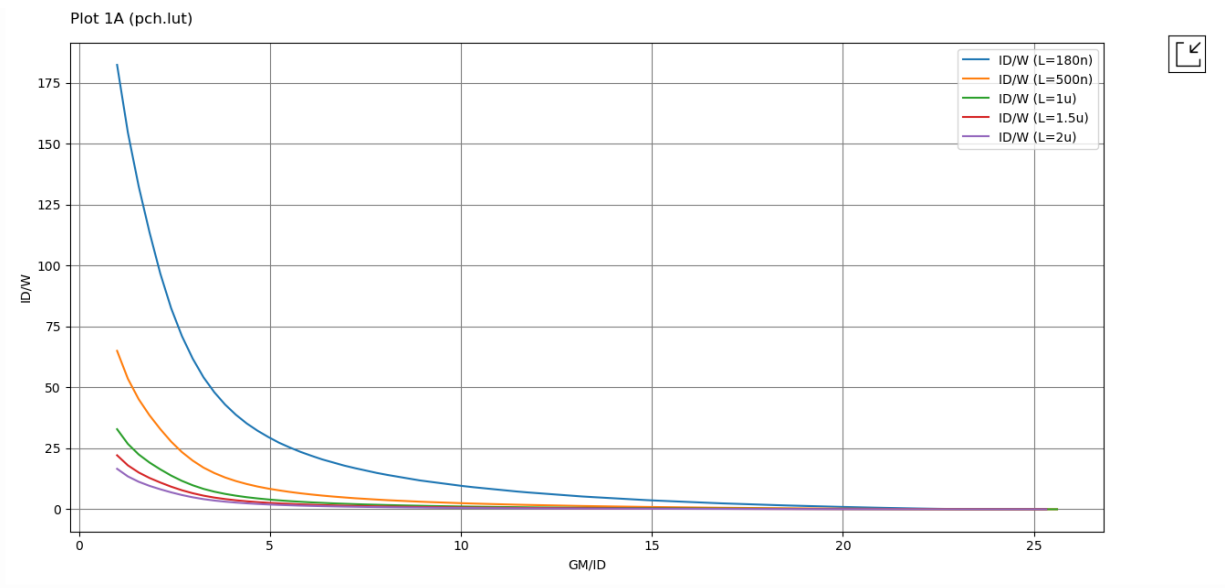
## PMOS



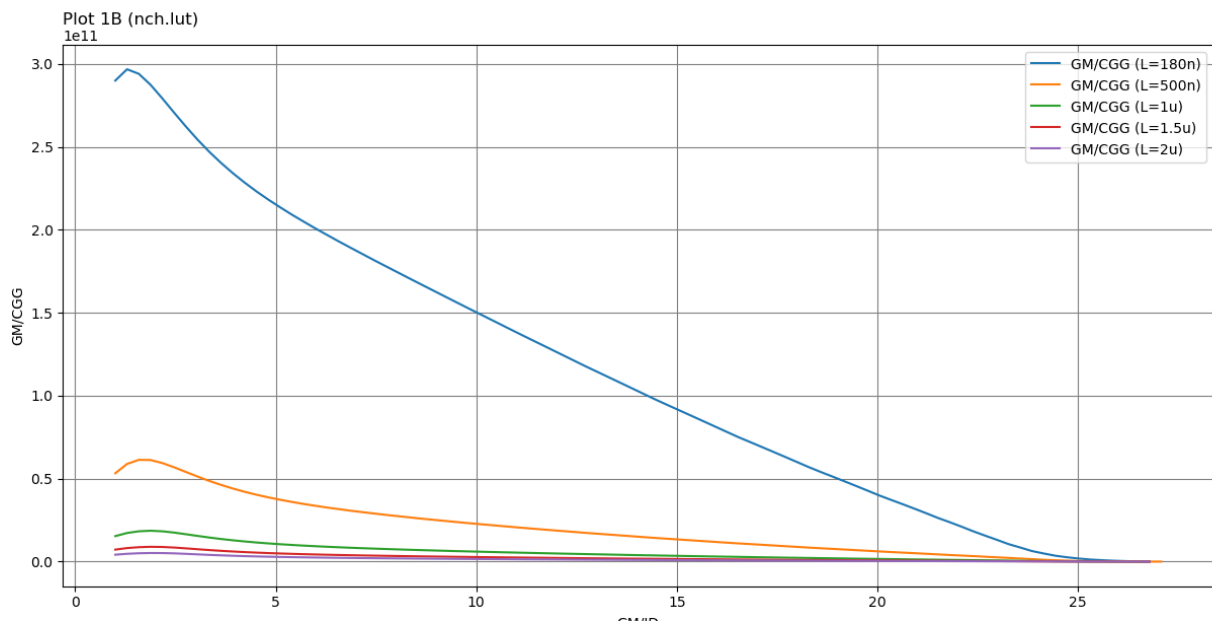
## 1.2 ID/W NMOS



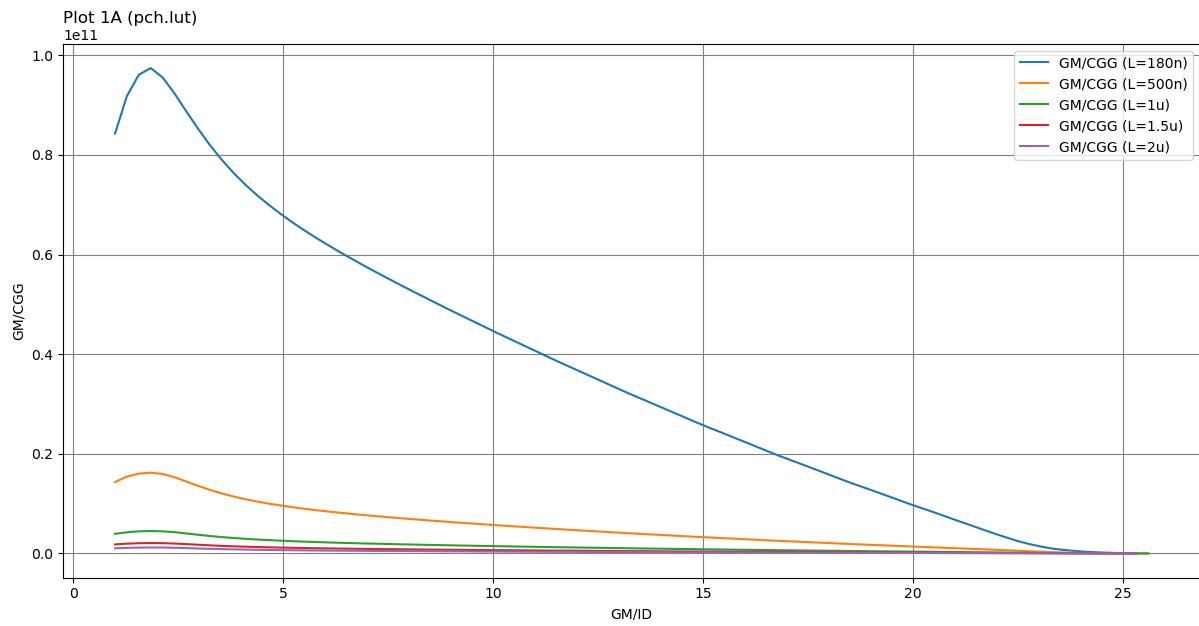
## PMOS



### 1.3 $GM/CGG$ NMOS

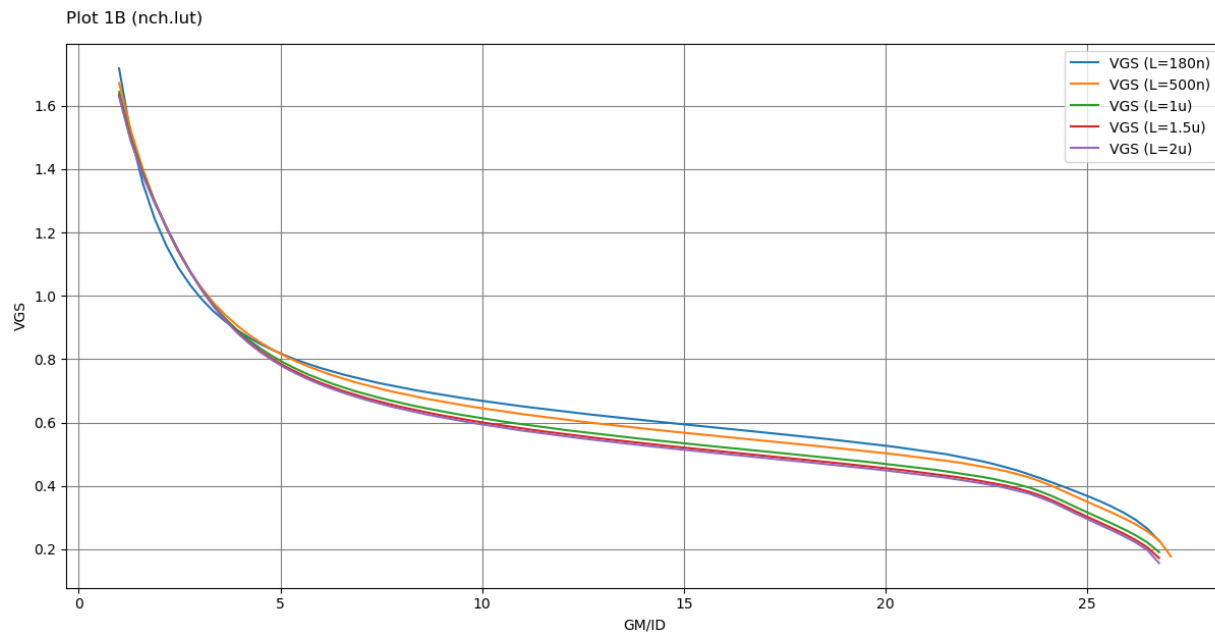


PMOS

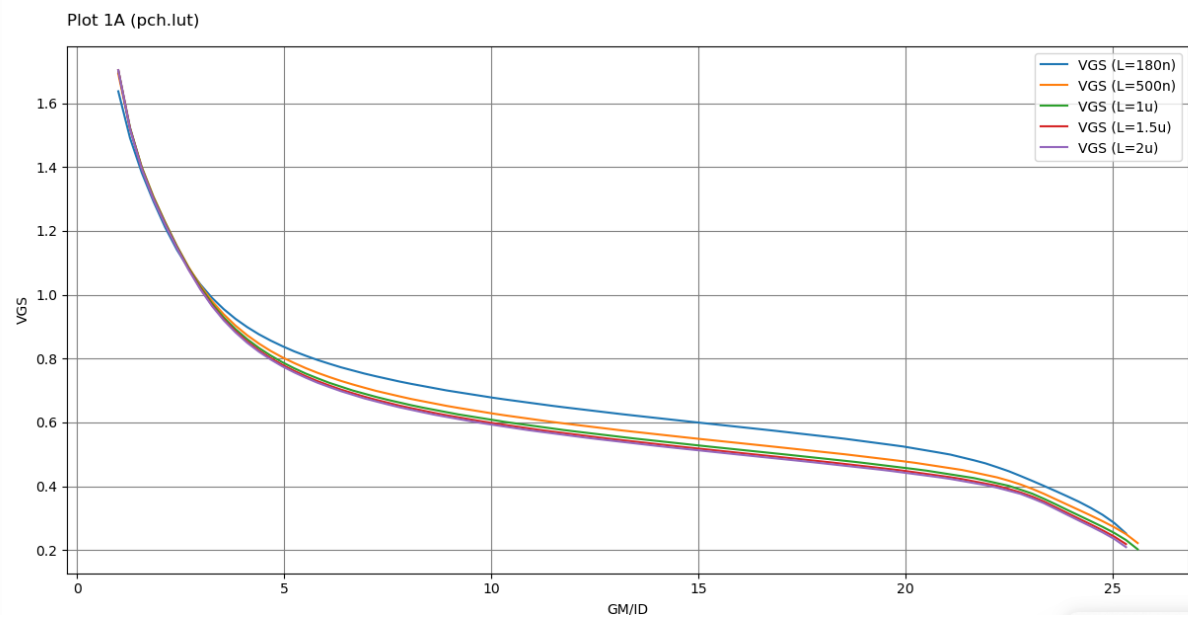


## 1.4 VGS

### Nmos



PMOS



## PART2

### 1 DETAILED DESIGN PROCEDURE AND HAND ANALYSIS.

#### 1.1 DESIGN OF INPUT PAIR

Subject: موضوع الدرس Date: التاريخ

$1,5$   
 $0,8$

$1,8$   
 $0V$

$V_{in} \text{ et } 0,8 < V_{cm} < 1,5$   
 $0,8V$        $1,8 - 1,5 = 0,3V$

So we will use NMOS Pair Topology.

Design of Input Pairs

We will Assume  $V_{DS} = \frac{1,8}{3} = 0,6V$

from the Specs  $\Rightarrow GBW = 5MHz \Rightarrow$

$\frac{g_{m1,2}}{2\pi C_L} = 5MHz \Rightarrow g_{m1,2} \approx 160\mu S$

Subject موضوع الدرس

$$\frac{g_m}{I_D} \approx \frac{160 \mu}{10 \mu} = 16$$

Date

التاريخ

From the specs  $\Rightarrow A_{v_{Di}} > 34 \text{ dB} \Rightarrow 50$

$$50 \Rightarrow 50 > \frac{g_m}{2g_{ds}} \Rightarrow \frac{g_m}{g_{ds}} > 100$$

$$g_{ds} < 1.6 \mu \text{S}$$

From the chart we found that the first  $L$  to give  $g_{ds} < 1.6 \mu \text{S}$

$$\textcircled{2} \frac{g_m}{I_D} \approx 16 \text{ is } \boxed{0.7 \mu}$$

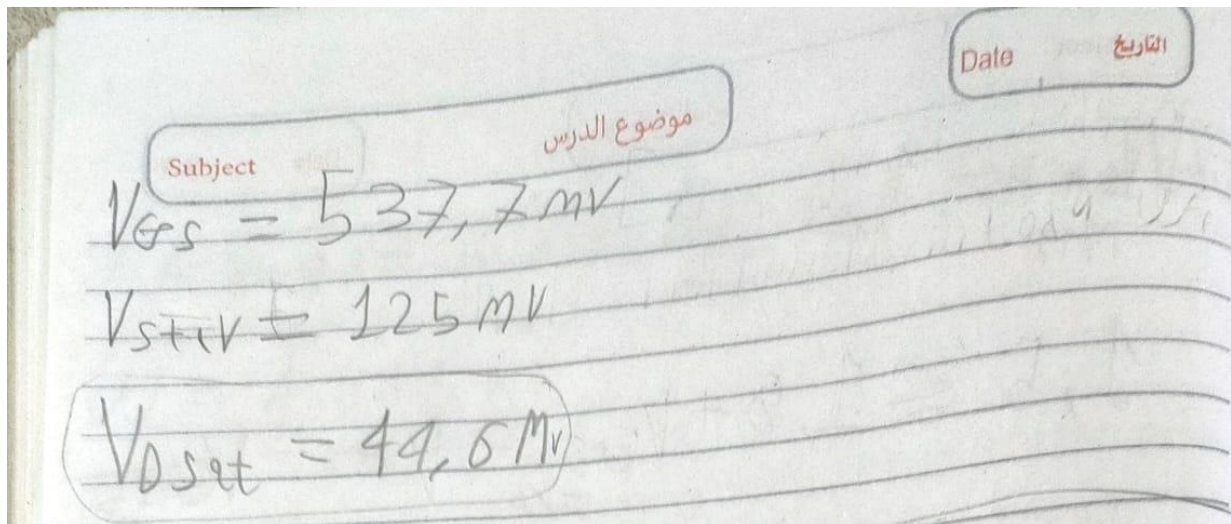
So we swept  $W$  vs  $\frac{g_m}{I_D}$  at constant  $L = 0.7 \mu$

$$\text{and Found } \boxed{W = 4.057 \mu}$$

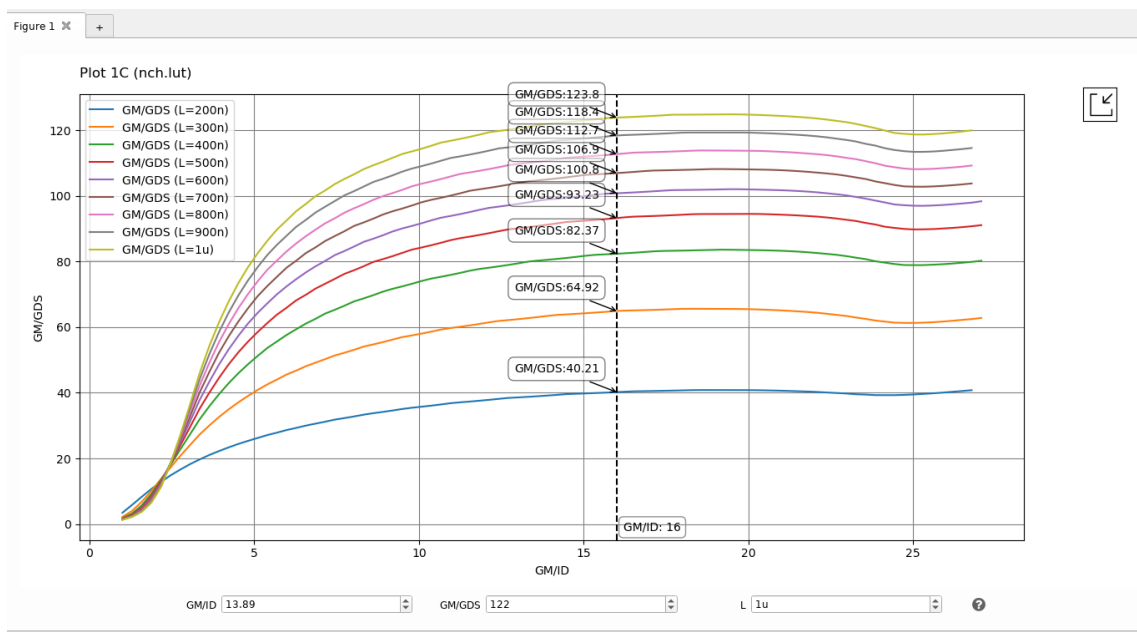
We swept  $V_{GS}$  2 Times one with considering body effect = 600mV, and another without

Elsham

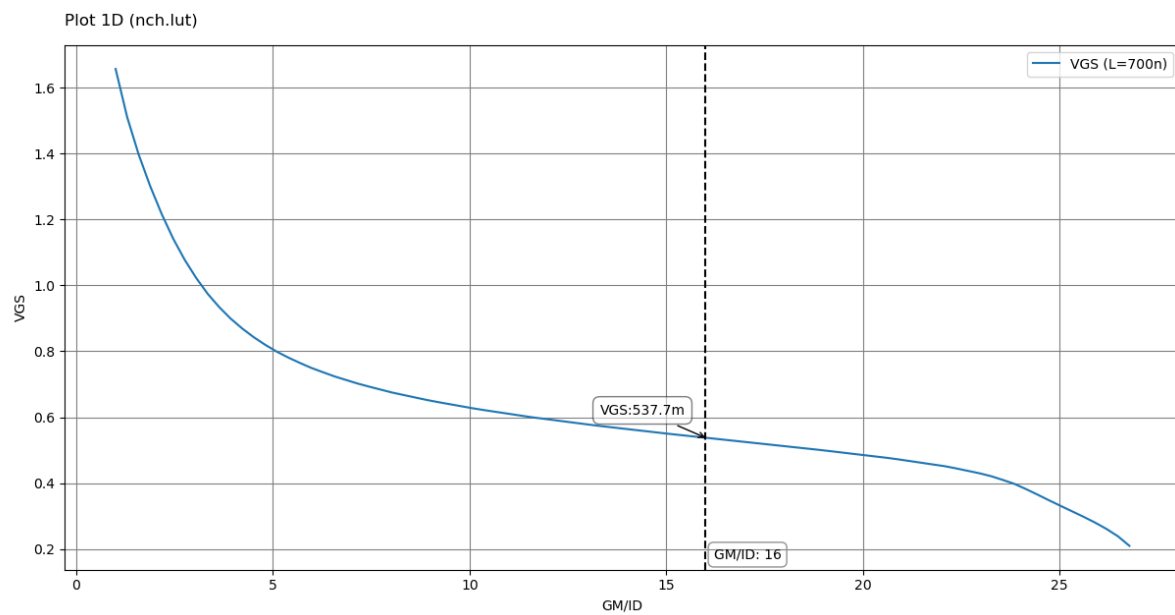
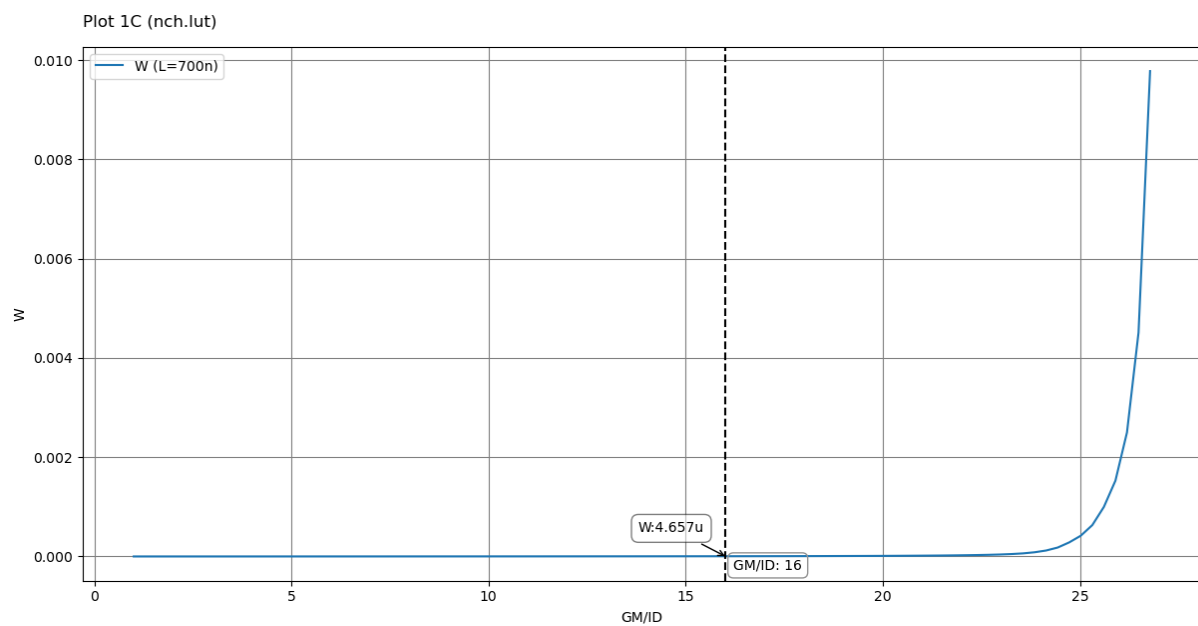


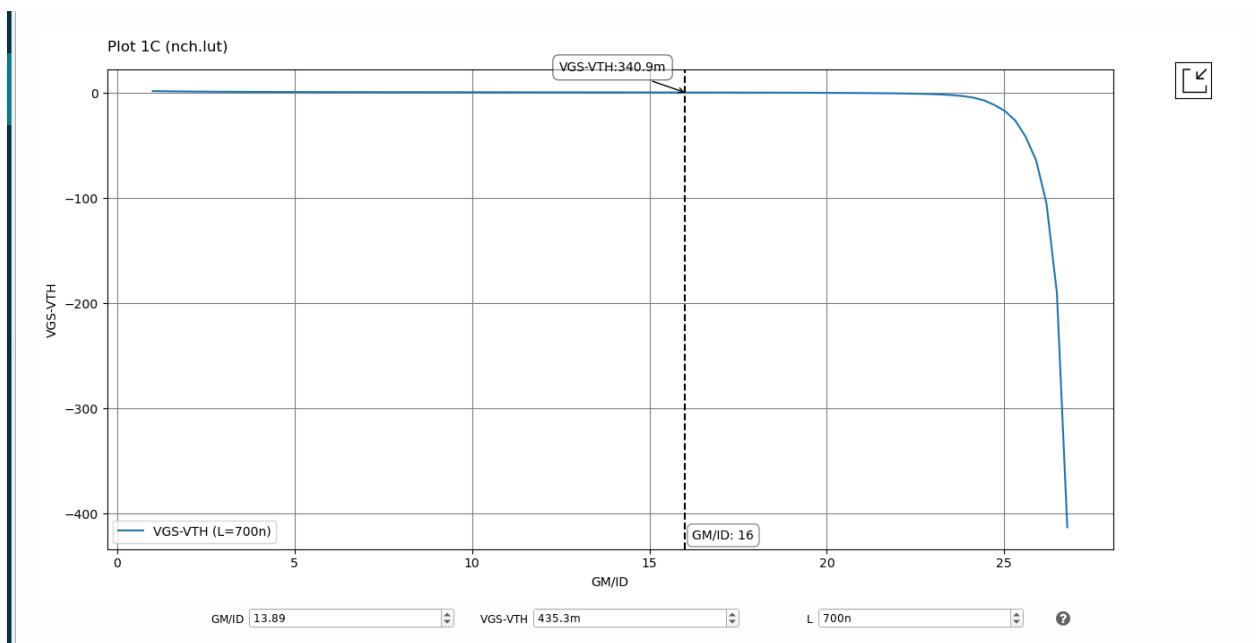
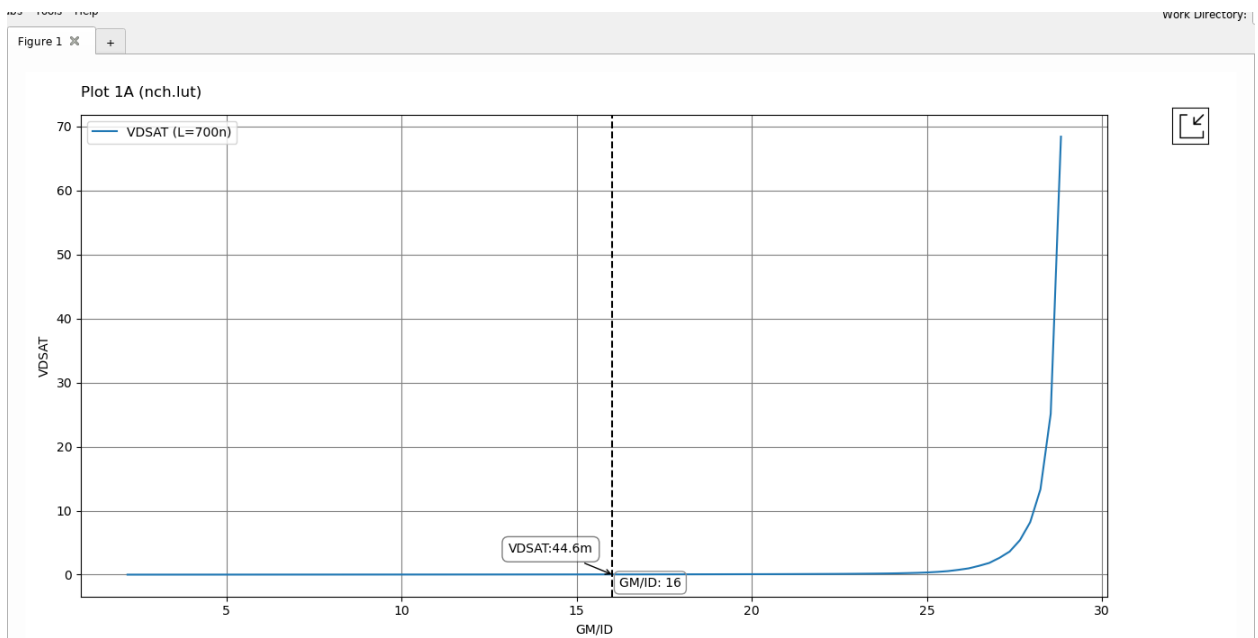


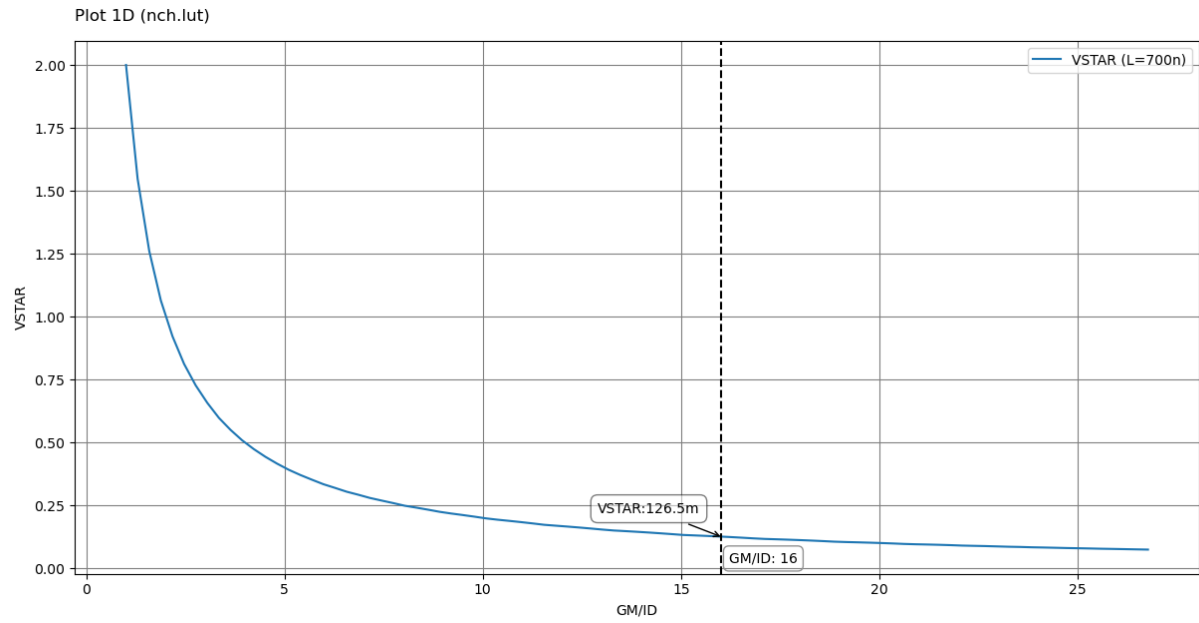
## CHARTS:











## 1.2 DESIGN OF MIRROR LOAD

Design of Mirror Load

We Assumed  $I_{ds} = I_{ds} < 1,6 \mu S$   
i/p mirror

$$I_{ds} = \frac{I_D}{V_A} \Rightarrow \boxed{V_A > 6,25}$$

To find  $L$  from the chart we should

assume  $\frac{I_M}{I_D}$ , so we assumed  $\frac{I_M}{I_D} = 10$

[a large value so we make sure the  $V_{eff}$   $\frac{I_M}{I_D}$  would achieve the requirement]

We found that  $\boxed{L \geq 0,6 \mu m}$

$$V_{icm} \geq 1,5$$

MAX

$$1,5 \leq 1,8 + V_{GS} - V_{th} - V_{GS3}$$

I/P

$$V_{GS3} \leq 0,3 + V_{GS} - V_{th}$$

$$V_{GS3} \leq 300 + 537,7 - 125$$

$$V_{GS3} \leq 712,7 \Rightarrow V_{GS} = 712,7 \text{ mV}$$

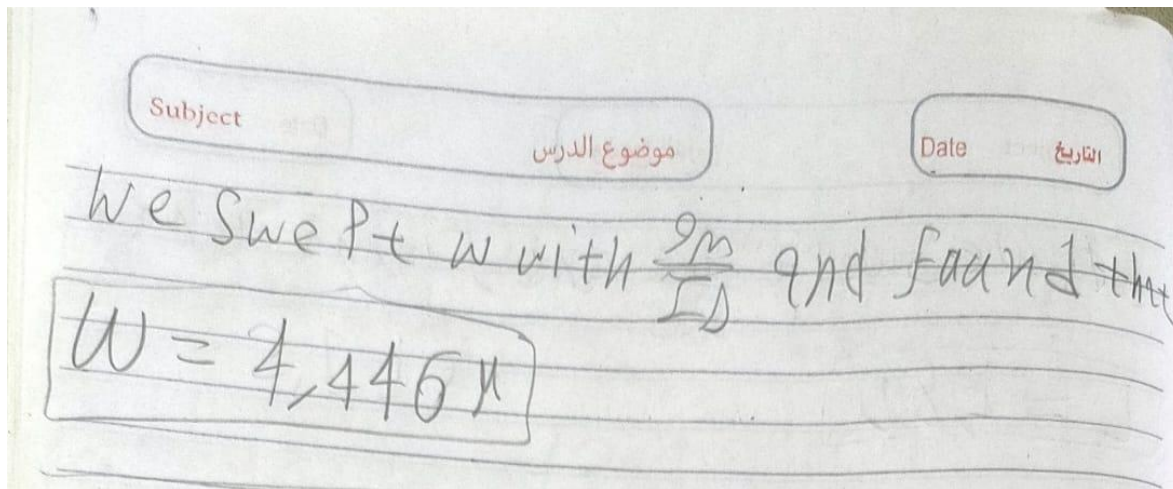
MAX

So to find  $\frac{g_m}{I_D \text{ min}}$  we swept  $V_{GS}$ .

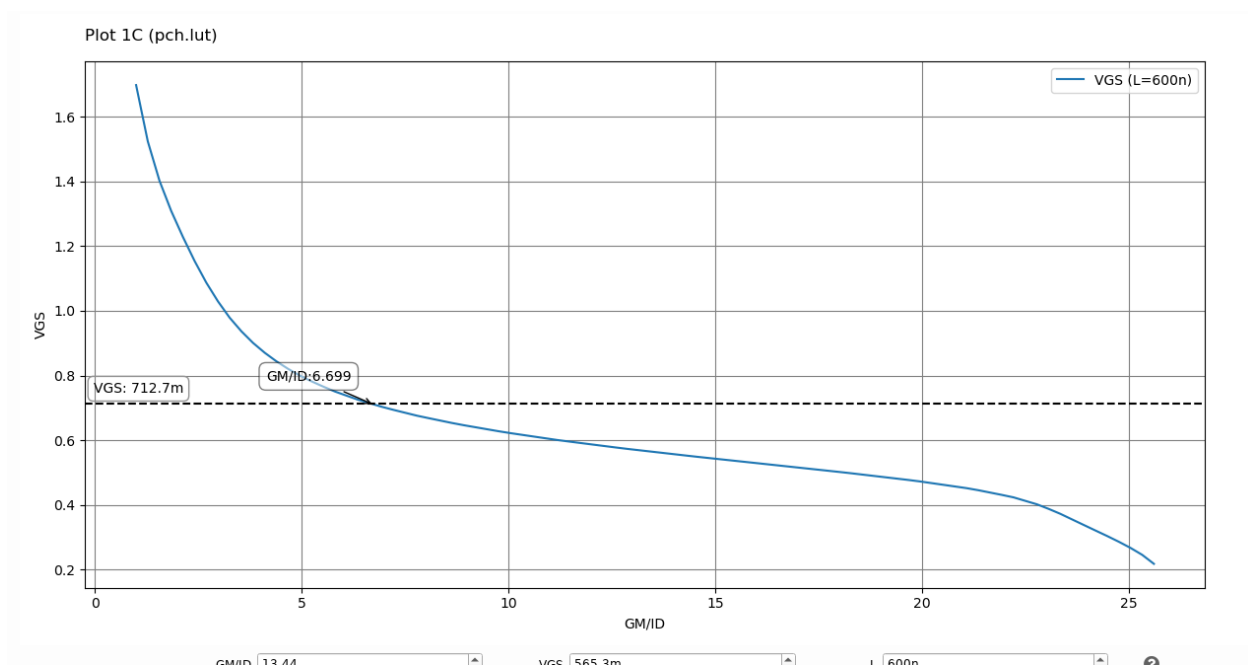
With  $\frac{g_m}{I_D}$ , we found  $\left(\frac{g_m}{I_D}\right)_{\text{min}} = 6,7$

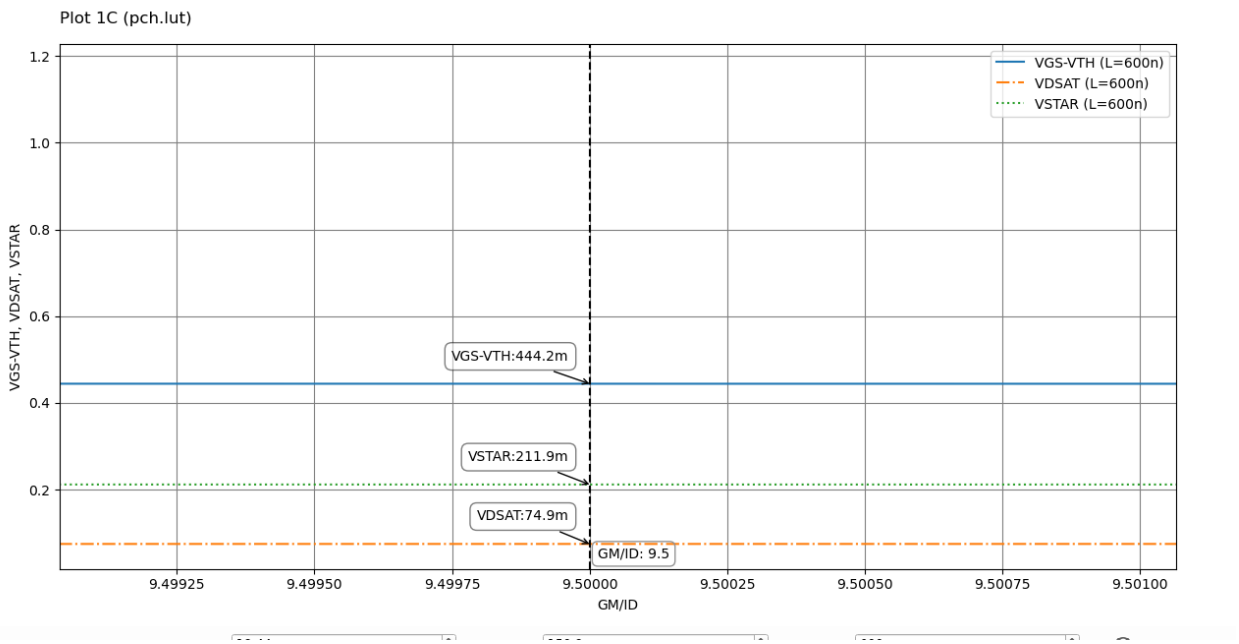
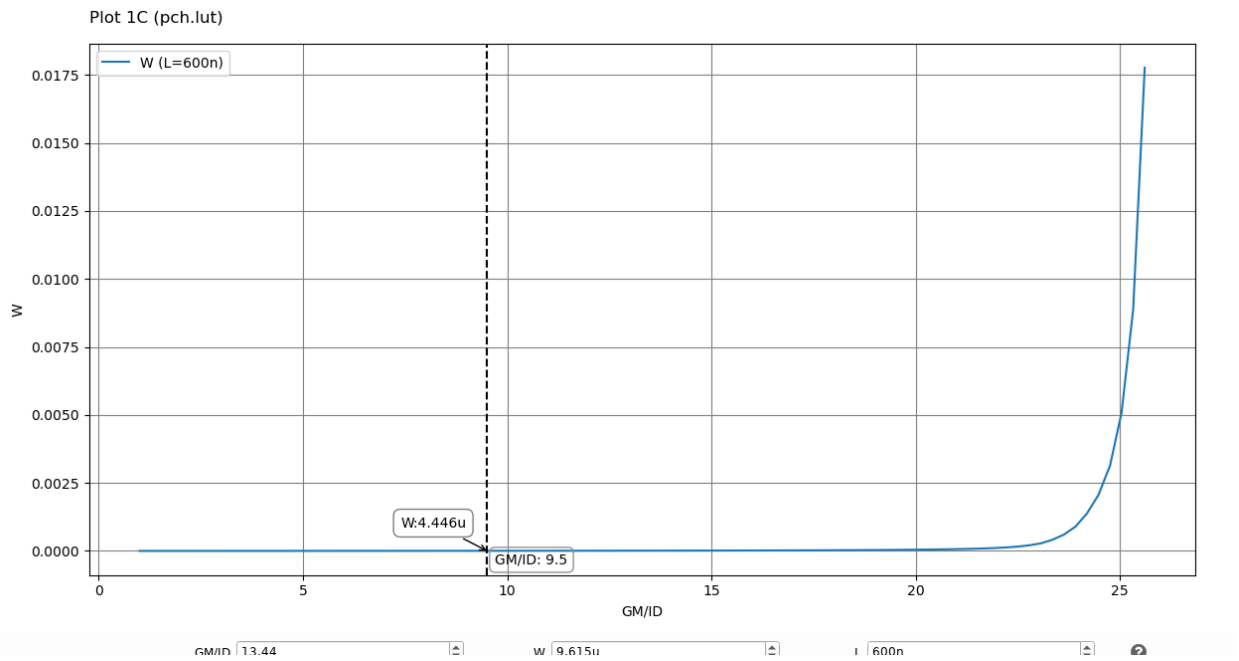
We took 9 margin so  $\left(\frac{g_m}{I_D}\right) = 9,5$

We took 9 margin so  $\left(\frac{g_m}{I_D}\right)$



## CHARTS:







### 1.3 DESIGN OF TAIL CURRENT SOURCE

Design of Tail:

$$CMRR = 74 \text{ dB}, A_{VDI} = 34 \text{ dB}$$

$$A_{VCM} = A_{VD} - CMRR = -40 \text{ dB}$$

$$\approx 0,01$$

$$A_{VCM} = 0,01 = \frac{1}{\frac{2I_{M3,4}}{3,1} R_{EE}} \approx \frac{I_{DS}}{2I_{M3,4}}$$

$$I_{M3,4} = 95 \mu A \Rightarrow I_{DS} < 1,9 \mu A$$

$$\text{We Assumed } \frac{I_M}{I_D} = 15 \Rightarrow \frac{I_M}{I_{DS}} > 157,89$$

So we swept  $\frac{I_M}{I_D}$  and found that

$$L = 1,8 \mu$$

$$V_{in_{cm}} = 0,8 V$$

$$V_{icm} \geq V_{GS1} + V_S$$

$$800 \geq 537,7 + V_S$$

$$262,3 \geq V_S \Rightarrow V_{S_{sit MAX}} = 262,3$$

We swept and found that  $\frac{I_M}{I_D} = 16,53$

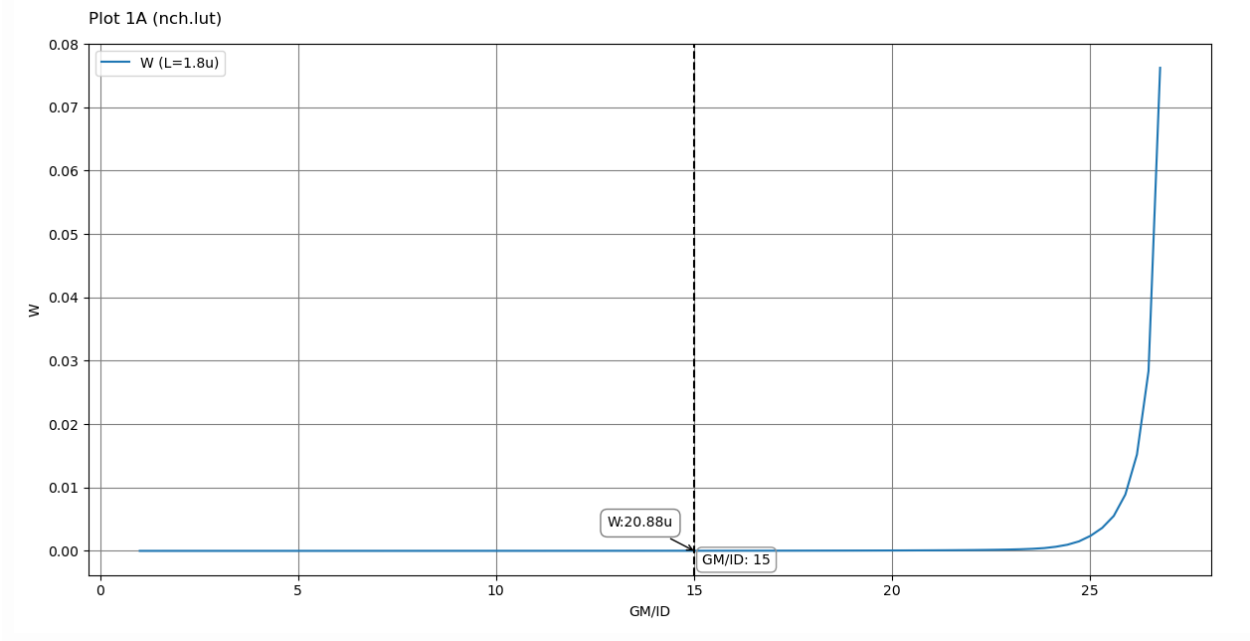
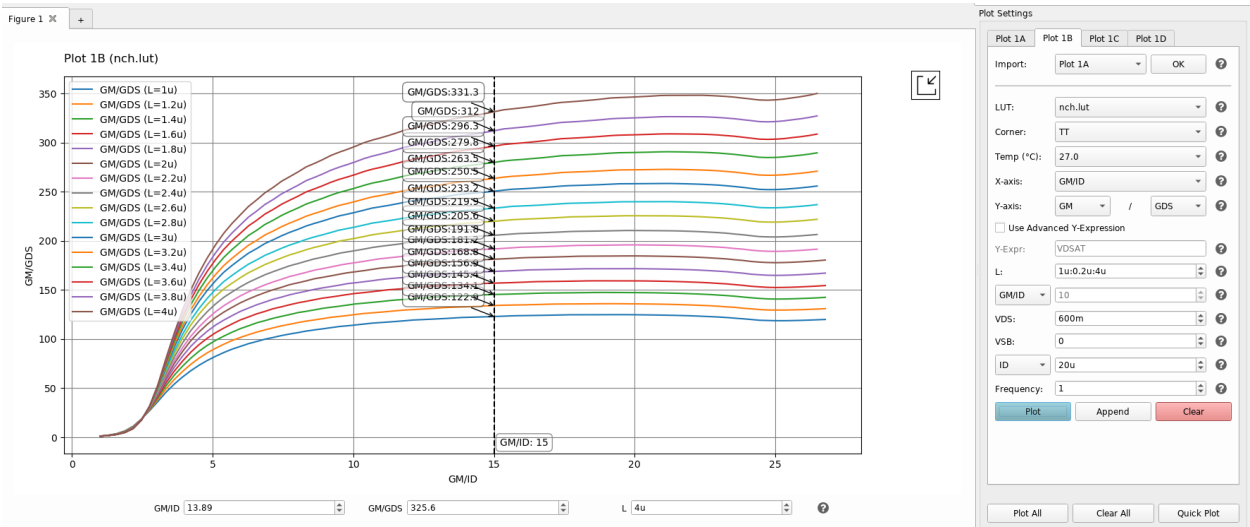
$$\text{Keep some Margin: } \left( \frac{I_M}{I_D} = 15 \right)$$

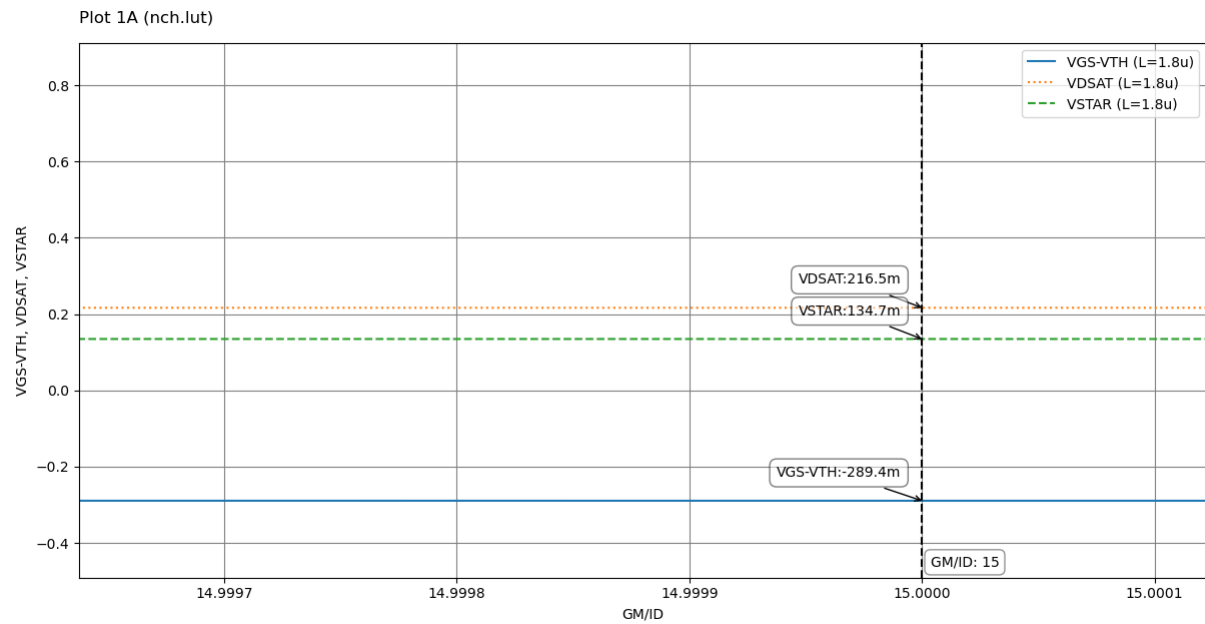
$$W = 20,88 \mu \text{ at } 20 \text{ mA}$$

$$W \text{ for Half the current } \frac{W}{2} = 10,44 \mu$$

El Salam

# CHARTS:



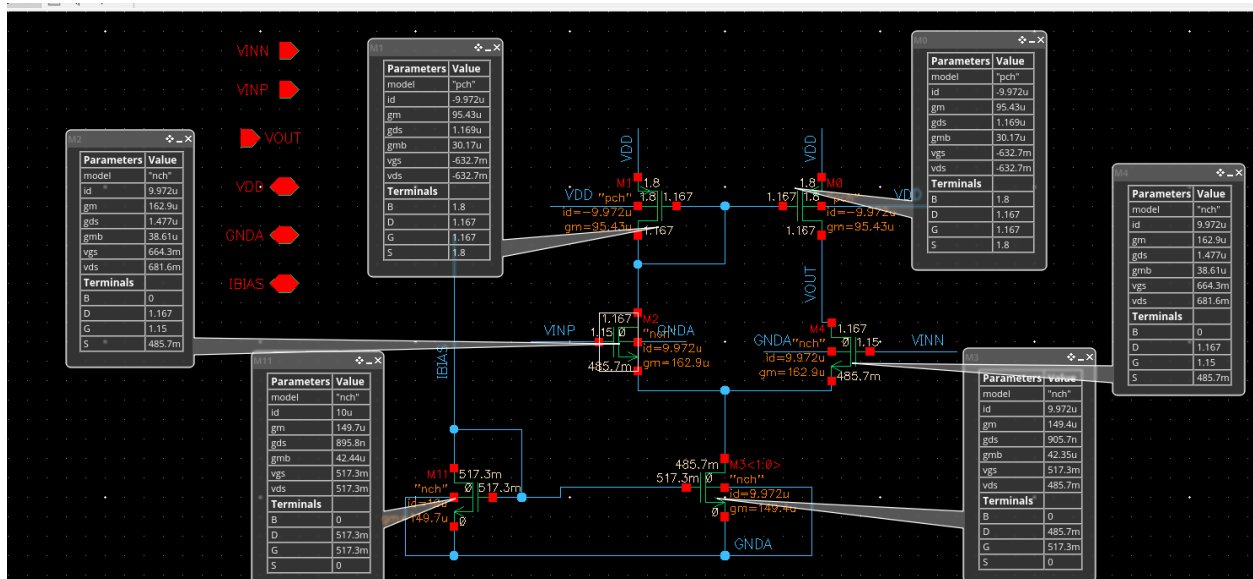
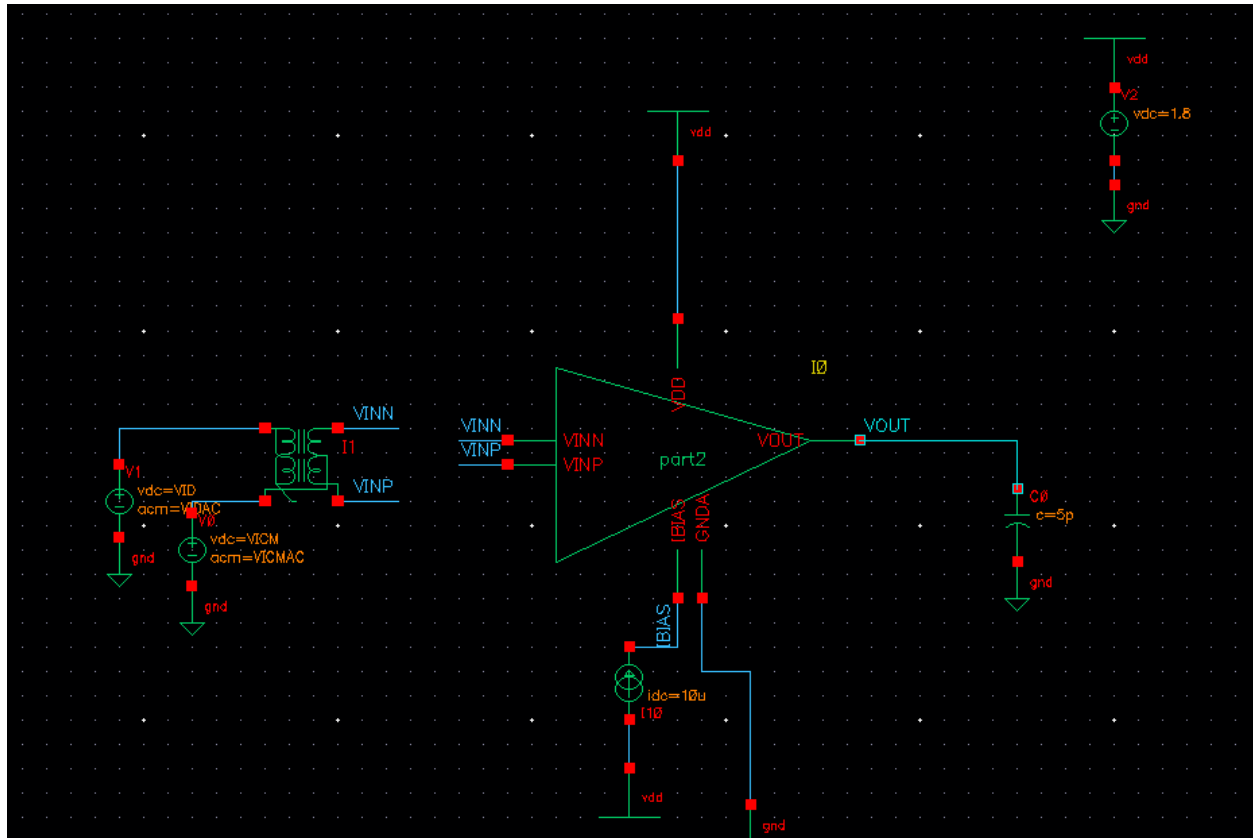


2 A TABLE SHOWING  $W$ ,  $L$ ,  $gm$ ,  $ID$ ,  $gm/ID$ ,  $VDSsat$ ,  $Vov = VGS - VTH$ , AND  $V^* = 2ID/gm$  OF ALL TRANSISTORS (AS CALCULATED FROM  $GM/ID$  CURVES)

TRANS	W	L	GM	ID	GM/ID	VDSsat	VOV	VSTAR
Input pair	4.657u	0.7u	160u	10u	16	44.6m	340.9m	125m
MIRROR LOAD	4.446u	0.6u	95u	10u	9.5	74.9m	444.2m	211.9m
TAIL CURRENT SOURCE	with 20u 20.88 with 10u 10.44u	1.8u	300u	20u	15	216.5m	-298.4m	134.7m

# PART3

## 1 SCHEMATIC OF THE OTA WITH DC NODE VOLTAGES CLEARLY ANNOTATED



The tail current source transistor is made of array of two transistors and the sizing shown is of one of the unit transistor of them.

1.1 USE VICM AT THE MIDDLE OF THE CMIR.

$$(1.5+0.8)/2=1.15V$$

1.2 IS THE CURRENT (AND GM) IN THE INPUT PAIR EXACTLY EQUAL?

YES,  $i_d=9.972\mu$   $g_m=162.9\mu$

1.3 WHAT IS DC VOLTAGE AT VOUT? WHY?

1.167v, as  $V_{OUT}=V_{DD}-V_{GS}(0)$  and M0 follow M1 and it is diode connected so  $V_{GS}(0)=V_{GS}(1)=V_{DS}$ ,  $1.8-0.632=1.167V$

## 2 DIFF SMALL SIGNAL CCS:

### 2.1 USE AC ANALYSIS (1Hz:10GHz, LOGARITHMIC, 10 POINTS/DECADE).

**Choosing Analyses -- ADE Explorer**

Analysis

☐ tran ☐ dc ☒ ac ☐ noise

☐ xf ☐ sens ☐ dcmatch ☐ acmatch

☐ stb ☐ pz ☐ lf ☐ sp

☐ envlp ☐ pss ☐ pac ☐ pstb

☐ pnoise ☐ pxf ☐ psp ☐ qpss

☐ qpac ☐ qpnoise ☐ qpxf ☐ qpssp

☐ hb ☐ hbac ☐ hbstb ☐ hbnoise

☐ hbasp ☐ hbxf

**AC Analysis**

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

Sweep Range

☒ Start-Stop Start  Stop

☐ Center-Span

Sweep Type

☒ Logarithmic ☐ Points Per Decade

☐ Number of Steps

Add Specific Points ☐

Add Points By File ☐

Specialized Analyses

Enabled ☒

Options...

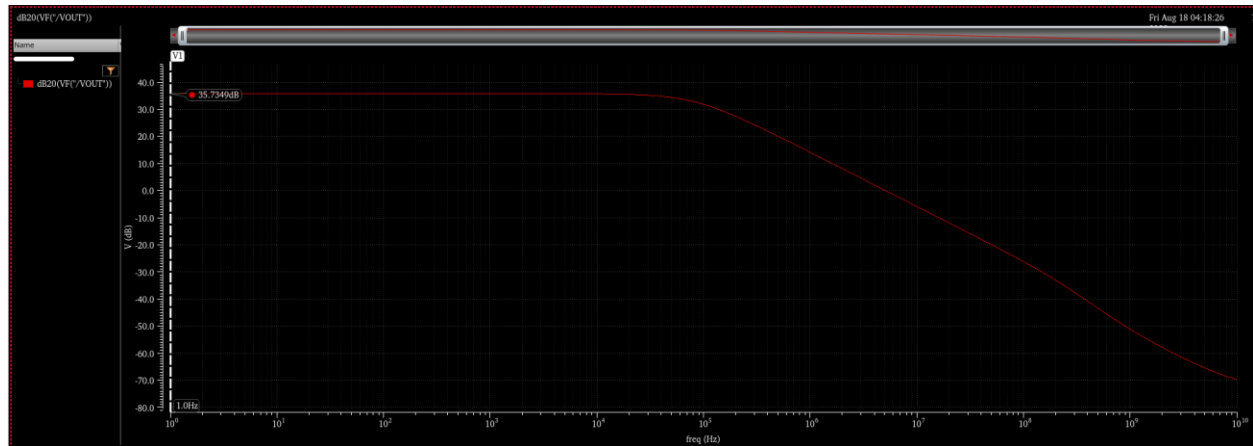
**OK** Cancel Defaults Apply Help

### 2.2 SET VIDAC = 1 AND VICMAC = 0 & USE VICM AT THE MIDDLE OF THE CMIR.

	VICM	1.15
	VICMAC	0
	VID	0
	VIDAC	1



## 2.3 PLOT DIFF GAIN (IN DB) VS FREQUENCY.



## 2.4 COMPARE SIMULATION RESULTS WITH HAND CALCULATIONS IN A TABLE

Subject موضوع الدرس Date التاريخ

$$A_{VD} = g_{m_{I/P}} \left[ \frac{1}{g_{ds_{I/P}} + g_{ds_{M1/M2}}} \right] = \frac{g_m}{2g_{ds}} = \frac{106.9}{2}$$

$$= 53.45 = 34.5 \text{ db}$$

$$1 + \frac{g_m}{g_{ds}} = 16 \Rightarrow \frac{g_m}{g_{ds}} = 106.9 \Rightarrow g_{ds} = 1.49 \mu$$

$$\text{So } BW = \frac{1}{2\pi \times C_L \times \frac{1}{2g_{ds}}} = 94.8 \text{ K}$$

$$GBW = A_{VD} \times BW = 5.07 \text{ M}$$

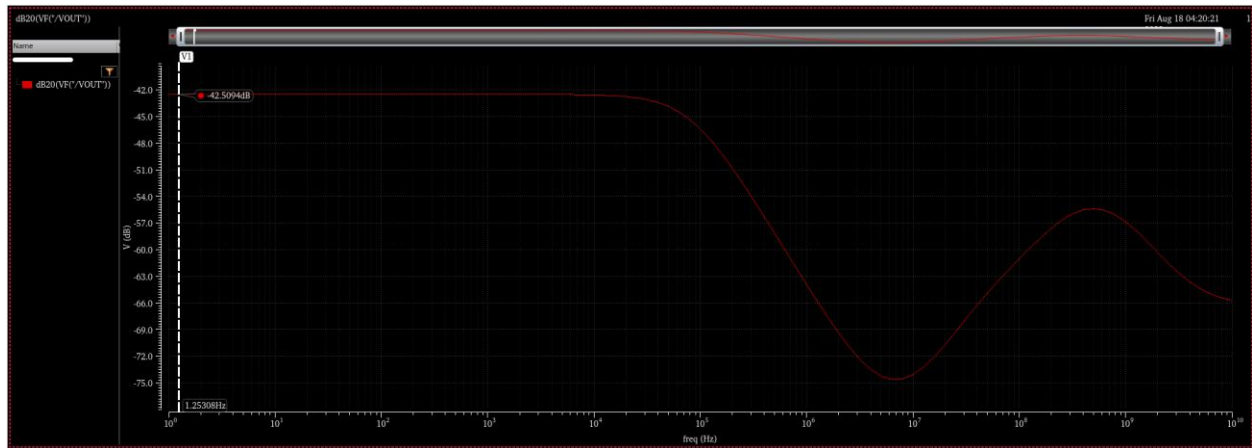
UGF

lab7_part234_1	AO	61.2			
lab7_part234_1	AO_DB	35.73			
lab7_part234_1	BW	83.35K			
lab7_part234_1	fu	5.12M			
lab7_part234_1	GBW	5.101M			
lab7_part234_1	dB20(VF("VOUT...				

	simulated	Analytical
A0	61.2	53.45
A0_DB	35.73 db	34.5 db
BW	83.35k	94.8k
GBW	5.12M	5.07M
Fu	51.01M	5.07M

### 3 CM SMALL SIGNAL CCS

#### 3.1 PLOT CM GAIN IN DB VS FREQUENCY.



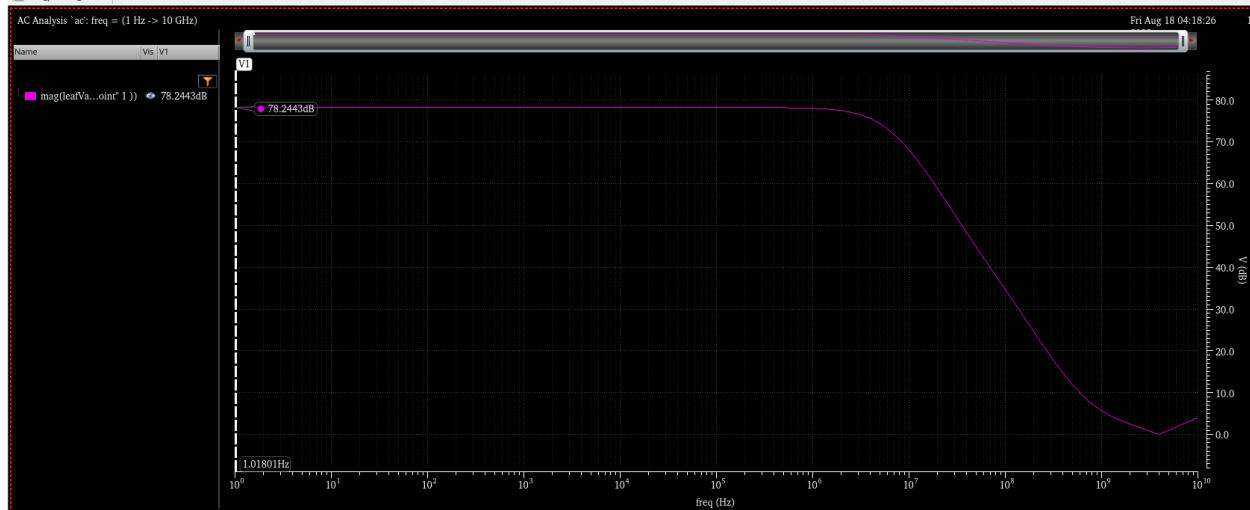
#### 3.2 COMPARE SIMULATION RESULTS WITH HAND CALCULATIONS IN A TABLE.

$$\begin{aligned}
 A_{VCM} &= \frac{1}{29\text{M} R_{SS}} = \frac{1}{2 \frac{9\text{M} \cdot 34}{9\text{ds}}} \\
 &= \frac{I_{DS\text{TAIL}}}{29\text{M}} = \frac{1,732}{2[300]} = 2,8\text{M} \\
 &= \boxed{-50,8 \text{ db}}
 \end{aligned}$$

	SIMULATOR	ANALYTICAL
AVCM	-42.8 db	-50.8 db

## 4 CMRR:

### 4.1 PLOT CMRR IN dB VS FREQUENCY AT VICM AT THE MIDDLE OF THE CMIR.



### 4.2 COMPARE SIMULATION RESULTS WITH HAND CALCULATIONS IN A TABLE.

$$CMRR = 34,5 - [-50,8] = (85,3 \text{ dB})$$

	SIMULATOR	ANALYTICAL
CMRR	78.24 db	85.3 db

## 5 DIFF LARGE SIGNAL CCS:

5.1 USE DC SWEEP (NOT PARAMETRIC SWEEP)  $V_{ID} = -V_{DD}:1m:V_{DD}$ . YOU MUST USE A SMALL STEP (1mV) BECAUSE THE GAIN REGION IS VERY SMALL (STEEP SLOPE).

**Choosing Analyses -- ADE Assembler** x

Analysis

☐ tran ☒ dc ☐ ac ☐ noise

☐ xf ☐ sens ☐ dcmatch ☐ acmatch

☐ stb ☐ pz ☐ lf ☐ sp

☐ envlp ☐ pss ☐ pac ☐ pstb

☐ pnoise ☐ pxf ☐ psp ☐ qpss

☐ qpac ☐ qpnoise ☐ qpxf ☐ qpssp

☐ hb ☐ hbac ☐ hbstb ☐ hbnoise

☐ hbsp ☐ hbxf

DC Analysis

Save DC Operating Point ☐

Hysteresis Sweep ☐

Sweep Variable

☐ Temperature

☒ Design Variable Variable Name

☐ Component Parameter

☐ Model Parameter

Sweep Range

☒ Start-Stop Start  Stop

☐ Center-Span

Sweep Type

☒ Step Size

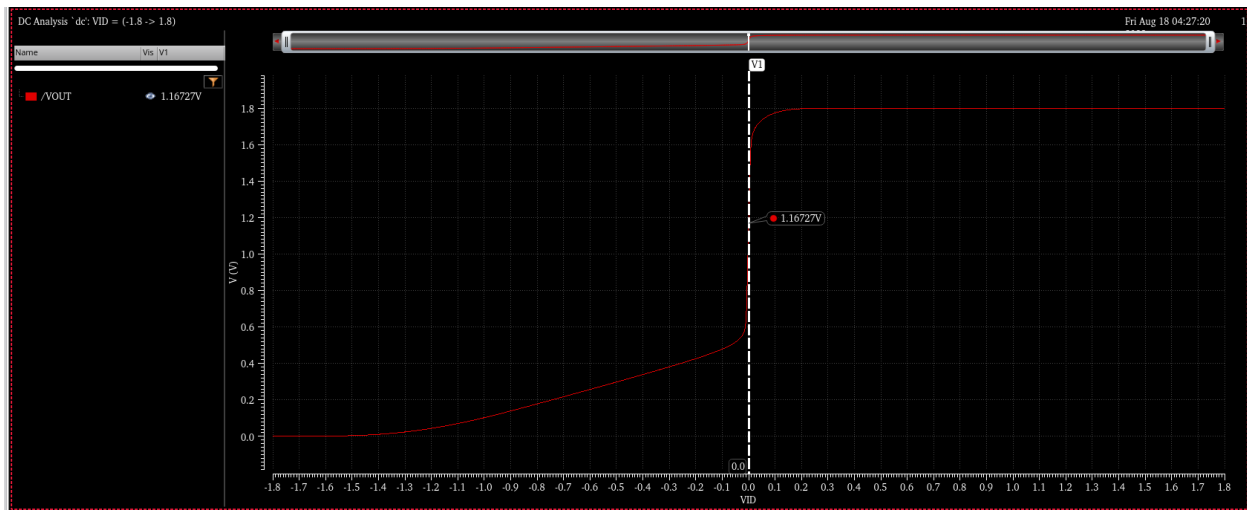
☐ Number of Steps

Add Specific Points ☐

Add Points By File ☐

Enabled ☒

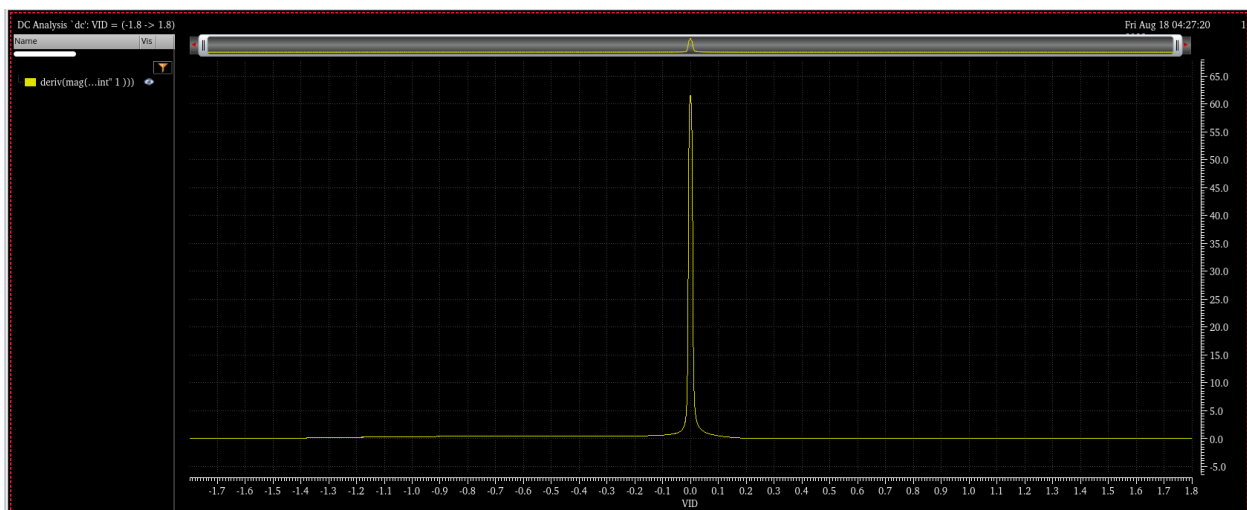
## 5.2 Plot $V_{OUT}$ vs $V_{ID}$ .



## 5.3 FROM THE PLOT, WHAT IS THE VALUE OF $V_{OUT}$ AT $V_{ID} = 0$ ? WHY?

1.167, Which is the dc operating point (vicm) as  $V_{ID}=0$ , the current is equal in the two halves at this point so  $V_{out}$  follow  $V_f$ .

## 5.4 PLOT THE DERIVATIVE OF $V_{OUT}$ vs $V_{ID}$ . COMPARE THE PEAK WSOITH $A_{VD}$ .



Expression	Value
1 ymax(deriv(mag(...in* 1)))	61.55

Here is the peak is 61.55, but  $A_{vd}=61.2$

## 6 CM LARGE SIGNAL CCS (REGION VS VICM):

### 6.1 USE DC SWEEP (NOT PARAMETRIC SWEEP) VICM = 0:10m:VDD.

**Choosing Analyses -- ADE Assembler** ×

Analysis

<input type="radio"/> tran	<input checked="" type="radio"/> dc	<input type="radio"/> ac	<input type="radio"/> noise
<input type="radio"/> xf	<input type="radio"/> sens	<input type="radio"/> dcmatch	<input type="radio"/> acmatch
<input type="radio"/> stb	<input type="radio"/> pz	<input type="radio"/> lf	<input type="radio"/> sp
<input type="radio"/> envlp	<input type="radio"/> pss	<input type="radio"/> pac	<input type="radio"/> pstb
<input type="radio"/> pnoise	<input type="radio"/> pxf	<input type="radio"/> psp	<input type="radio"/> qpss
<input type="radio"/> qpac	<input type="radio"/> qpnoise	<input type="radio"/> qpxf	<input type="radio"/> qpssp
<input type="radio"/> hb	<input type="radio"/> hbac	<input type="radio"/> hbstb	<input type="radio"/> hbnoise
<input type="radio"/> hbsp	<input type="radio"/> hbxf		

DC Analysis

Save DC Operating Point ☐

Hysteresis Sweep ☐

Sweep Variable

☐ Temperature

☒ Design Variable

☐ Component Parameter

☐ Model Parameter

Variable Name

Select Design Variable

Sweep Range

☒ Start-Stop

Start  Stop

☐ Center-Span

Sweep Type

Linear

☒ Step Size

☐ Number of Steps

Add Specific Points ☐

Add Points By File ☐

Enabled ☒

Options...

**OK** Cancel Defaults Apply Help



## 6.2 PLOT “REGION” OP PARAMETER VS VICM FOR THE INPUT PAIR AND THE TAIL CURRENT SOURCE.



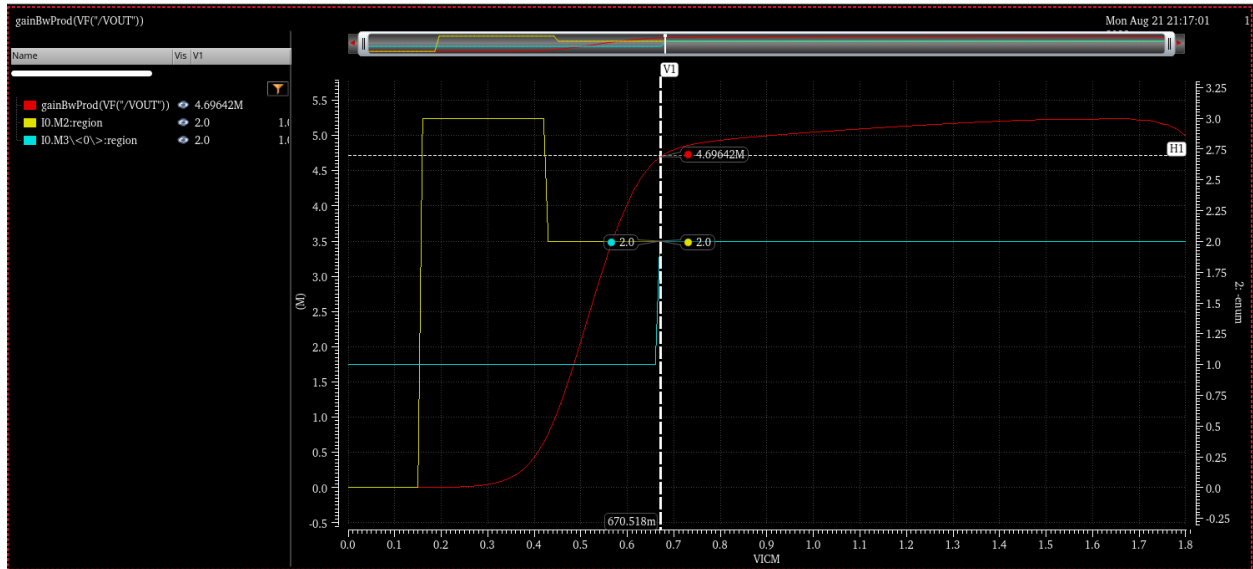
## 6.3 FIND THE CM INPUT RANGE (CMIR). COMPARE WITH HAND ANALYSIS IN A TABLE.

$$1.8 - 670.79\text{m} = 1.13\text{ V}$$

$$\text{HAND ANALYSIS: } 1.5 - 0.8 = 0.7\text{ V}$$

	sim	Hand analysis
CMIR	1.13	0.7

6.4 PLOT “REGION” OP PARAMETER VS VICM FOR THE INPUT PAIR AND THE TAIL CURRENT SOURCE (0 CUT-OFF, 1 TRIODE, 2 SAT, 3 SUBTH, AND 4 BREAKDOWN). PLOT THE RESULTS OVERLAID ON THE RESULTS OF THE PREVIOUS METHOD (10% REDUCTION OF GBW).



## 7 (OPTIONAL) CM LARGE SIGNAL CCS (GBW vs VICM)

### 7.1

**Choosing Analyses -- ADE Assembler** x

Analysis

<input type="radio"/> tran	<input type="radio"/> dc	<input checked="" type="radio"/> ac	<input type="radio"/> noise
<input type="radio"/> xf	<input type="radio"/> sens	<input type="radio"/> dcmatch	<input type="radio"/> acmatch
<input type="radio"/> stb	<input type="radio"/> pz	<input type="radio"/> lf	<input type="radio"/> sp
<input type="radio"/> envlp	<input type="radio"/> pss	<input type="radio"/> pac	<input type="radio"/> pstb
<input type="radio"/> pnoise	<input type="radio"/> pxf	<input type="radio"/> psp	<input type="radio"/> qpss
<input type="radio"/> qpac	<input type="radio"/> qpnoise	<input type="radio"/> qpxf	<input type="radio"/> qpssp
<input type="radio"/> hb	<input type="radio"/> hbac	<input type="radio"/> hbstb	<input type="radio"/> hbnoise
<input type="radio"/> hbsp	<input type="radio"/> hbxf		

AC Analysis

Sweep Variable

☐ Frequency

☒ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

At Frequency (Hz)

Variable Name

Select Design Variable

Sweep Range

☒ Start-Stop

☐ Center-Span

Start  Stop

Sweep Type

Linear

☒ Step Size

☐ Number of Steps

Step Size

Add Specific Points ☐

Add Points By File ☐

Specialized Analyses

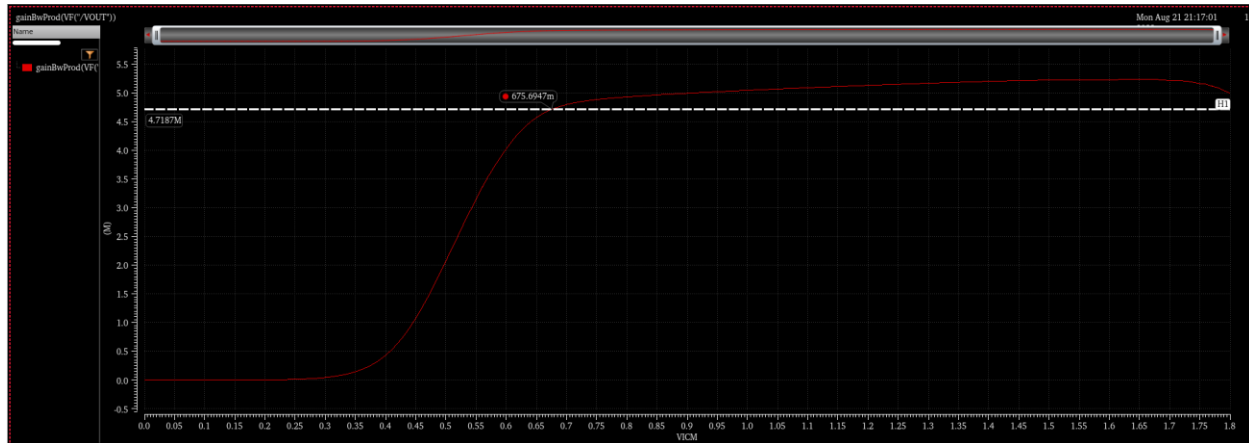
None

Enabled ☒

Options...

OK Cancel Defaults Apply Help

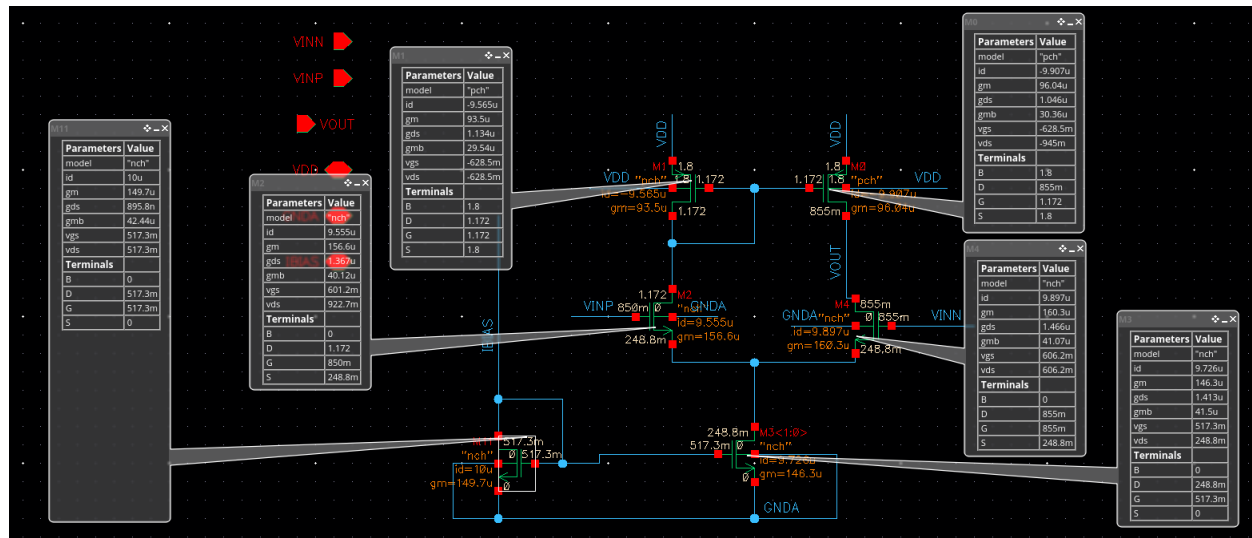
7.2 ANNOTATE THE CM INPUT RANGE. CALCULATE THE INPUT RANGE AS THE RANGE OVER WHICH THE GBW IS WITHIN 90% OF THE MAX GBW, I.E., 10% REDUCTION IN GBW2 .



The input range=  $1.8 - 0.676 = 1.124$  V

## Part4:

### 1 SCHEMATIC OF THE OTA WITH DC OP POINT CLEARLY ANNOTATED IN UNITY GAIN BUFFER CONFIGURATION. USE VIN = CMIR-LOW + 50MV.



#### 1.1 IS THE CURRENT (AND GM) IN THE INPUT PAIR EXACTLY EQUAL ? WHY?

NO, because of the feedback make The output voltage deviates from its CM level  
Since the gain is finite (Verror=5mv)

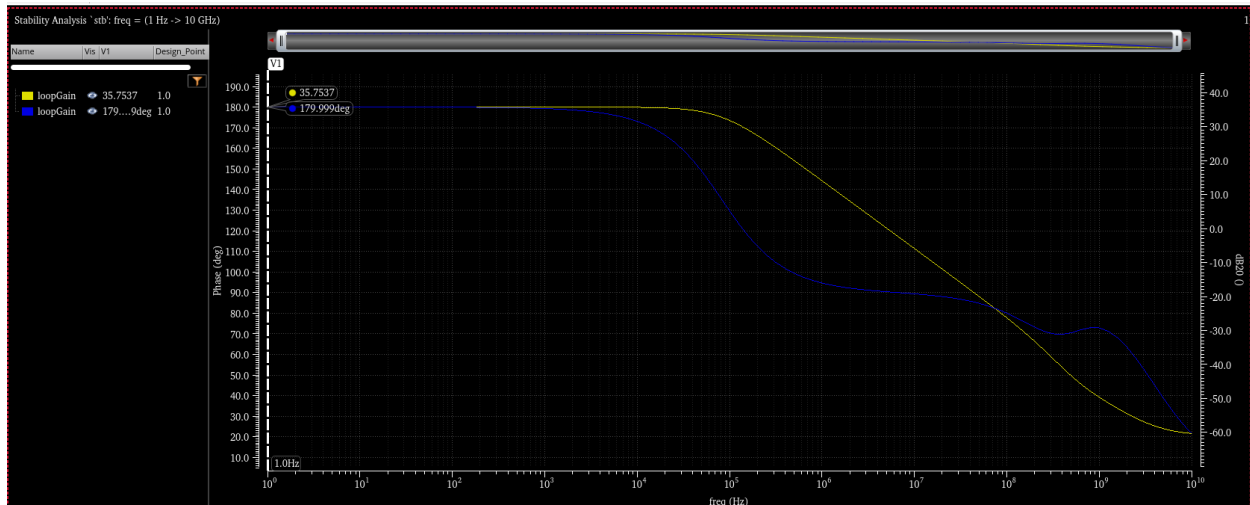
#### 1.2 CALCULATE THE MISMATCH IN $ID$ AND $GM$ .

$$ID = \frac{9.897 - 9.555}{9.555} = 0.0357 = 3.57\%$$

$$gm = \frac{160.3 - 156.6}{156.6} = 0.023 = 2.36\%$$

## 2 LOOP GAIN:

### 2.1 PLOT LOOP GAIN IN dB AND PHASE VS FREQUENCY



### 2.2 COMPARE DC GAIN AND GBW WITH THOSE OBTAINED FROM OPEN-LOOP SIMULATION.

COMMENT

	OPEN-LOOP	LOOP GAIN
DC GAIN	35.73 db	35.75 DB
GBW	5.12M	5.10 M

The dc gain of loop gain is higher than open loop because of mismatch happend, but BW in open-loop is higher so GBW in open-loop is higher than loop gain case but they are approximately equal.

### 2.3 COMPARE SIMULATION RESULTS WITH HAND CALCULATIONS IN A TABLE

	ANALYTICAL	SIMULATION
DC GAIN	$\beta A_{ol}$ and $\beta = 1$ =34.5 db (the value we ANALYTICALLY calculated above)	35.75 DB
GBW	5.07 M $\beta = 1$ same as Open loop we calculated above	5.10 M