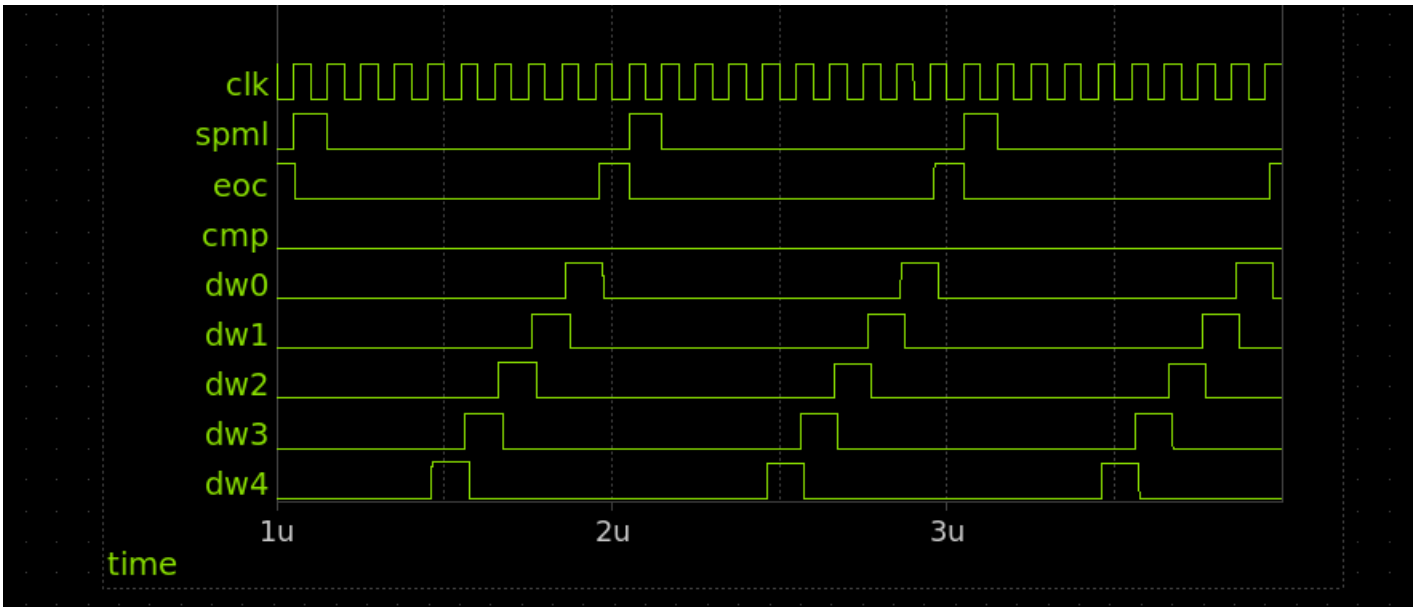
Lab 04 (Mini-Project 01)

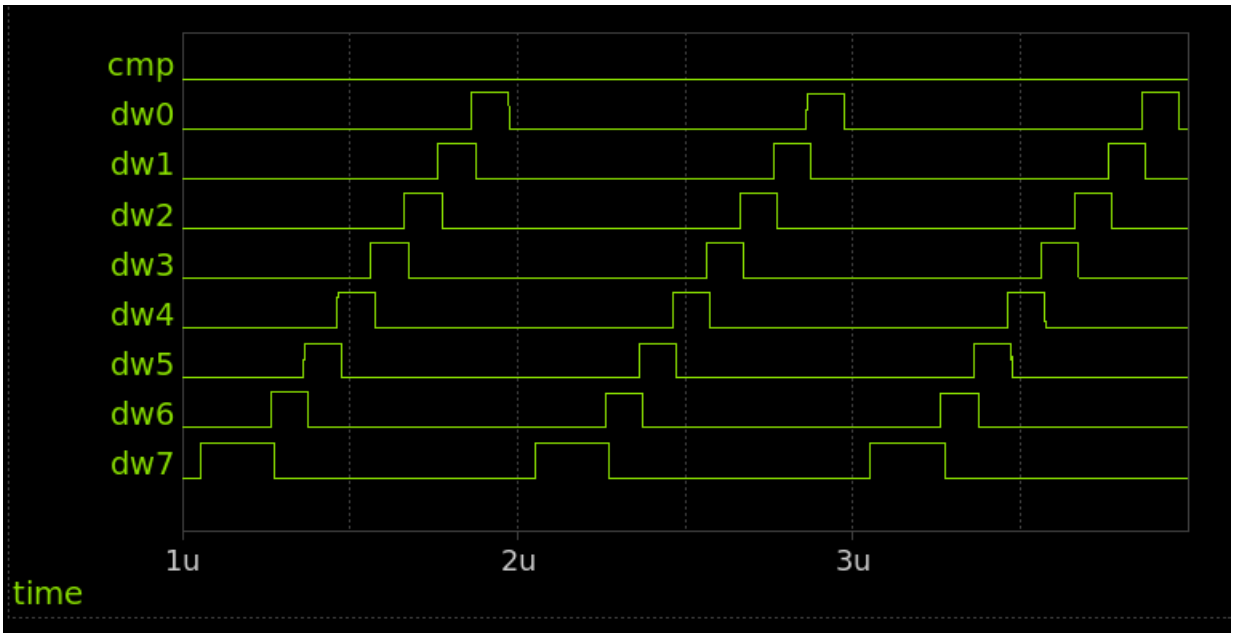
SAR ADC

Part1: SAR Logic

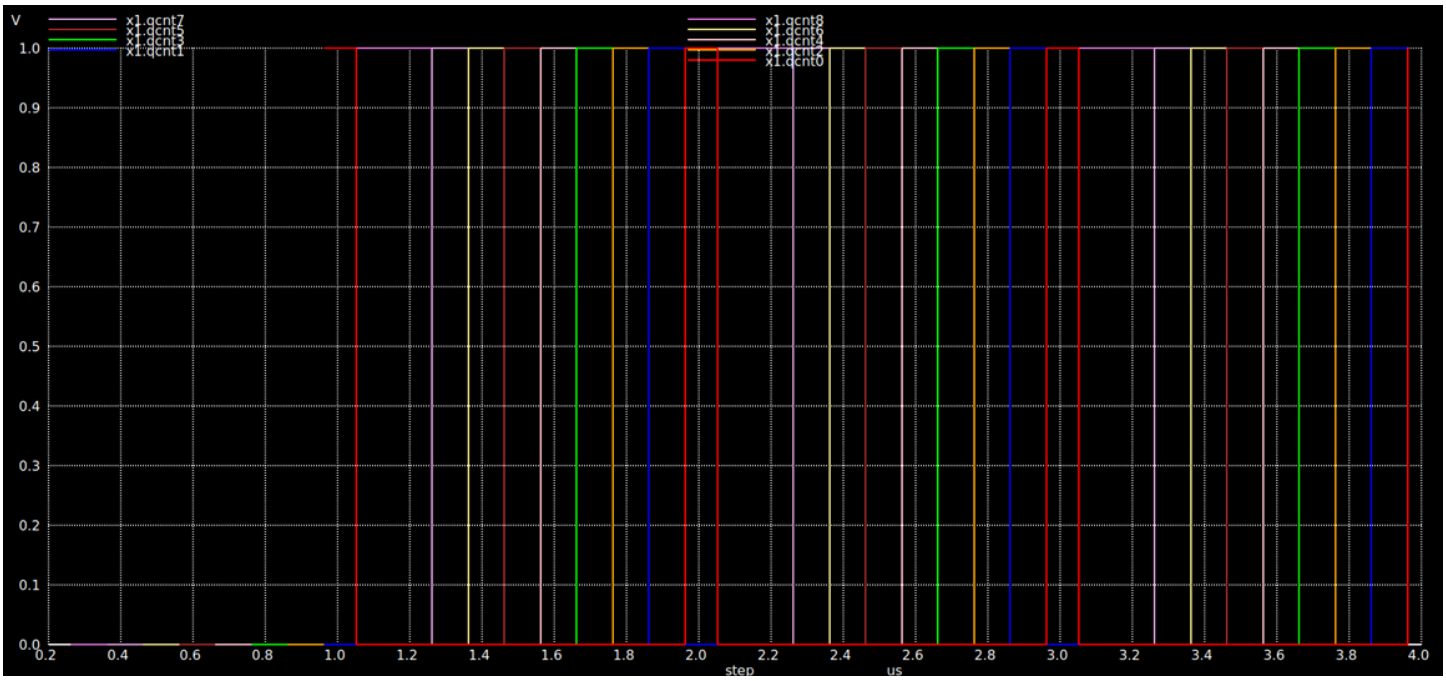
1 Report transient simulation results for the ring counter output, the code register output, and the EOC signal for the following cases:

1.1 CMP is all zeros

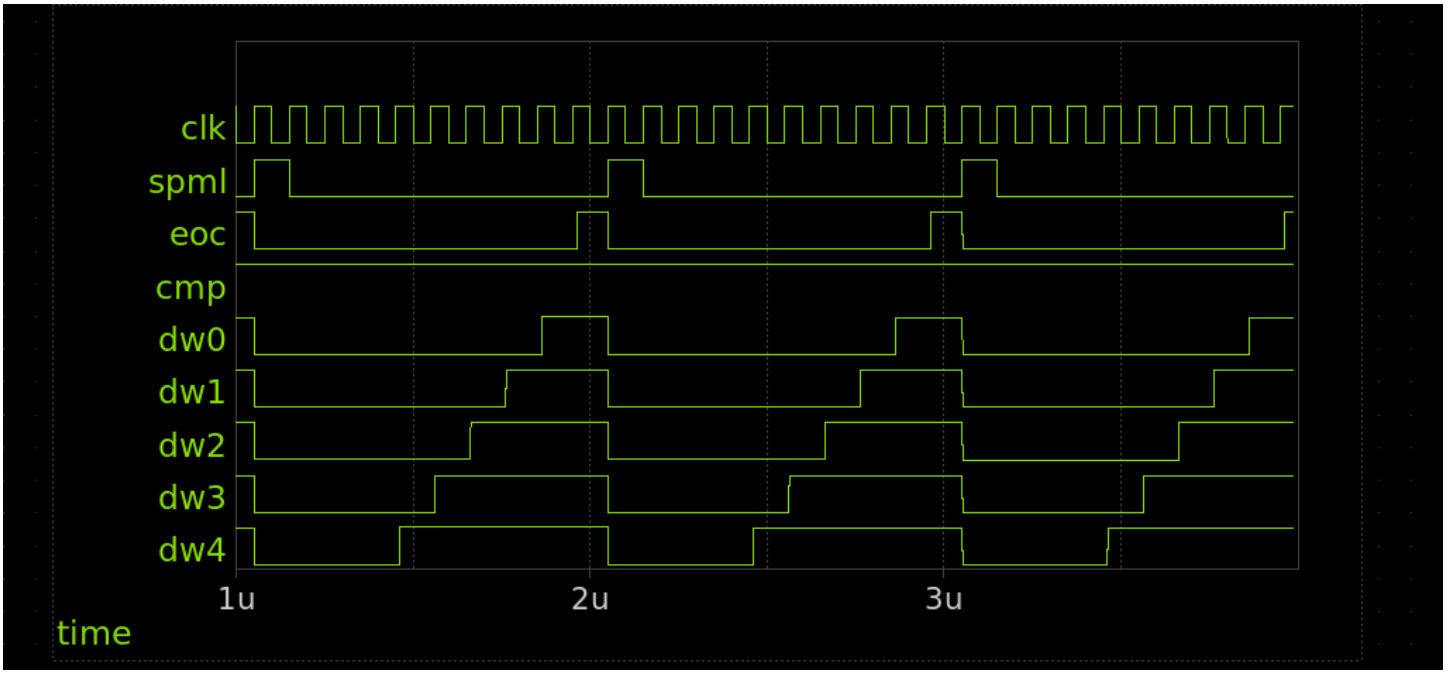


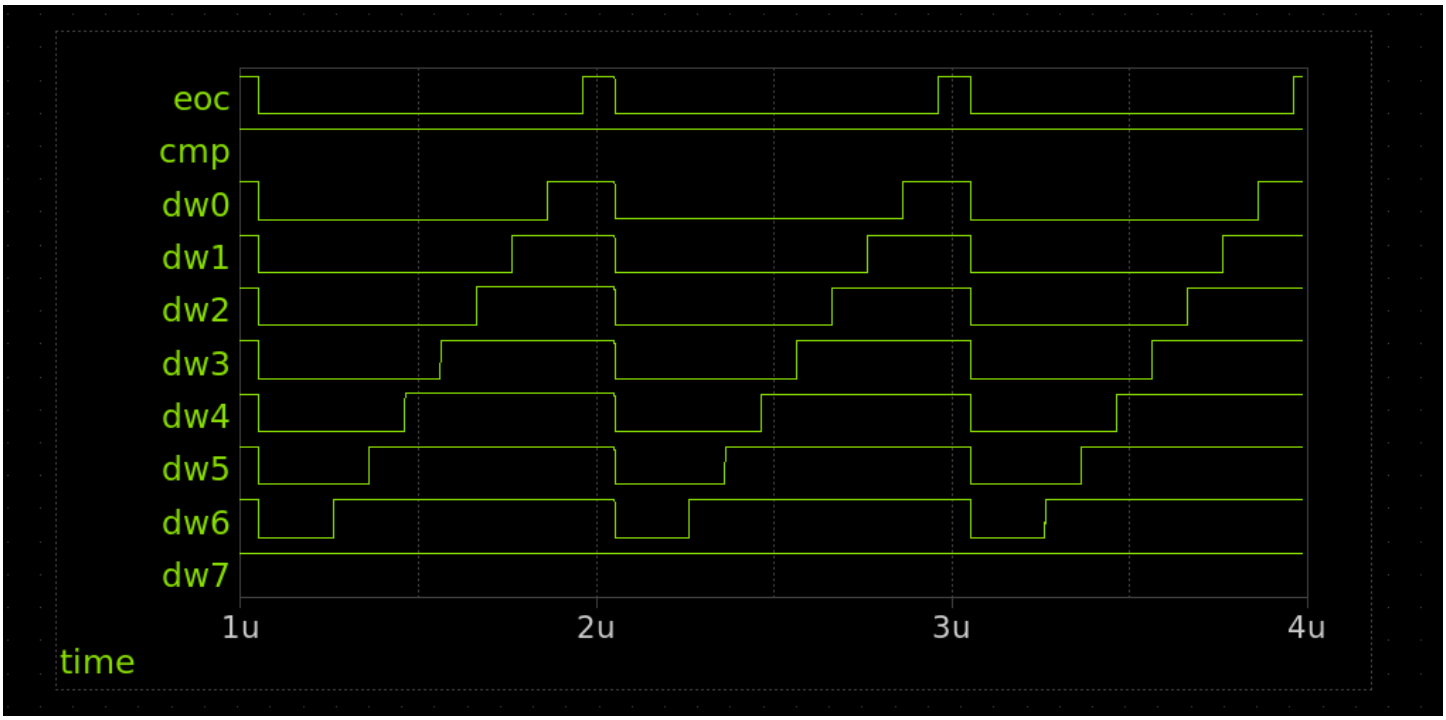


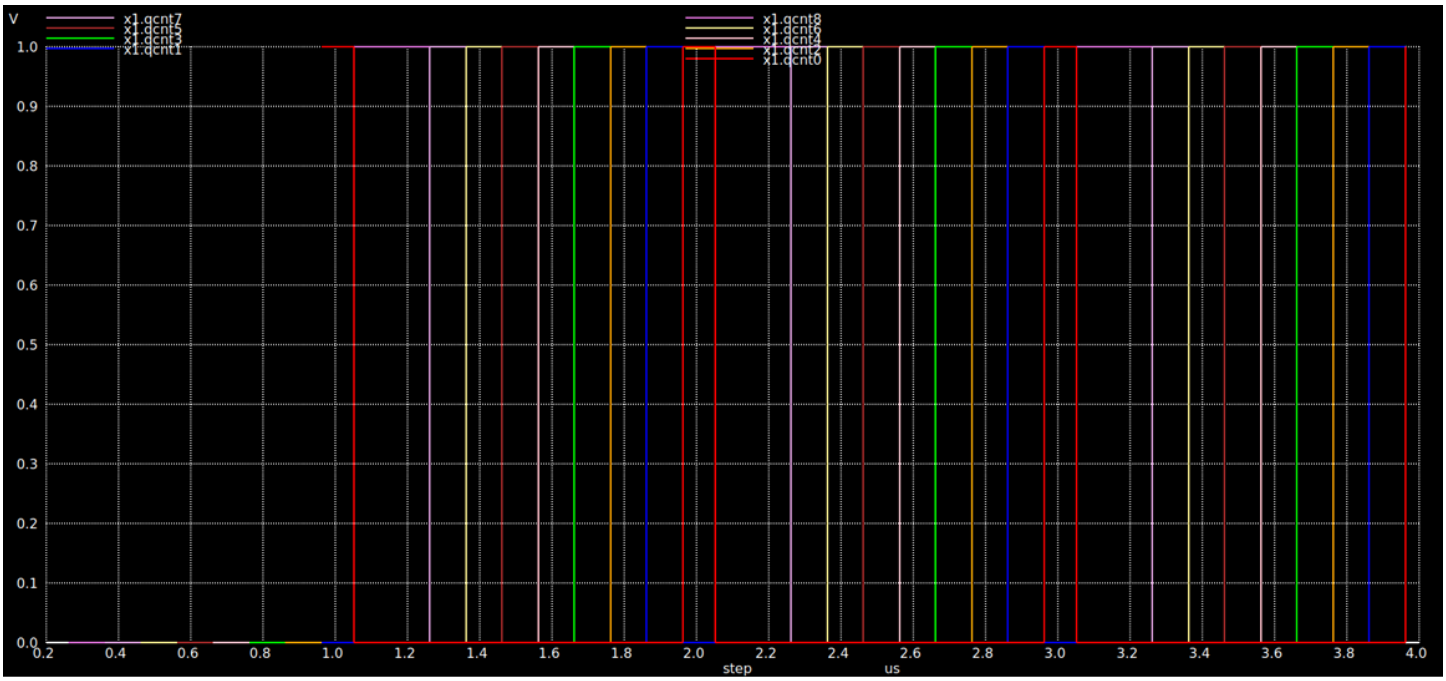
Counter output:



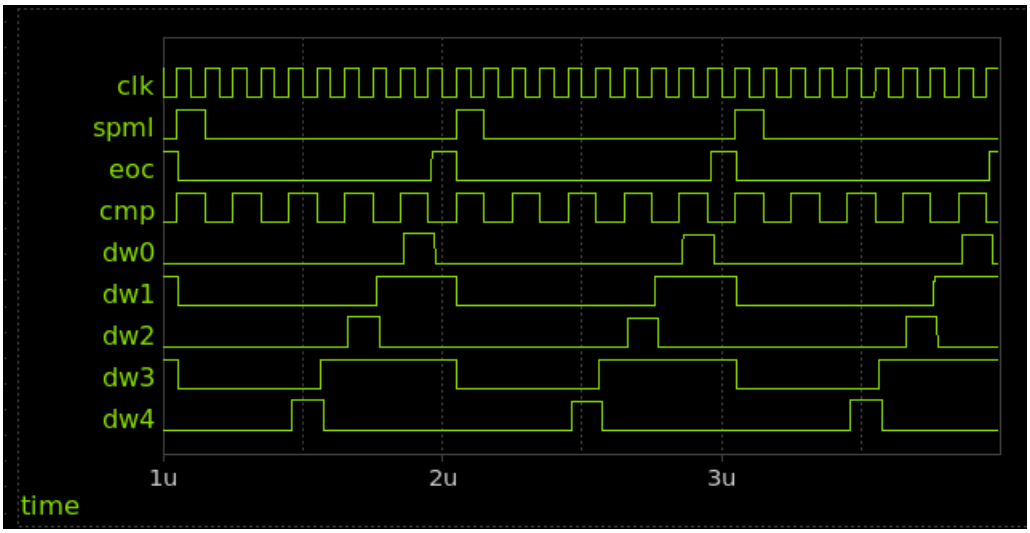
1.2 CMP IS ALL ONES

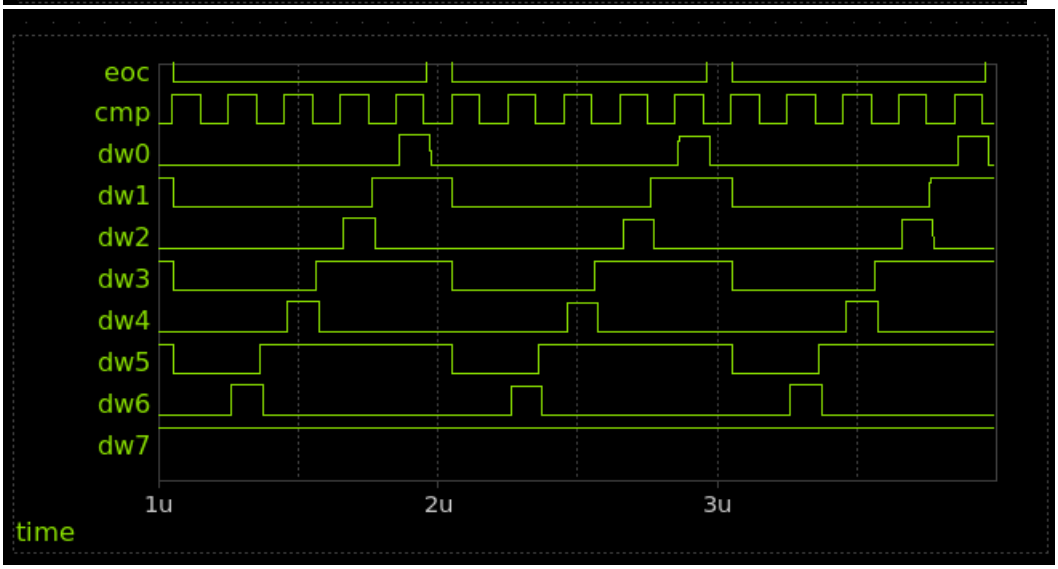



eoc
cmp
dw0
dw1
dw2
dw3
dw4
dw5
dw6
dw7
1u
2u
3u
4u
time

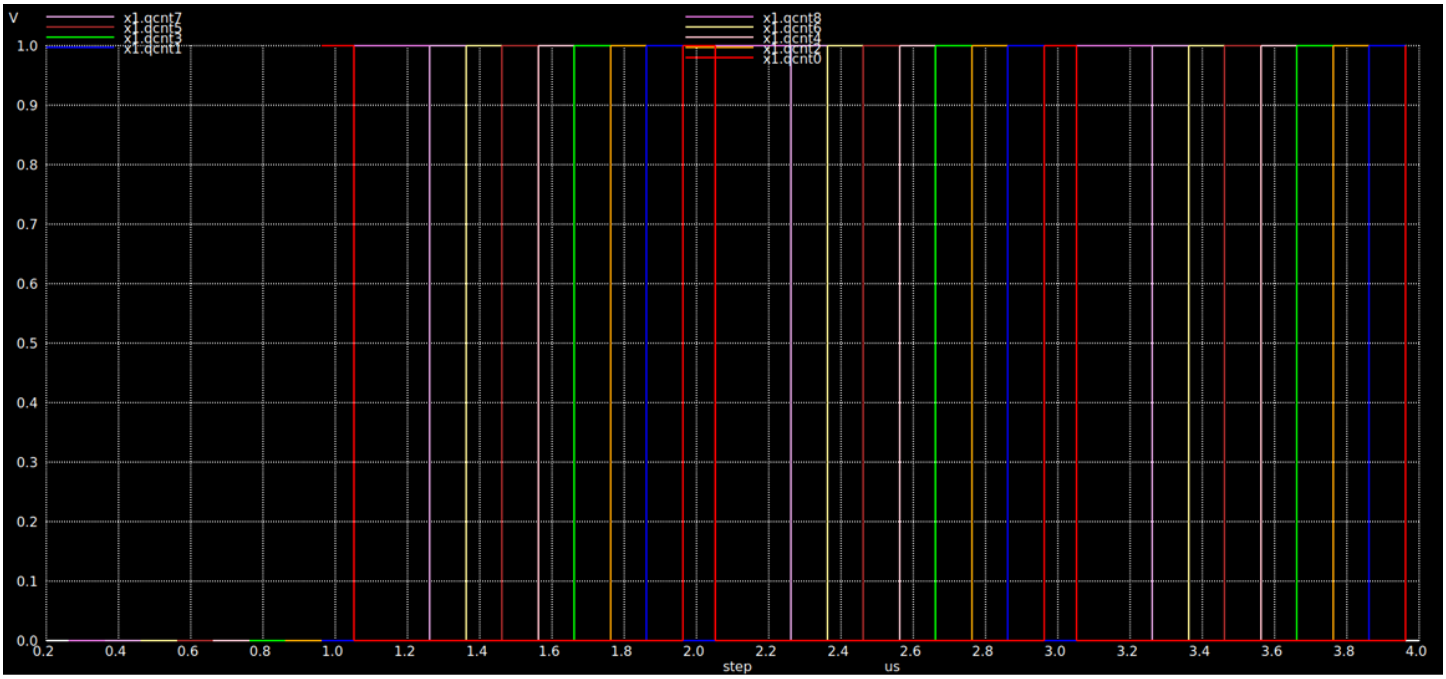

V
x1.qcnt7
x1.qcnt5
x1.qcnt3
x1.qcnt1
x1.qcnt8
x1.qcnt6
x1.qcnt4
x1.qcnt2
x1.qcnt0
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
3.2
3.4
3.6
3.8
4.0
step
us

1.3 CMP IS ALTERNATING ONES AND ZEROS (PERIOD = 2*TCLK AND PULSE WIDTH = TCLK)





Eoc should be low to look at clk cycles, with every new cycle a new bit will be set to 1 then look at the comparator output value within this cycle and keep it in the next cycles till the final cycle.



2 BRIEFLY EXPLAIN IN YOUR OWN WORDS HOW DOES THIS DESIGN WORK AND HOW DOES IT IMPLEMENT THE SUCCESSIVE APPROXIMATION ALGORITHM. SUPPORT YOUR EXPLANATION BY FILLING THE STATE TABLE BELOW.

Based on the results of the comparator, the circuit sets the value of bits sequentially, if we have N bits the first cycle is resetting so all the bits must have 0 value, then with every cycle sequentially the bit would be high then with the next cycle it would capture the comparator output signal and keep it till final bit.

cycle	Dw<7>	Dw<6>	Dw<5>	Dw<4>	Dw<3>	Dw<2>	Dw<1>	Dw<0>	cmp
1(reset)	1	0	0	0	0	0	0	0	
2	1	0	0	0	0	0	0	0	B7
3	B7	1	0	0	0	0	0	0	B6
4	B7	B6	1	0	0	0	0	0	B5
5	B7	B6	B5	1	0	0	0	0	B4
6	B7	B6	B5	B4	1	0	0	0	B3
7	B7	B6	B5	B4	B3	1	0	0	B2
8	B7	B6	B5	B4	B3	B2	1	0	B1
9	B7	B6	B5	B4	B3	B2	B1	1	B0
10	B7	B6	B5	B4	B3	B2	B1	B0	

2.1 CASE 1: CMP IS ALL ZEROS

cycle	Dw<7>	Dw<6>	Dw<5>	Dw<4>	Dw<3>	Dw<2>	Dw<1>	Dw<0>	cmp
1(reset)	1	0	0	0	0	0	0	0	
2	1	0	0	0	0	0	0	0	0
3	0	1	0	0	0	0	0	0	0
4	0	0	1	0	0	0	0	0	0
5	0	0	0	1	0	0	0	0	0
6	0	0	0	0	1	0	0	0	0
7	0	0	0	0	0	1	0	0	0
8	0	0	0	0	0	0	1	0	0
9	0	0	0	0	0	0	0	1	0
10	0	0	0	0	0	0	0	0	

2.1 CASE 2: CMP IS ALL ONES

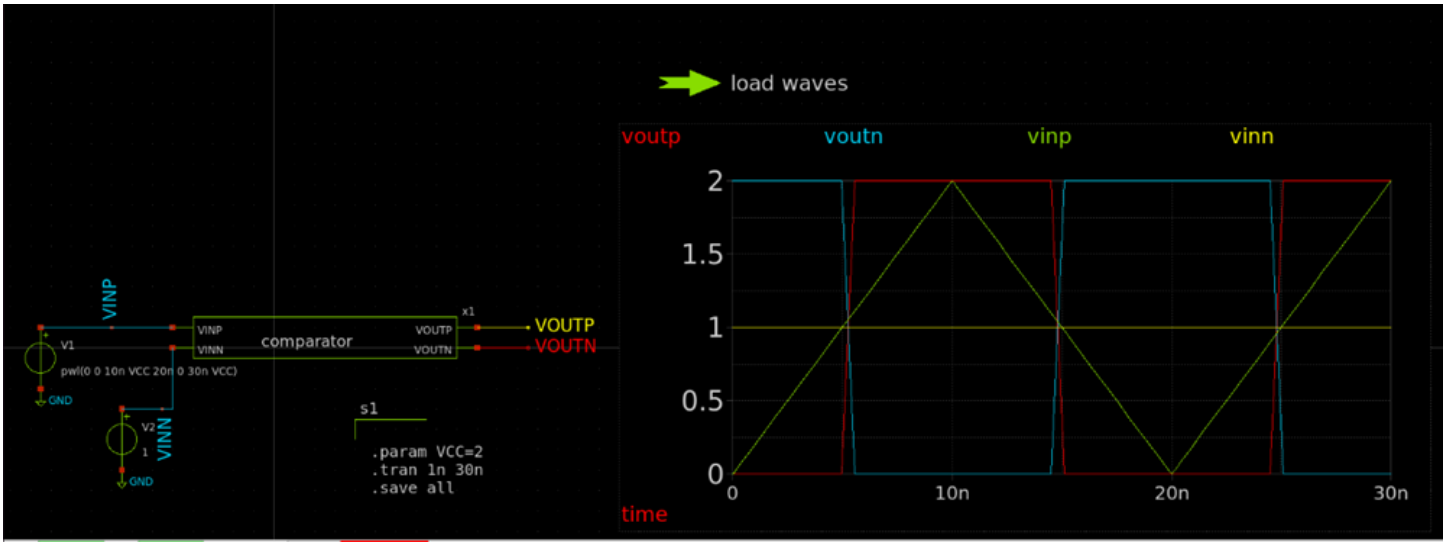
cycle	Dw<7>	Dw<6>	Dw<5>	Dw<4>	Dw<3>	Dw<2>	Dw<1>	Dw<0>	cmp
1(reset)	1	0	0	0	0	0	0	0	
2	1	0	0	0	0	0	0	0	1
3	1	1	0	0	0	0	0	0	1
4	1	1	1	0	0	0	0	0	1
5	1	1	1	1	0	0	0	0	1
6	1	1	1	1	1	0	0	0	1
7	1	1	1	1	1	1	0	0	1
8	1	1	1	1	1	1	1	0	1
9	1	1	1	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1	

2.2 CASE 3:CMP IS ALTERNATING ONES AND ZEROS

cycle	Dw<7>	Dw<6>	Dw<5>	Dw<4>	Dw<3>	Dw<2>	Dw<1>	Dw<0>	cmp
1(reset)	1	0	0	0	0	0	0	0	
2	1	0	0	0	0	0	0	0	1
3	1	1	0	0	0	0	0	0	0
4	1	0	1	0	0	0	0	0	1

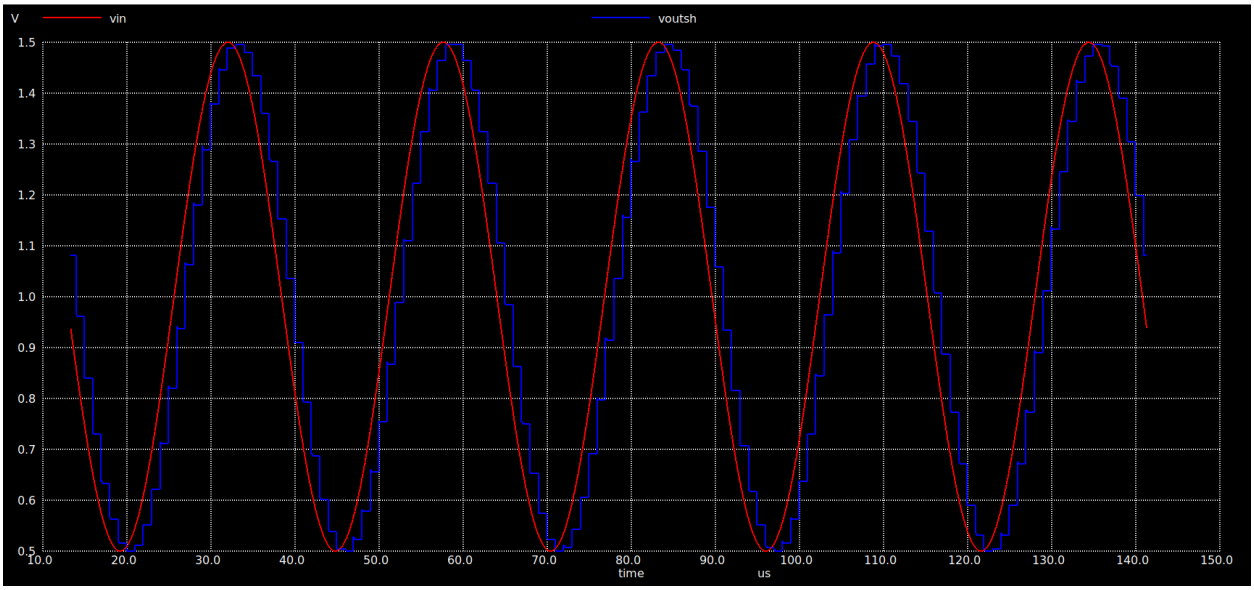
5	1	0	1	1	0	0	0	0	0
6	1	0	1	0	1	0	0	0	1
7	1	0	1	0	1	1	0	0	0
8	1	0	1	0	1	0	1	0	1
9	1	0	1	0	1	0	1	1	0
10	1	0	1	0	1	0	1	0	

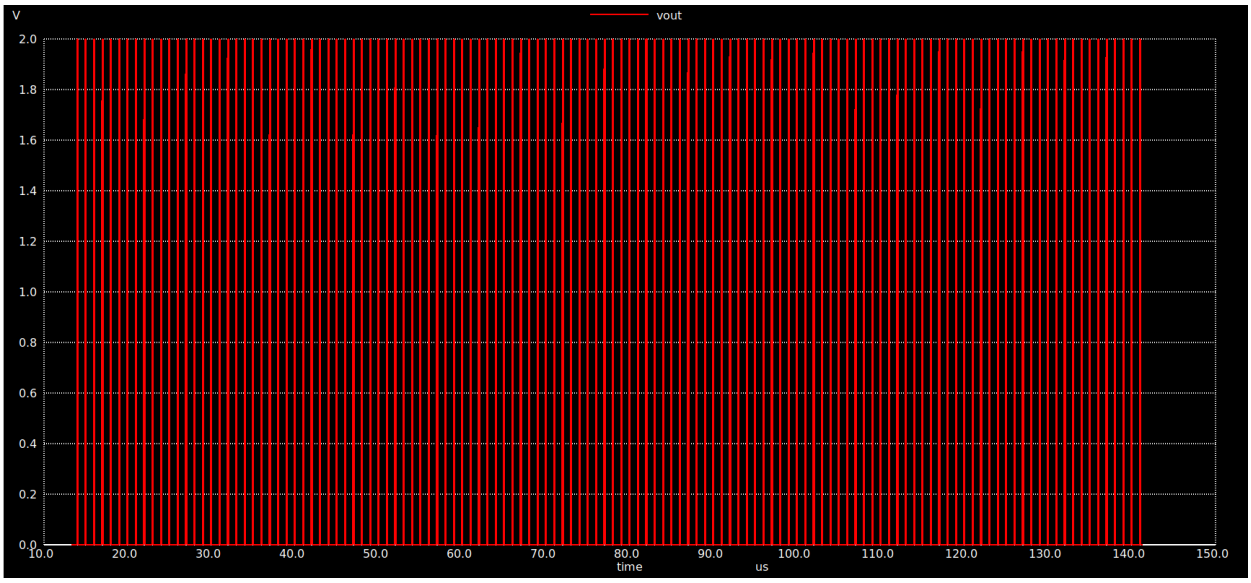
3 COMPARATOR:

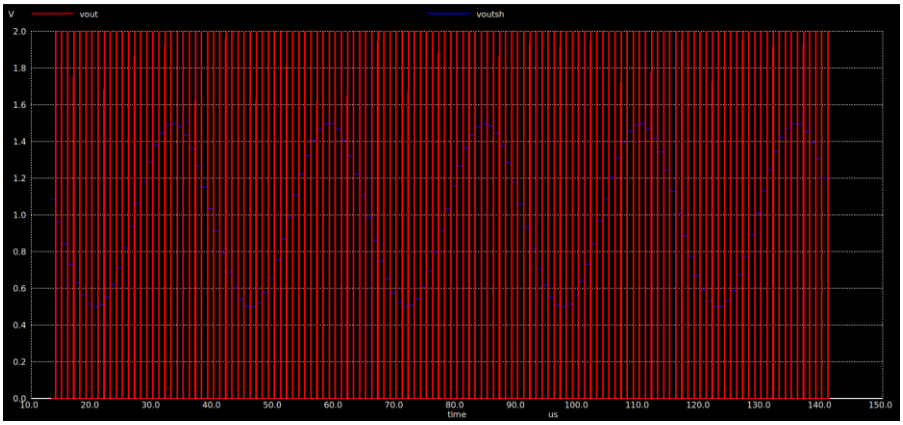


Part2: SAR ADC Testbench

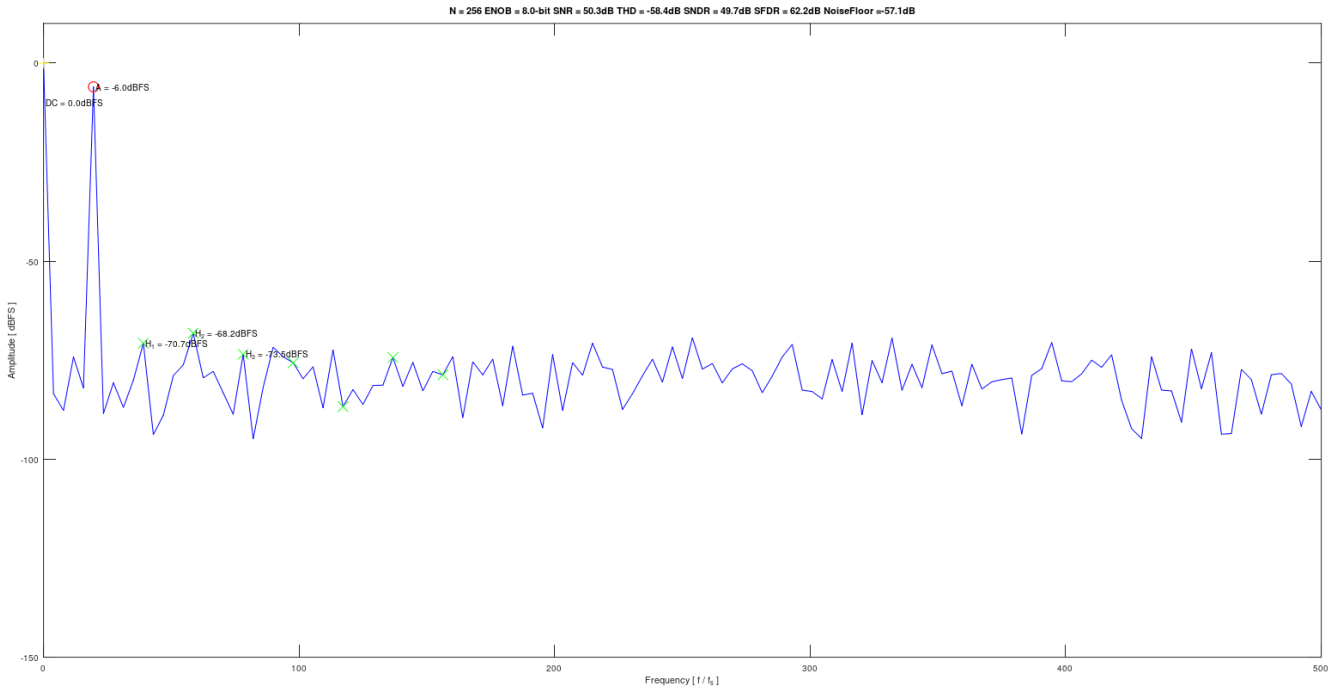
1 Report the waveforms of VOUTSH and VOUT for Sine Wave test







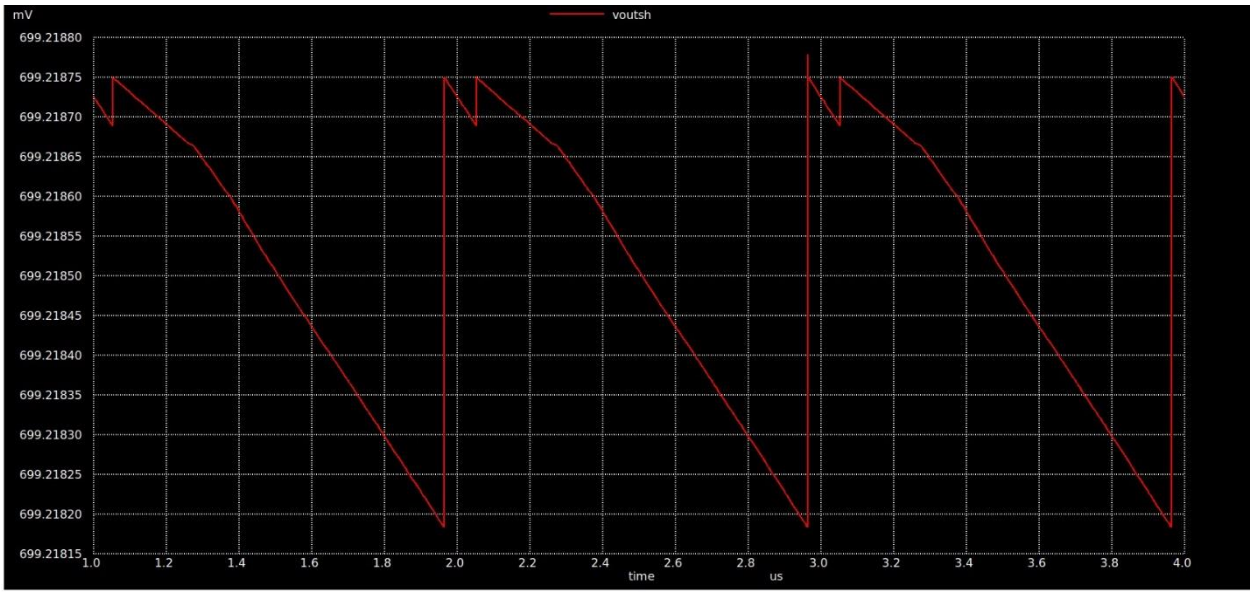
1.1 PLOT THE FFT OF THE VOUT TO MEASURE THE ENOB AND OTHER PERFORMANCE PARAMETERS:

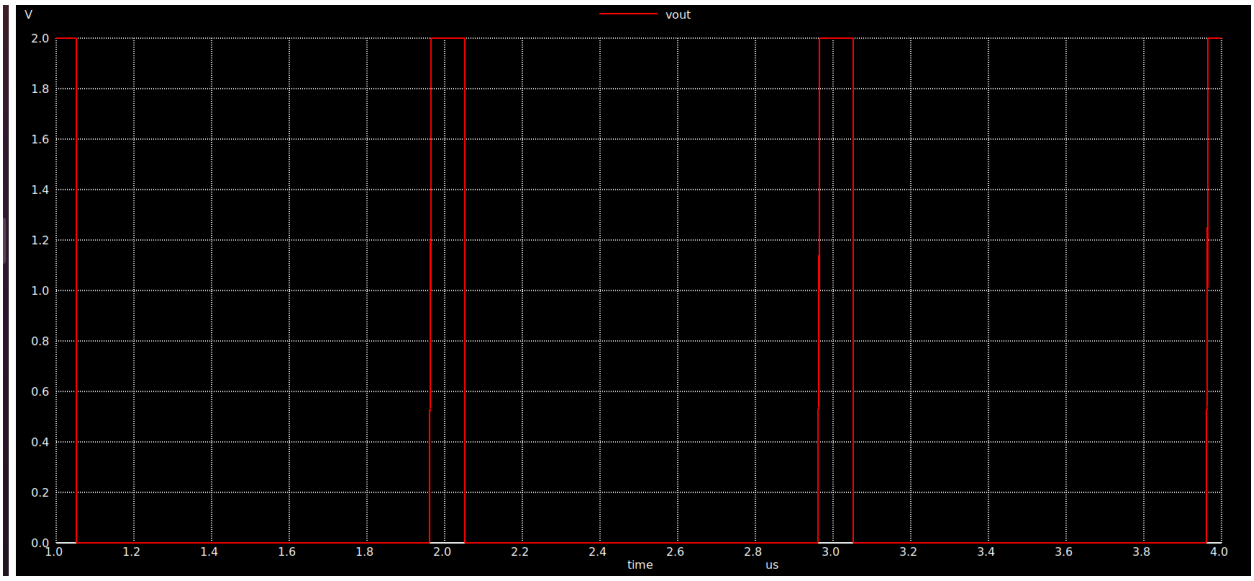


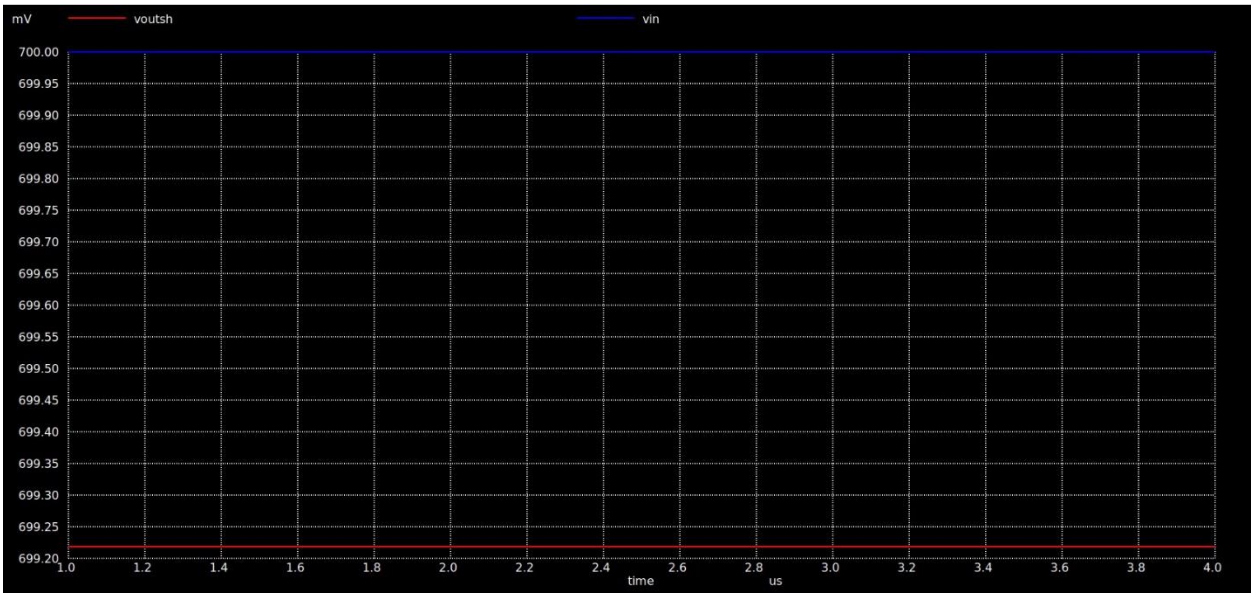
ENOB	8-bit
SNR	50.3db
THD	-58.4db
SNDR	49.7db
SFDR	62.2db
Noise Floor	-57.1db

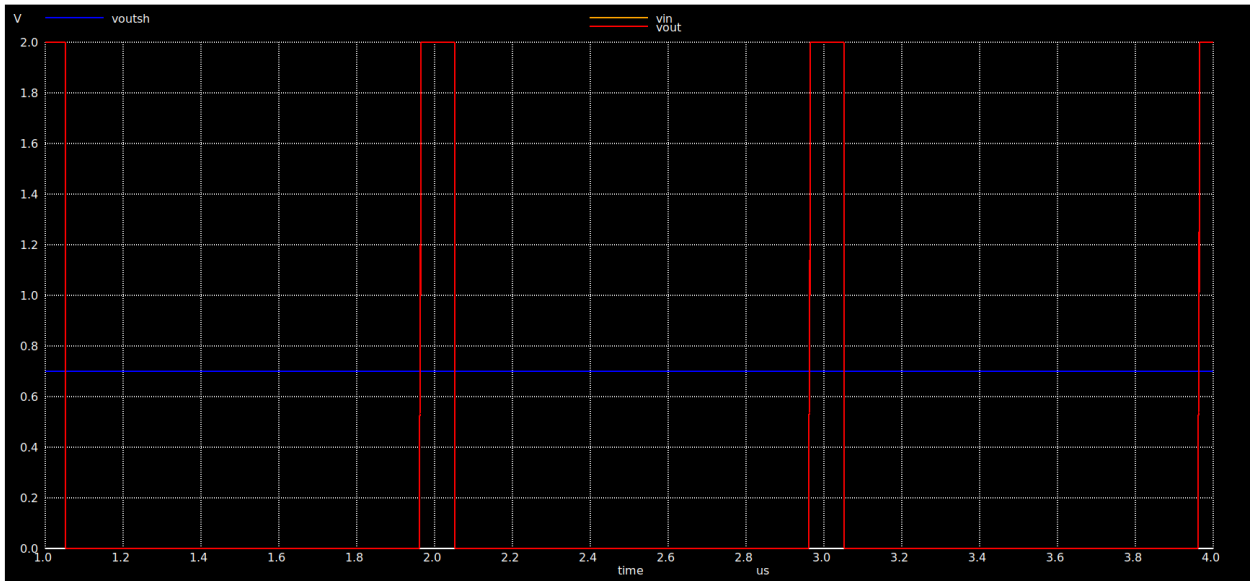
2 REPORT THE WAVEFORMS OF VOUTSH AND VOUT FOR DC_SIMULATION.

0.7v:



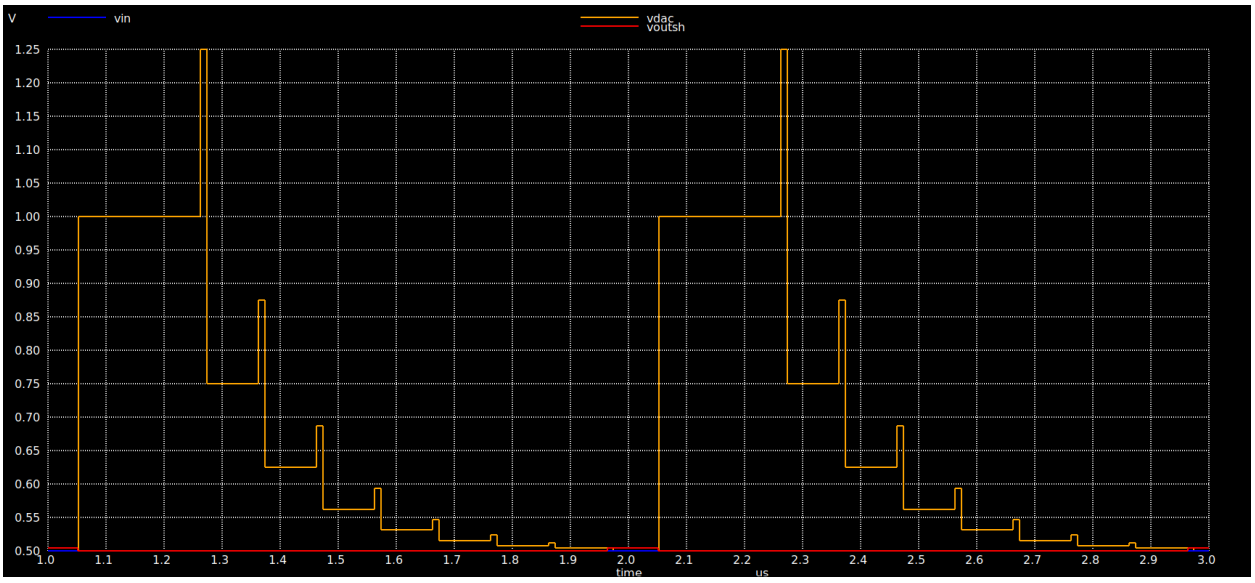




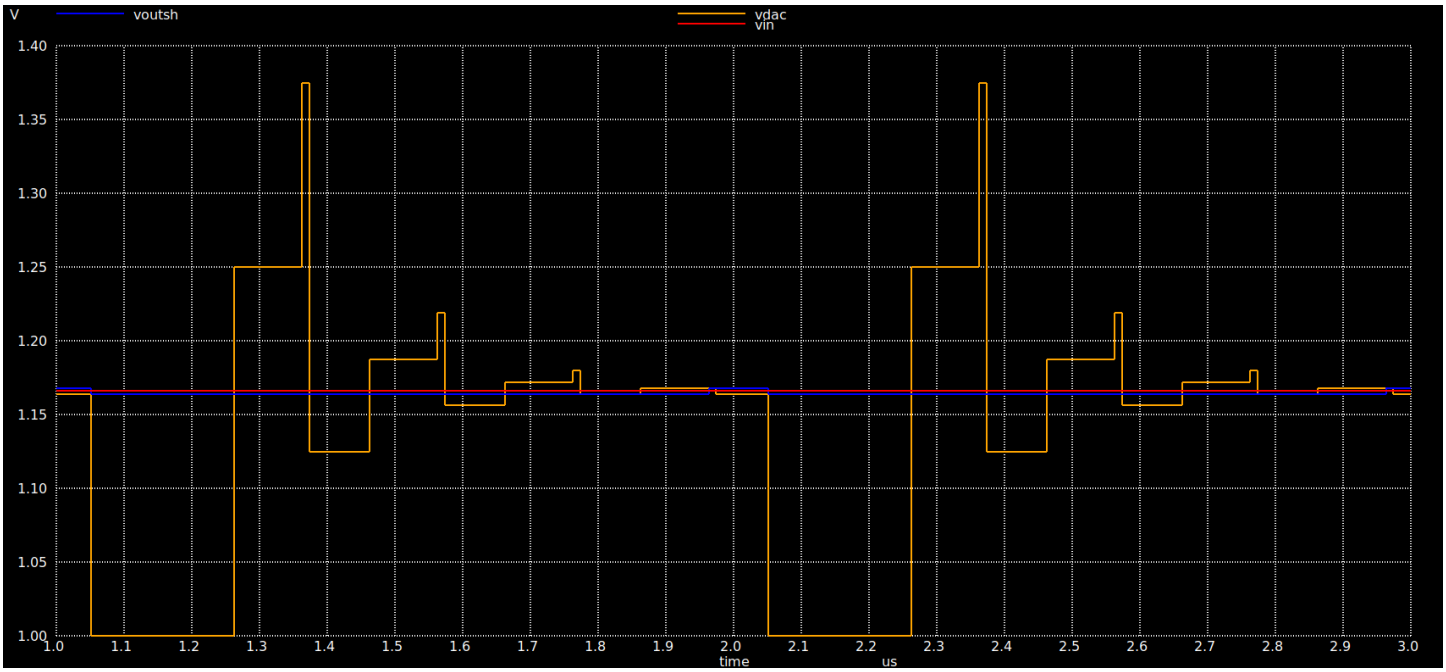


Tstop=3Ts:

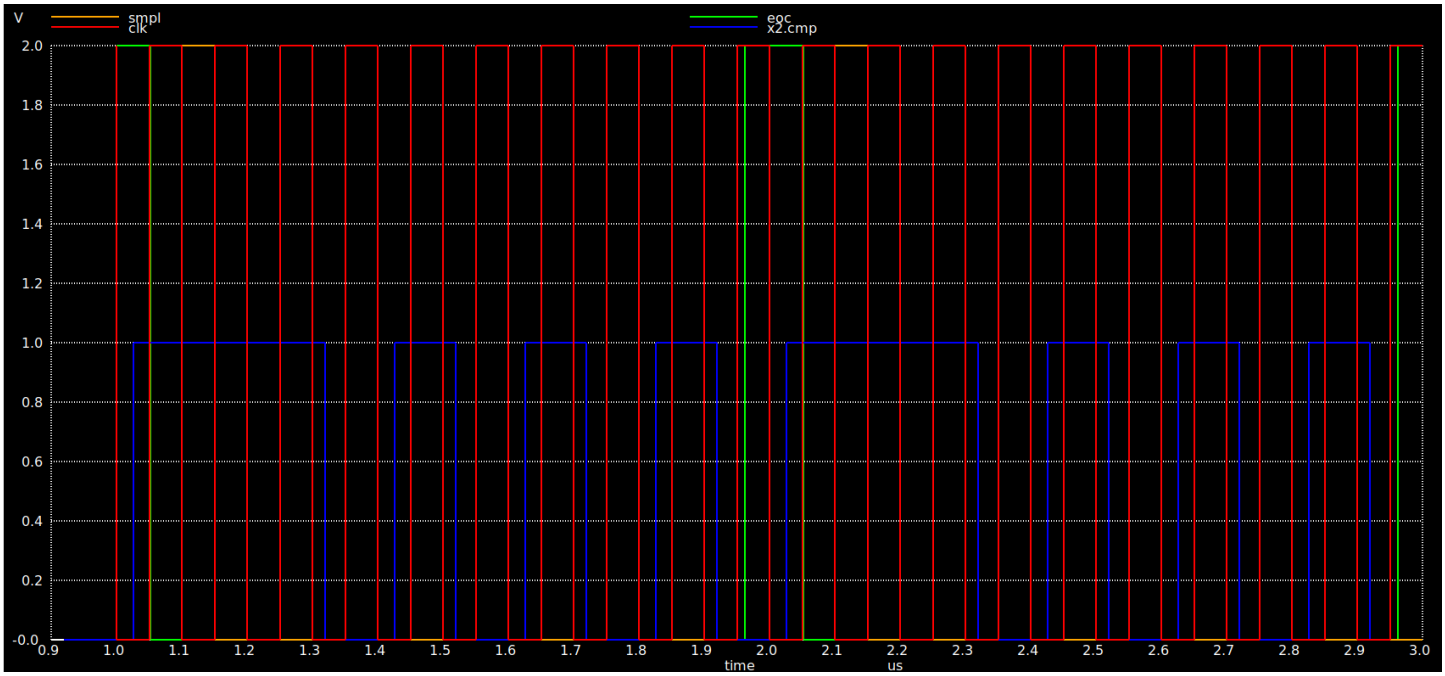
2.1 VDC=VREFN:



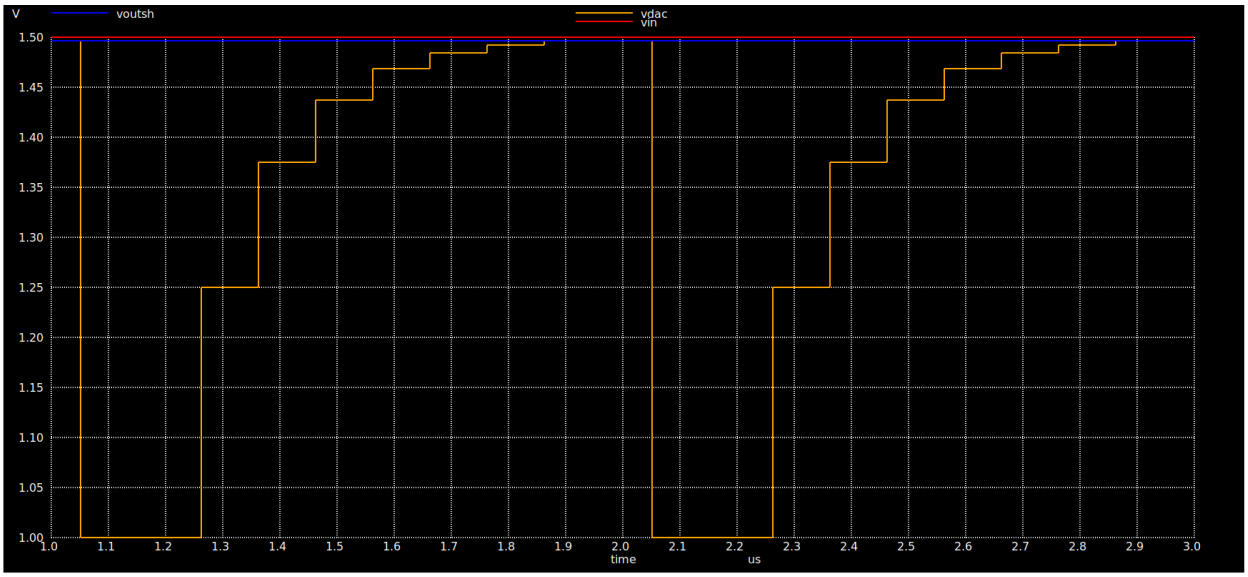
2.2 VIN = VREFN + (128+32+8+2+0.5)*VLSB:



2.2.1 CLK, smpl, eoc



2.3 VIN = VREFP:


V
voutsh
vdac
vin
1.50
1.45
1.40
1.35
1.30
1.25
1.20
1.15
1.10
1.05
1.00
1.0
1.1
1.2
1.3
1.4
1.5
1.6
1.7
1.8
1.9
2.0
2.1
2.2
2.3
2.4
2.5
2.6
2.7
2.8
2.9
3.0
time
us