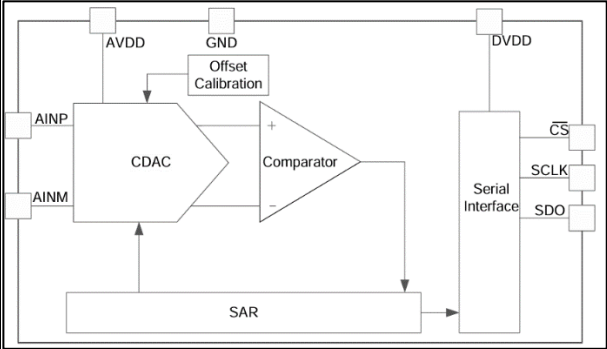
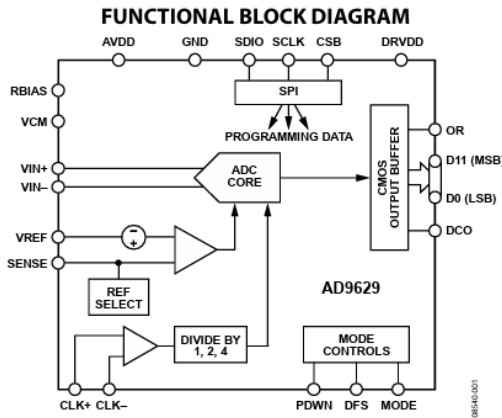
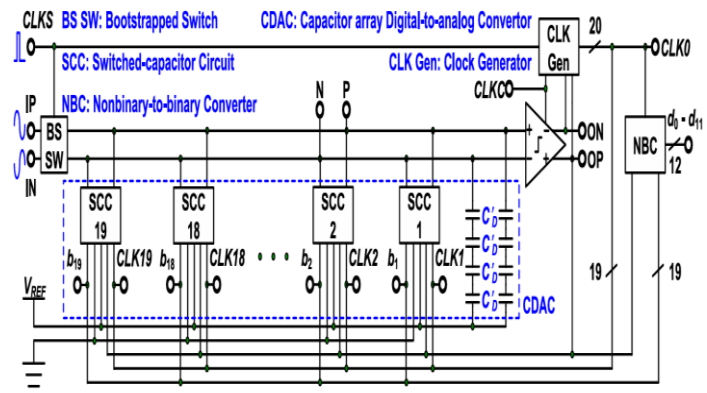


	TI: ADS7047	ADI : AD9629-20	H.-L. Kuo et al.: 18.39 fJ/Conversion-Step 1-MS/s 12-bit SAR ADC
Architecture	SAR	Pipelined	SAR
Block diagram	 <p>The block diagram of the TI ADS7047 shows an internal structure with an AVDD and DVDD supply rails. It includes an Offset Calibration block, a CDAC (Capacitor Digital-to-analog Converter), a Comparator, a SAR (Successive Approximation Register), and a Serial Interface. The SAR is connected to the CDAC and the Comparator. The Serial Interface has pins for CS, SCLK, SDO, and SDI.</p>	 <p>The functional block diagram of the AD9629 shows a complex internal structure. It includes an ADC CORE, a CMOS OUTPUT BUFFER, a MODE CONTROLS block, and a DIVIDE BY 1, 2, 4 block. The ADC CORE is connected to the CMOS OUTPUT BUFFER and the MODE CONTROLS. The MODE CONTROLS block has pins for PDWN, DFS, and MODE. The DIVIDE BY 1, 2, 4 block is connected to the CLK+ and CLK- pins. The ADC CORE has pins for RBIAS, VCM, VIN+, VIN-, VREF, and SENSE. The CMOS OUTPUT BUFFER has pins for OR, D11 (MSB), D0 (LSB), and DCO. The MODE CONTROLS block has pins for AVDD, GND, SDIO, SCLK, CSB, and DRVDD. The DIVIDE BY 1, 2, 4 block has pins for CLK+ and CLK-.</p>	 <p>The architecture of the proposed 12-bit SAR ADC shows a detailed internal structure. It includes a CLK Gen (Clock Generator), a BS SW (Bootstrapped Switch), a CDAC (Capacitor array Digital-to-analog Converter), a SCC (Switched-capacitor Circuit), a NBC (Nonbinary-to-binary Converter), and a CLKO pin. The CLK Gen is connected to the BS SW and the CDAC. The BS SW is connected to the SCC and the NBC. The CDAC is connected to the SCC and the NBC. The SCC is connected to the NBC. The NBC is connected to the CLKO pin. The CLKO pin has a pin number 20. The BS SW has pins for BS and SW. The CDAC has pins for VREF and CLKO. The SCC has pins for CLK19, CLK18, CLK2, CLK1, and CLKO. The NBC has pins for d0, d11, and CLKO. The CLKO pin has a pin number 19.</p>
Price (\$) 1ku	1.650	6.94	
Min power supply (V)	Analog : 2.35 v Digital : 1.65 v	1.7 V	Analog : 1.4 v Digital : 0.95 v
Peak-to-peak input range (v)	3.6	2	2
Power consumption at 1 MSps (mW)	1.33	30.5 Estimated from power vs frequency curve	0.0447
Max DNL (LSB)	0.5	0.25	0.54
Max INL (LSB)	0.75	0.40	0.89
ENOB (bit)	11.8	11.5	11.25
SNR (dB)	72.9	71.4	69.51
SINAD (dB)	72.7	71.3	69.51
SFDR (dB)	89.7	95	84.95
Digital output format	Serial	Parallel	Serial

Internal reference (Yes/No)?	NO	Yes	Yes
Internal sampling clock (Yes/No)?	No	No	Yes
Walden FoM (fJ/step) @ typical values	374	776.8	18.39
Schreier FoM (dB) @ typical values	158.6	154.8	169.99