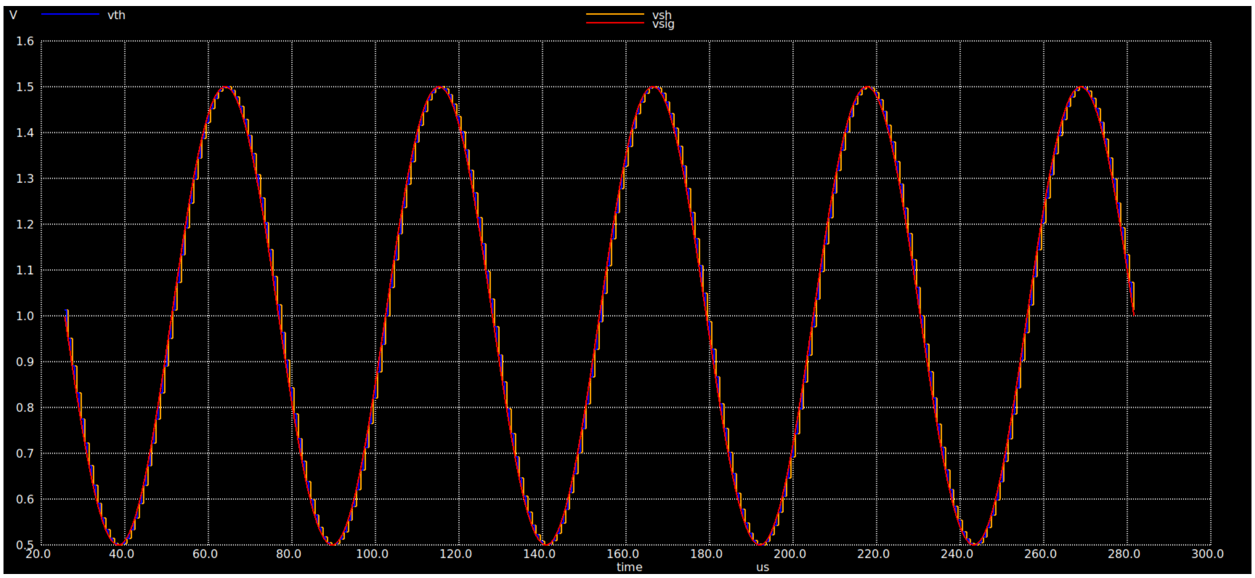
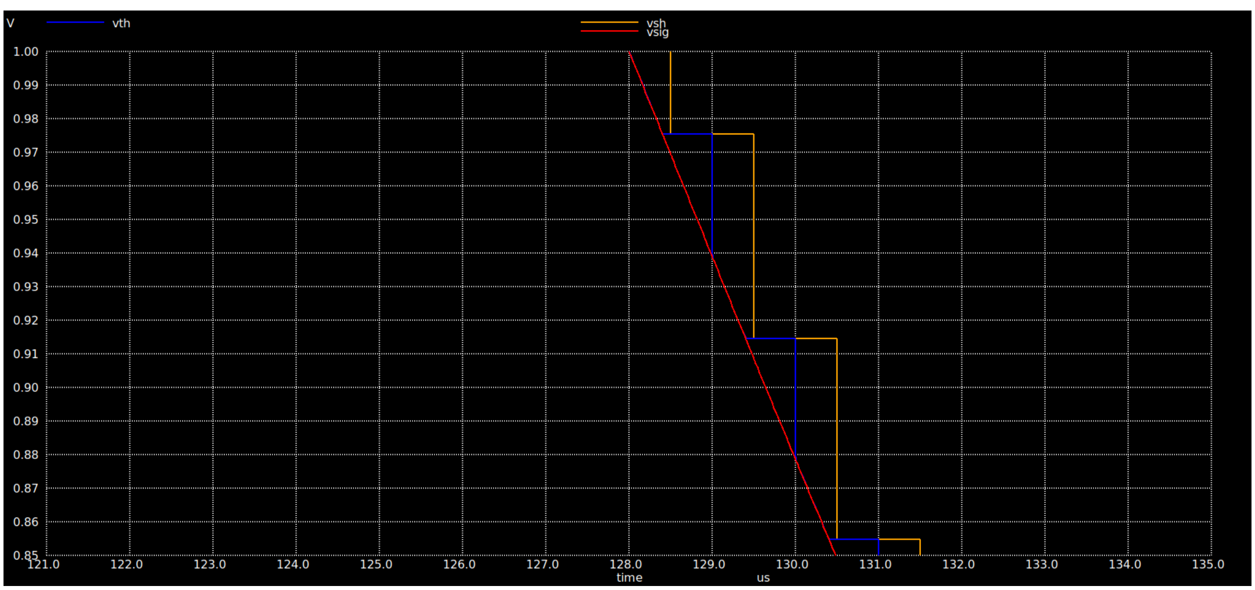
Lab 02

Part 1: Sampling and Windowing

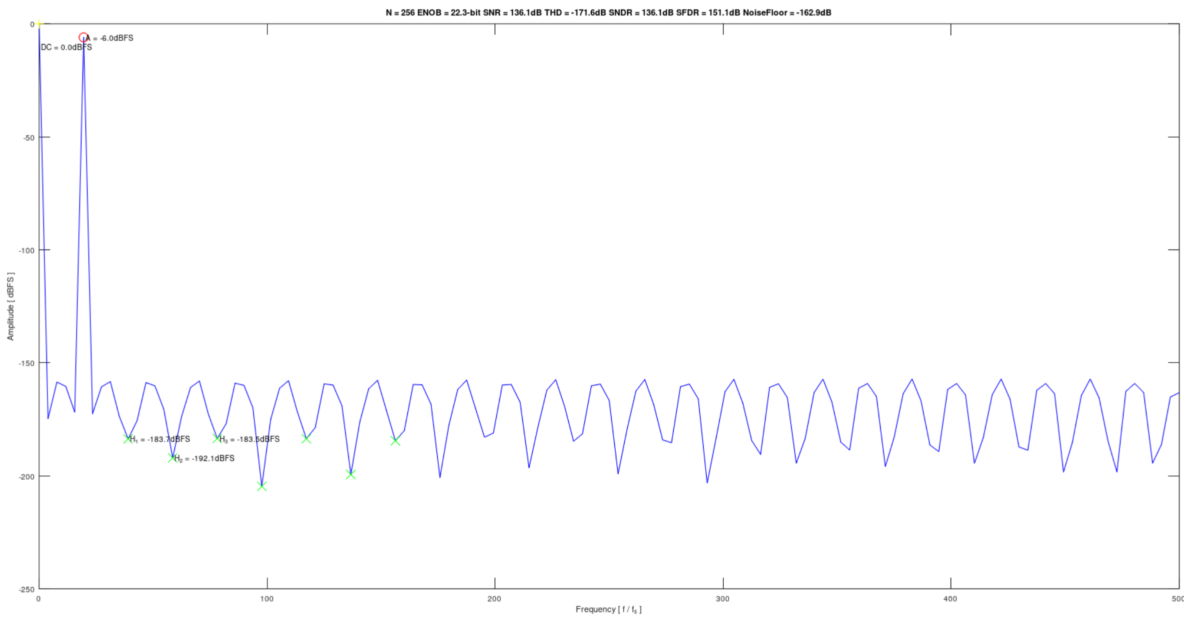
1 Plot VSIG, VTH, and VSH overlaid. Zoom in to observe the difference between T&H (VTH) and S&H (VSH).





T&H tracks the signal when the clock is high and then holds the signal when the clock is low, S&H always holds the signal on the transitions of the clock (sample the input signal).

2 USE THE PROVIDED CODE TO PLOT THE FFT OF THE SIGNAL



2.1 WHAT IS THE POWER OF THE PEAK SIGNAL (IN DB)? WHY?

The peak signal (without DC) is -6 dbfs while DC is 0 dbfs , because the amplitude of the sinusoidal signal was set to be half the DC value and 20 log(0.5) = -6 db.

2.2 HOW MANY BINS ARE OCCUPIED BY THE TEST SIGNAL?

1 bin

2.3 WHAT IS THE NOISE FLOOR (IN DBFS)?

-162.9 dbfs

2.4 WHAT IS THE RELATION BETWEEN THE SNR, NFFT, SIGNAL POWER, AND NOISE FLOOR?

As signal power increases SNR increases, and as SNR increases the noise floor decreases, and as NFFT (the number of FFT points) increases the noise floor decreases

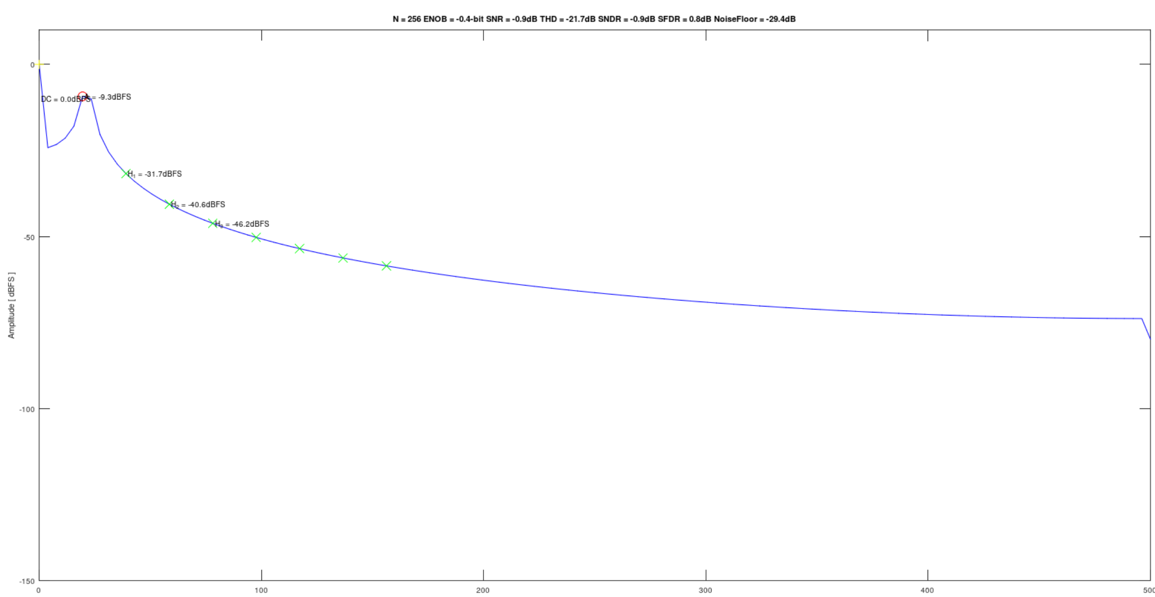
2.5 IF THE SAMPLING IS IDEAL, WHAT IS THE SOURCE OF ERROR THAT CAUSES THE NOISE FLOOR?

Simulation errors as the computer and fft operation itself gives us errors (limited quantization levels, as quantization is lossy process).

2.6 NOTE THAT IF YOU MADE THE RELTOL AND VNTOL OPTIONS IN THE SPICE CODE SMALLER, ENOB WILL INCREASE WHY ?

Because by that we decrease the tolerances, so that decreases the quantization error which will lead to increase ENOB.

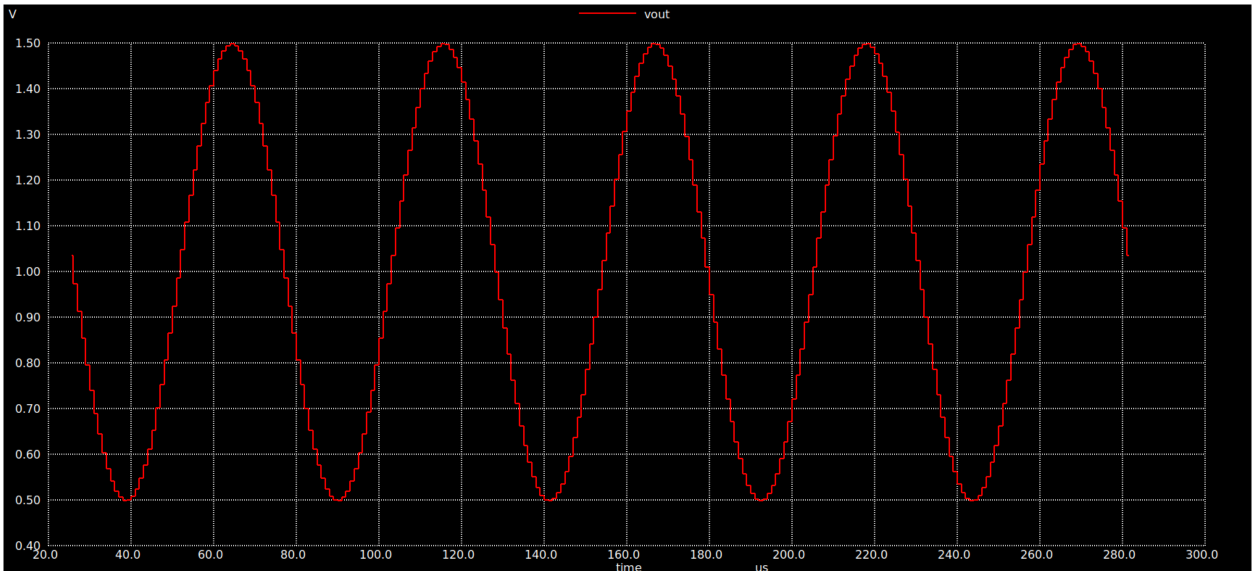
3 CHANGE NCYC TO 5.5 AND RE-SIMULATE. NOTE THAT THE START AND STOP TIME IN THE DFT WILL CHANGE FROM THE PREVIOUS CASE. PLOT THE NEW FFT. OBSERVE THE SPECTRAL LEAKAGE.

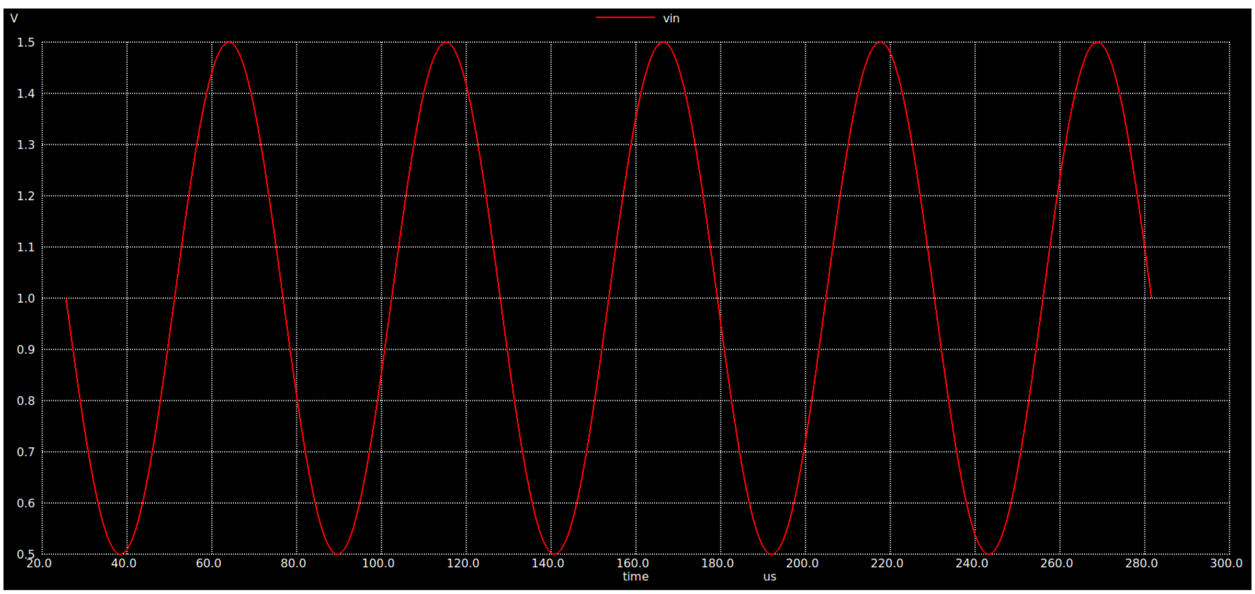


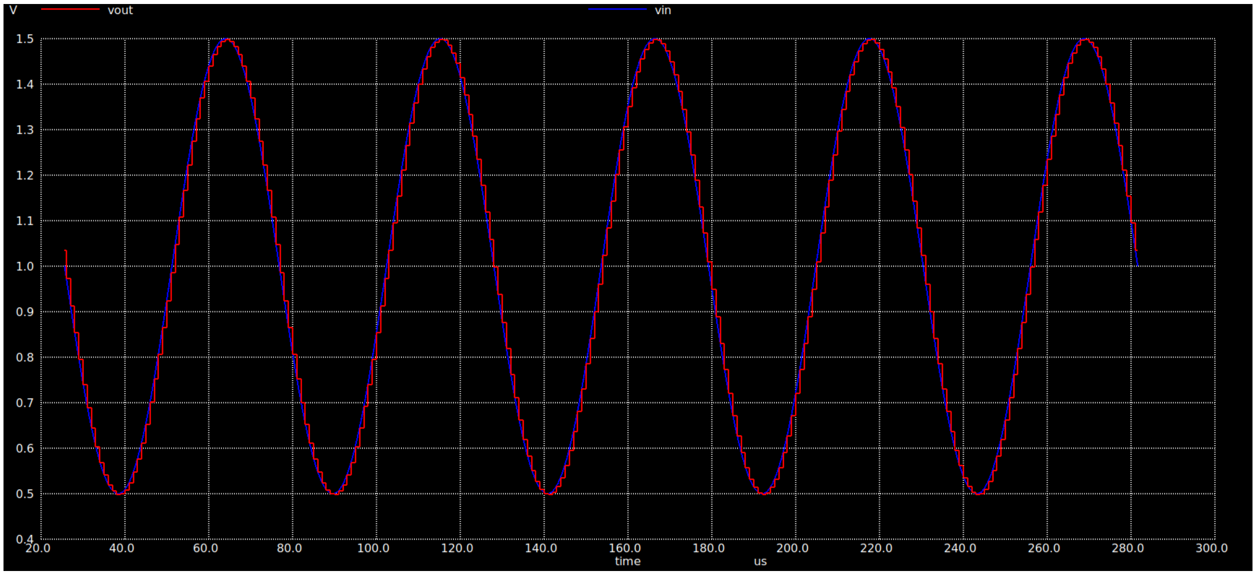
As seen there is spectral leakage and a high amplitude between our signal and the dc value, and noise floor increased much more than the previous case.

Part 2: Quantization

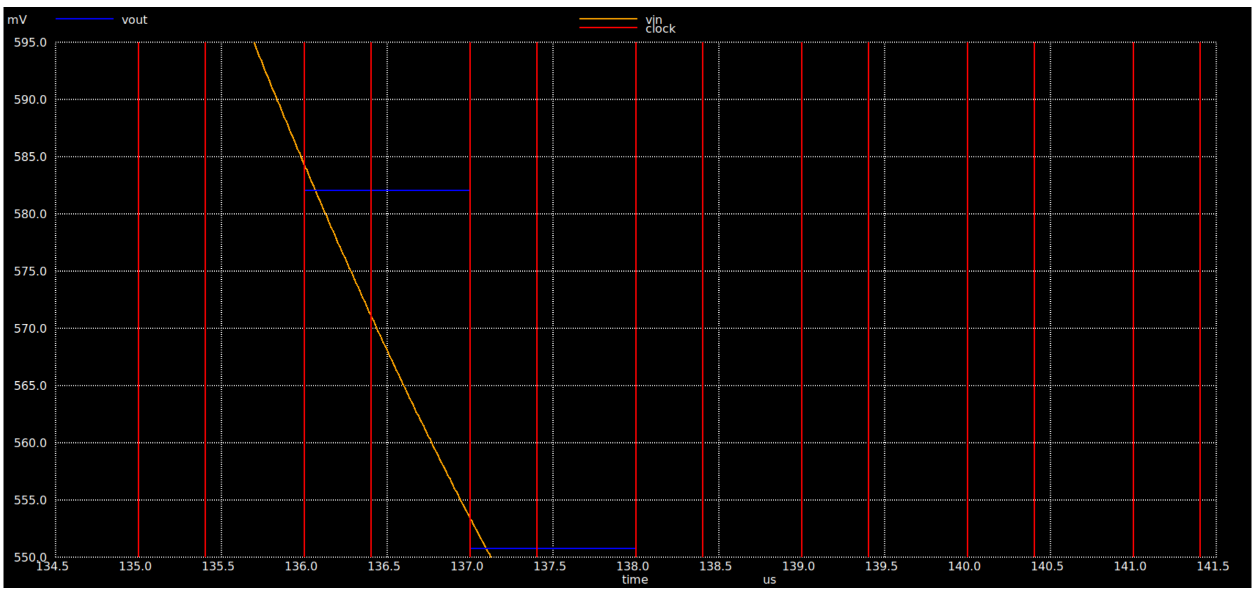
1 PLOT THE TRANSIENT WAVEFORMS AND STUDY THE TIMING RELATIONS BETWEEN DIFFERENT SIGNALS.





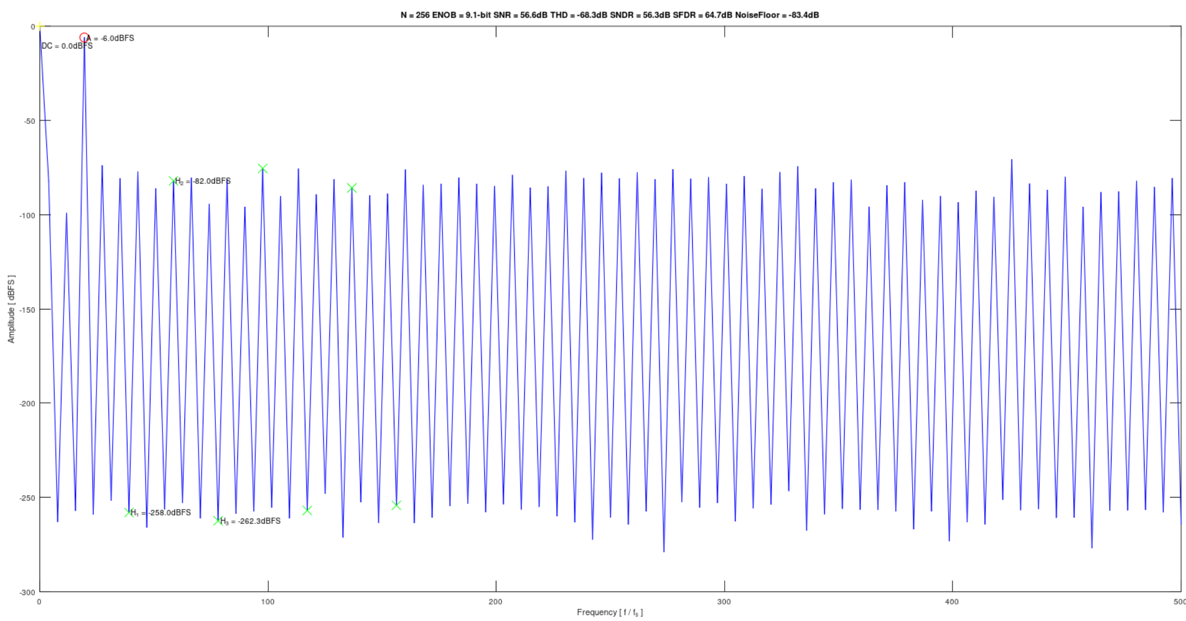


V
vout
vin
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
time
us

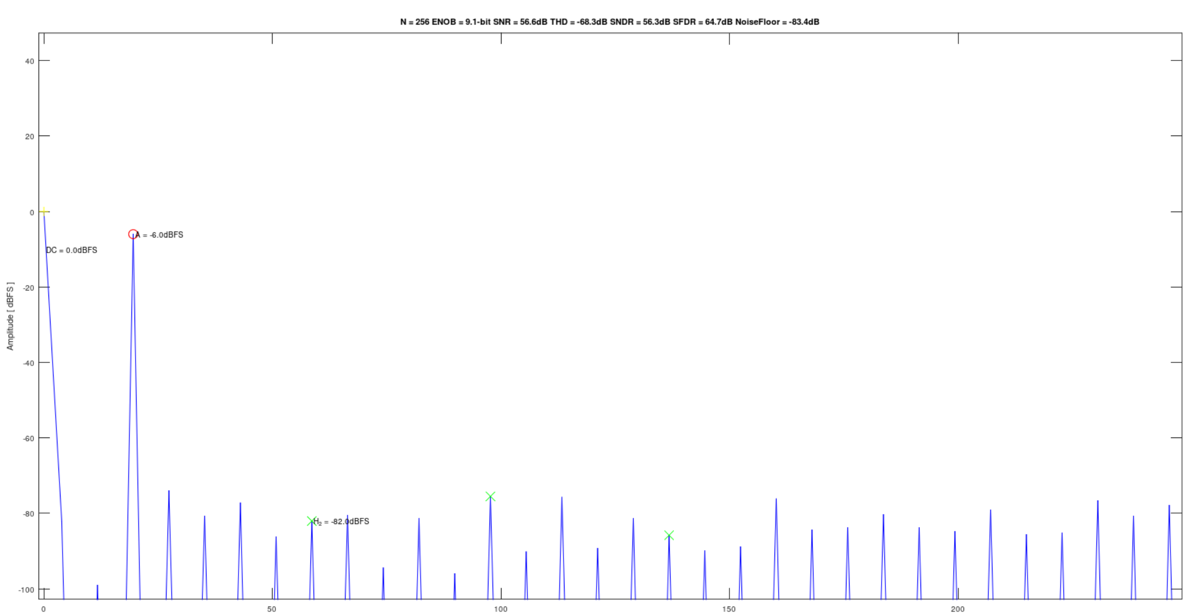


mV
vout
vin
clock
595.0
590.0
585.0
580.0
575.0
570.0
565.0
560.0
555.0
550.0
134.5
135.0
135.5
136.0
136.5
137.0
137.5
138.0
138.5
139.0
139.5
140.0
140.5
141.0
141.5
time
us

2 ANALYZE THE DAC OUTPUT USING OCTAVE FFT CODE IN THE APPENDIX. THE RESULT WILL BE AS SHOWN BELOW (ZOOM IN Y-AXIS FROM 0 TO-100DB). COMPARE THE SNR, ENOB, SIGNAL POWER, DC POWER, AND NOISE FLOOR WITH THE EXPECTED THEORETICAL VALUES.



2.1 ZOOMED:

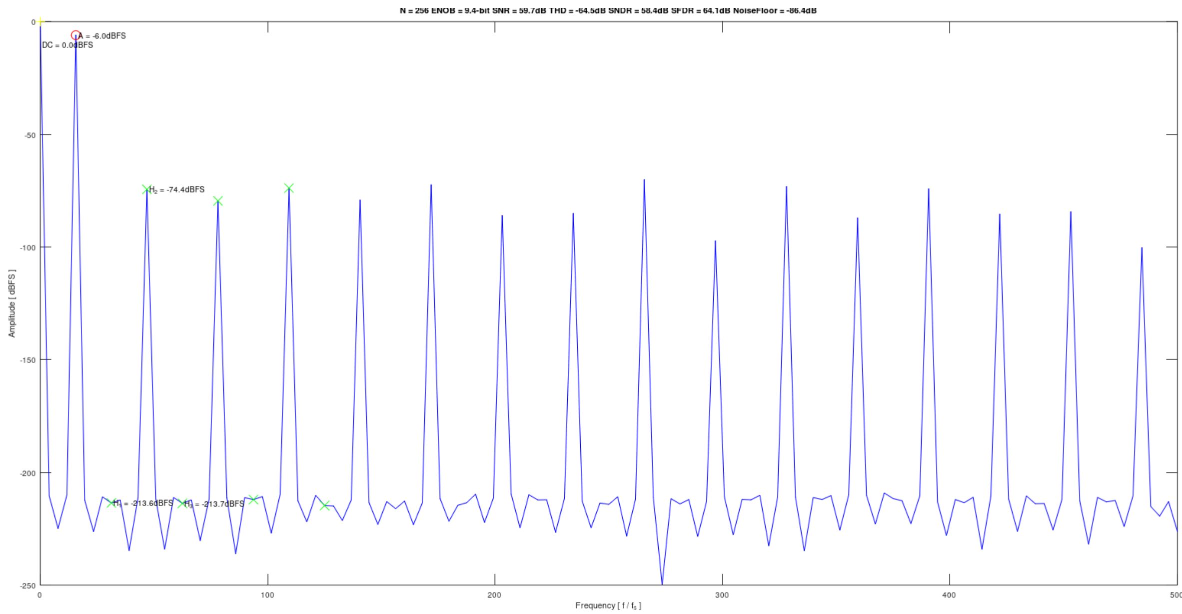


	Octave	Theoretical
SNR	56.6db	61.96dB (6.02*10+1.76)
ENOB	9.1 bits	10 bits
Signal Power	-6dbfs	-6dbfs
DC Power	0dbfs	0dbfs
Noise Floor	-83.4dbfs	- 89dbfs

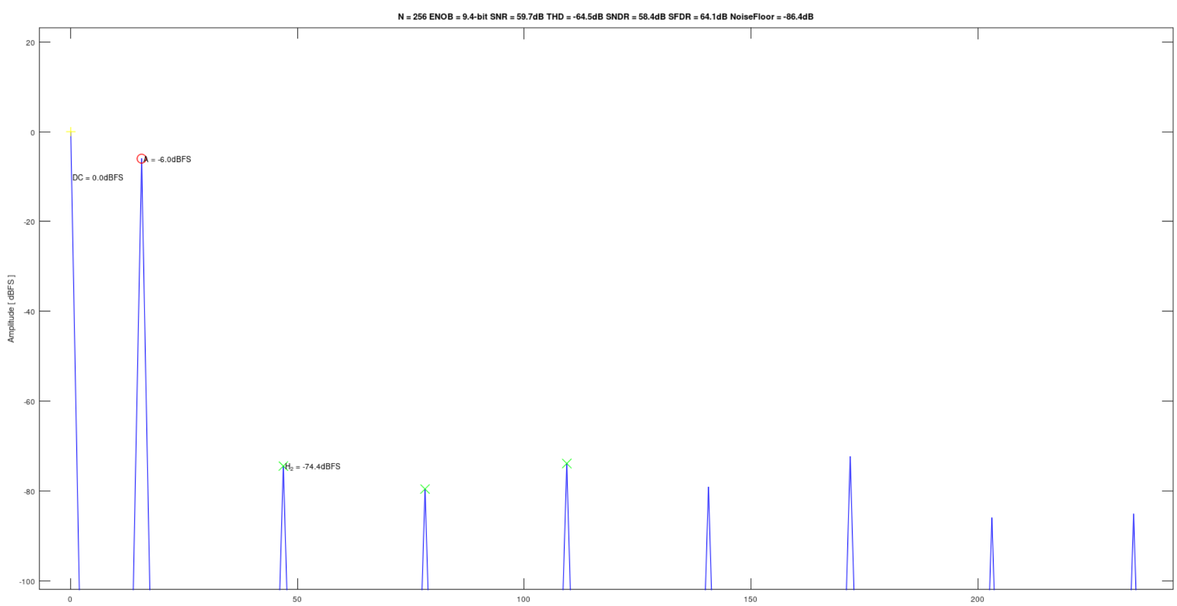
3 RECORD THE VALUE OF THE SFDR.

64.7 db

4 CHANGE NCYC TO 4 AND RE-SIMULATE (NOW NFFT/NCYC = INTEGER). PLOT THE NEW FFT.



4.1 (ZOOM IN Y-AXIS FROM 0 TO-100DB) :



4.2 Note that the start and stop time in the DFT will change from the previous case. Compare the new SFDR with the previous one. Comment.

Previous case (NCYC=5): 64.7db

This case (NCYC=4):64.1db

Now NCYC is even so NFFT /NCYC =integer which lead to the samples taken are correlated and SFDR is higher, this is a simulation error and doesn’t represent the actual performance.