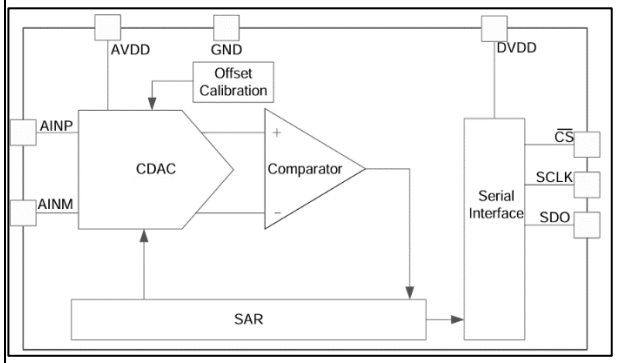
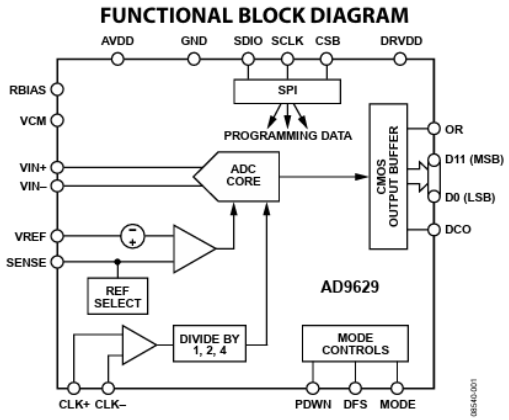
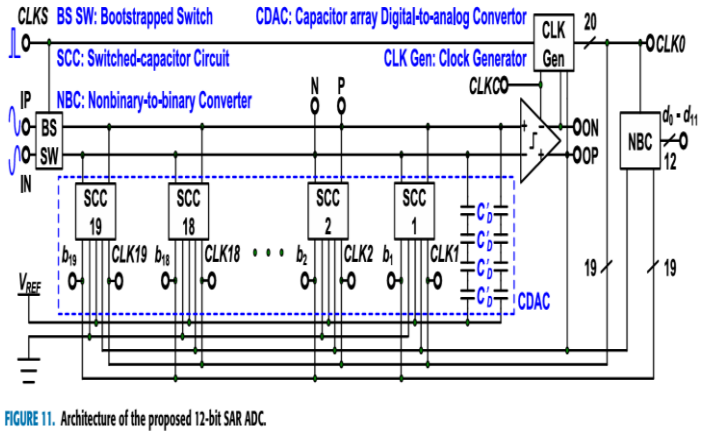
	TI: ADS7047	ADI : AD9629-20	H.-L. Kuo et al.: 18.39 fJ/Conversion-Step 1-MS/s 12-bit SAR ADC
Architecture	SAR	Pipelined	SAR
Block diagram			 FIGURE 11. Architecture of the proposed 12-bit SAR ADC.
Price ($) 1ku	1.650	6.94	
Min power supply (V)	Analog : 2.35 v Digital : 1.65 v	1.7 V	Analog : 1.4 v Digital : 0.95 v
Peak-to-peak input range (v)	3.6	2	2
Power consumption at 1 MSps (mW)	1.33	30.5 Estimated from power vs frequency curve	0.0447
Max DNL (LSB)	0.5	0.25	0.54
Max INL (LSB)	0.75	0.40	0.89
ENOB (bit)	11.8	11.5	11.25
SNR (dB)	72.9	71.4	69.51
SINAD (dB)	72.7	71.3	69.51
SFDR (dB)	89.7	95	84.95
Digital output format	Serial	Parallel	Serial

Internal reference (Yes/No)?	NO	Yes	Yes
Internal sampling clock (Yes/No)?	No	No	Yes
Walden FoM (fJ/step) @ typical values	374	776.8	18.39
Schreier FoM (dB) @ typical values	158.6	154.8	169.99