

Department of Electrical Engineering and Computing Computing Security

CSEC 202 Reverse Engineering Fundamentals

	Quiz #1		
	(22 Minutes)		
Name		ID	

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Spring 2024 Feb 15, 2024







Exam Instructions: Complete All Questions (Total: 10 Points)

Points Equally Distributed.

1. Which of the following is a common challenge when reverse engineering a complex binary?

- A) Translating the binary directly into high-level language constructs without any loss of information.
- B) Identifying and understanding the proprietary algorithms used within the binary.
- C) Enhancing the graphical user interface of the software being reverse-engineered.
- D) Converting assembly code back into the original high-level source code.

2. What is the correct sequence of phases in the gcc compilation system?

- A) Compiler, Preprocessor, Assembler, Linker
- B) Preprocessor, Compiler, Assembler, Linker
- C) Linker, Assembler, Compiler, Preprocessor
- D) Assembler, Linker, Preprocessor, Compiler

3. What part of the CPU is designed to store small amounts of data for quick access?

- A) Main memory
- B) Cache
- C) Registers
- D) Disk storage

4. What does the assembly instruction MOV EAX, DWORD PTR [A] perform in x86 32-bit architecture?

- A) Moves the value from the memory address labeled "A" into the 64-bit accumulator register.
- B) Moves the value from the memory address labeled "A" into the 32-bit accumulator register.
- C) Stores the value from the 32-bit accumulator register into the memory address labeled "A".
- D) Performs a bitwise AND operation between the value at the memory address labeled "A" and the 32-bit accumulator register.

5. What is the main advantage of the simpler hardware design in RISC architecture?

- A) More complex algorithms can be implemented
- B) Potentially more efficient use of the silicon area
- C) More cycles per instruction are possible
- D) Variable-length instructions can be executed

6. What happens during the 'Operate' step of CPU operations?

- A) The CPU turns off unnecessary functions to save energy.
- B) The ALU performs arithmetic or logical operations and stores the results in a register.
- C) The CPU requests data from the internet.
- D) Peripheral devices are checked for input.

7. After executing the following instructions, what will be the state of the Zero Flag (ZF) when the comparison happens?

MOV EAX, 5 CMP EAX, 5 JE Label

- A) The ZF will be set (ZF = 1) because EAX is not equal to 5.
- B) The ZF will be cleared (ZF = 0) because EAX is equal to 5.
- C) The ZF will be set (ZF = 1) because EAX is equal to 5.
- D) The ZF state is unpredictable.

8. What is the function of the EBP register?

- A) To point to the top of the stack.
- B) To serve as the base pointer for stack frames.
- C) To act as a data register.
- D) To function as a source index.

9. What does ISA stand for in computer architecture?

- A) Integrated System Architecture.
- B) Instruction Set Architecture.
- C) Internal Software Application.
- D) Intelligent Service Algorithm.

10. Which CPU instruction is an example of an operation dictated by the ISA?

- A) ADD EAX, EBX
- B) CREATE TABLE Users
- C) HTTP GET /index.html
- D) BOOTSTRAP SYSTEM



Bonus Question: [1 Point]

Note: This bonus point applies solely to this exam and cannot be transferred to other assignments or exams.

- 1. Using the attached ASCII table, what is the correct hexadecimal representation of the string "Hello, World"?
 - A) 48 61 6C 6C 6F 2C 20 57 6F 72 6C 64
 - B) 48 65 6C 6F 2C 20 57 6F 72 6C 64
 - C) 48 65 6C 6C 6F 2C 20 57 6F 72 6C 64
 - D) 4F 65 6C 6C 6F 2D 21 57 6F 72 6C 64

Good Luck

<u>D</u> 6	ec _	Нх	Oct	Cha	r	Dec	Нх	Oct	Html	Chr	Dec	Нх	Oct	Html	Chr	Dec	Нх	Oct	Html Cl	hr
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	1	1	001	SOH	(start of heading)	33	21	041	@#33;	1	65	41	101	A	A	97	61	141	<u>@</u> #97;	a
	2	2	002	STX	(start of text)	34	22	042	@#3 4 ;	"	66	42	102	B	В				@#98;	b
	3	3	003	ETX	(end of text)	35	23	043	a#35;	#	67	43	103	<u>4#67;</u>	C	99	63	143	@#99;	C
	4	4	004	EOT	(end of transmission)				a#36;		68			D					d	
	5	5	005	ENQ	(enquiry)				%		69			E					e	
	6	6	006	ACK	(acknowledge)				a#38;		70			F					f	
	7	7	007	BEL	(bell)	39	27	047	a#39;	1	71			G					g	
	8	8	010	BS	(backspace)	40			&# 4 0;		72	48	110	6#72;	H	104	68	150	h	h
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1	0	A	012	LF	(NL line feed, new line)	42	2A	052	6#42;	*	74			@#74;					j	
1	1	В	013	VT	(vertical tab)	43	2B	053	&#43;</td><td>+</td><td>75</td><td>_</td><td></td><td>6#75;</td><td></td><td>1</td><td></td><td></td><td>k</td><td></td></tr><tr><td>1</td><td>_</td><td>_</td><td>014</td><td></td><td>(NP form feed, new page)</td><td></td><td></td><td></td><td>a#44;</td><td>•</td><td>76</td><td></td><td></td><td>L</td><td></td><td></td><td></td><td></td><td>l</td><td></td></tr><tr><td>1</td><td>3</td><td>D</td><td>015</td><td>CR</td><td>(carriage return)</td><td></td><td></td><td></td><td>a#45;</td><td></td><td>77</td><td>_</td><td></td><td>@#77;</td><td></td><td> </td><td></td><td></td><td>m</td><td></td></tr><tr><td>1</td><td>4</td><td>E</td><td>016</td><td>SO</td><td>(shift out)</td><td>46</td><td>2E</td><td>056</td><td>&#46;</td><td>•</td><td>78</td><td>4E</td><td>116</td><td>N</td><td>N</td><td></td><td></td><td></td><td>n</td><td></td></tr><tr><td>1</td><td>5</td><td>F</td><td>017</td><td>SI</td><td>(shift in)</td><td>47</td><td>2F</td><td>057</td><td>a#47;</td><td>/</td><td>79</td><td>4F</td><td>117</td><td>O</td><td>0</td><td>111</td><td>6F</td><td>157</td><td>o</td><td>0</td></tr><tr><td>1</td><td>6 1</td><td>LO</td><td>020</td><td>DLE</td><td>(data link escape)</td><td>48</td><td>30</td><td>060</td><td>a#48;</td><td>0</td><td></td><td></td><td></td><td>P</td><td></td><td>112</td><td>70</td><td>160</td><td>p</td><td>p</td></tr><tr><td>1</td><td>7]</td><td>11</td><td>021</td><td>DC1</td><td>(device control 1)</td><td>49</td><td>31</td><td>061</td><td>a#49;</td><td>1</td><td>81</td><td>51</td><td>121</td><td>Q</td><td>Q</td><td>113</td><td>71</td><td>161</td><td>q</td><td>q</td></tr><tr><td>1</td><td>8 1</td><td>12</td><td>022</td><td>DC2</td><td>(device control 2)</td><td>50</td><td>32</td><td>062</td><td>2</td><td>2</td><td>82</td><td>52</td><td>122</td><td>R</td><td>R</td><td>114</td><td>72</td><td>162</td><td>a#114;</td><td>r</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td>(device control 3)</td><td></td><td></td><td></td><td>6#51;</td><td></td><td></td><td></td><td></td><td>%#83;</td><td></td><td>115</td><td>73</td><td>163</td><td>s</td><td>s</td></tr><tr><td>2</td><td>0 1</td><td>14</td><td>024</td><td>DC4</td><td>(device control 4)</td><td></td><td></td><td></td><td>4</td><td></td><td>84</td><td>54</td><td>124</td><td>4;</td><td>T</td><td>116</td><td>74</td><td>164</td><td>t</td><td>t</td></tr><tr><td>2</td><td>1 1</td><td>15</td><td>025</td><td>NAK</td><td>(negative acknowledge)</td><td></td><td></td><td></td><td>4#53;</td><td></td><td></td><td></td><td></td><td>%#85;</td><td></td><td></td><td></td><td></td><td>u</td><td></td></tr><tr><td>2</td><td>2 1</td><td>16</td><td>026</td><td>SYN</td><td>(synchronous idle)</td><td>54</td><td>36</td><td>066</td><td>a#54;</td><td>6</td><td>86</td><td></td><td></td><td>V</td><td></td><td>118</td><td>76</td><td>166</td><td>v</td><td>v</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td>(end of trans. block)</td><td></td><td></td><td></td><td>a#55;</td><td></td><td>87</td><td></td><td></td><td>W</td><td></td><td></td><td></td><td></td><td>w</td><td></td></tr><tr><td>2</td><td>4 1</td><td>18</td><td>030</td><td>CAN</td><td>(cancel)</td><td></td><td></td><td></td><td>a#56;</td><td></td><td>88</td><td>58</td><td>130</td><td>488; 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