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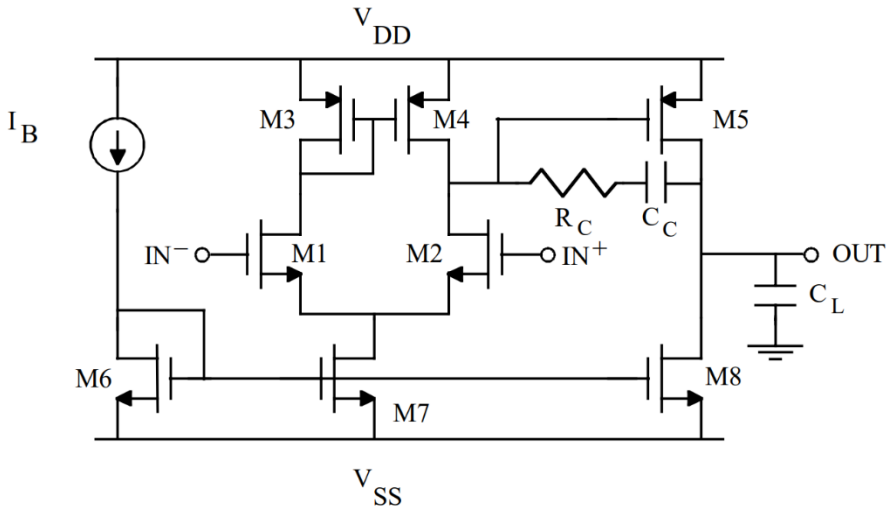
Design Exercise 3
OTA

An Operational Transconductance Amplifier (OTA) is a voltage-controlled current source (VCCS) that converts an input differential voltage into an output current.

The circuit shown represents a two-stage CMOS OTA:



The structure of this OTA includes two amplification stages, a biasing circuit, and a compensation network, all working together to achieve robust performance.

The first stage of the OTA is a differential amplifier composed of transistors M1 and M2, forming the input pair, with M3 and M4 serving as active loads implemented as a current mirror. This configuration ensures a high input impedance, making the circuit ideal for interfacing with high-impedance sources while providing the initial voltage gain. Furthermore, the tail current source, implemented with M6, stabilizes the bias current for the input transistors, ensuring precise operation over varying conditions.

The second stage of the OTA provides additional voltage gain through transistor M5, which amplifies the signal from the first stage. The current mirror composed of M7 and M8 in the second stage ensures proper current steering and further contributes to the circuit's efficiency.

This design achieves high gain through the combined contributions of the two amplification stages, which can be expressed approximately as:

$$A_v = g_{m1,2} \cdot g_{m5} \cdot (r_{o3} || r_{o1,2}) \cdot r_{o5}$$

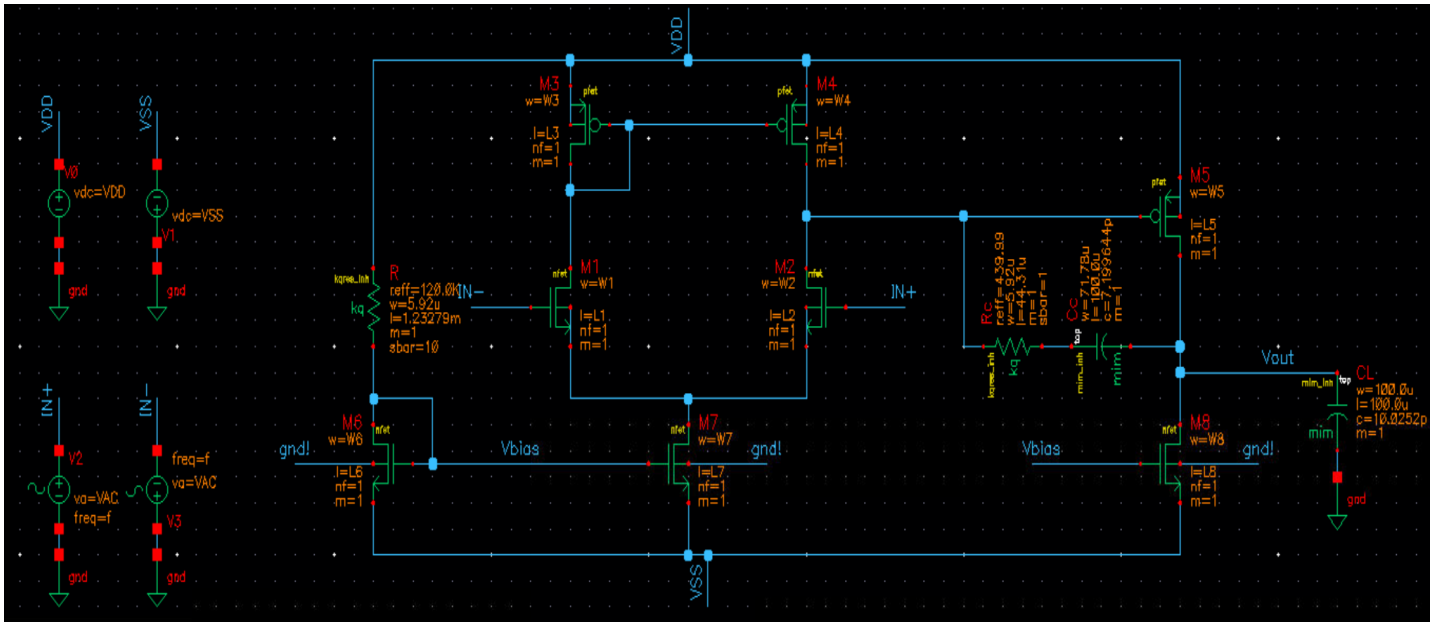
In this circuit, compensation is achieved using the Miller capacitor C_c and, optionally, a series resistor R_c. The Miller capacitor introduces a dominant pole at the output of the first stage, effectively reducing the gain at higher frequencies.

The addition of the optional resistor R_c in series with C_c can further improve the phase margin. This is achieved by introducing a low-frequency zero that cancels out one of the non-dominant poles, thereby reducing the phase lag caused by higher-frequency poles. The result is a more stable amplifier with improved transient response and a wider range of stable feedback conditions.

The design specifications are:

Parameter	Value	Physical
VDD	1	$Volts$
VSS	-1	$Volts$
Minimum small signal Gain - A_0	60	dB
Minimum GBW	100	MHz
Load Capacitance	10	pF
Phase Margin	>45	$Degrees$
Power Dissipation	Keep as low as possible	$Watts$
Dynamic range	Keep as high as possible	

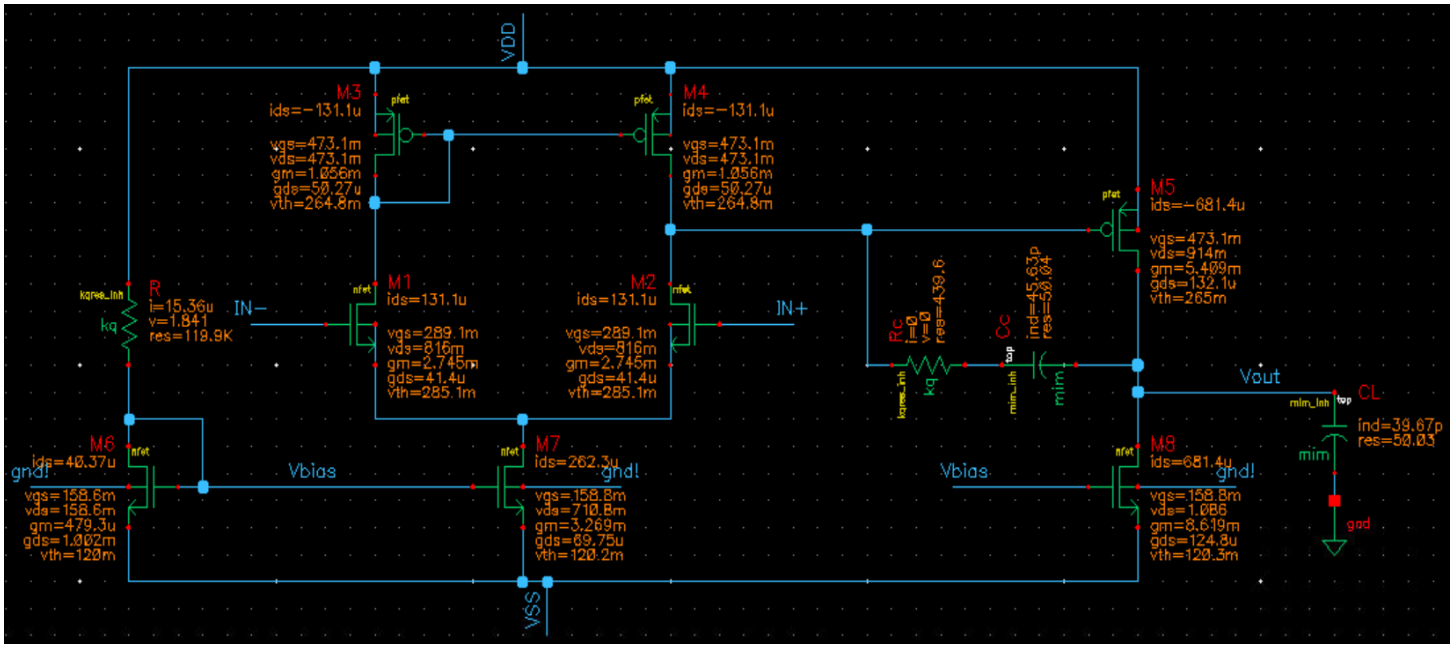
Circuit Schematic

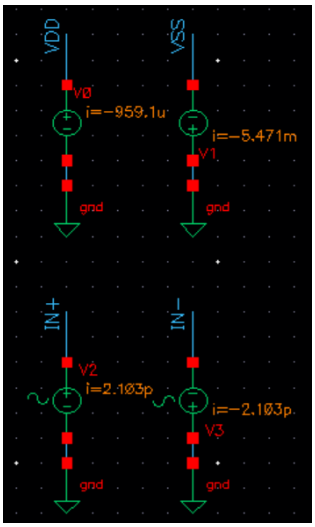


Device Dimensions table

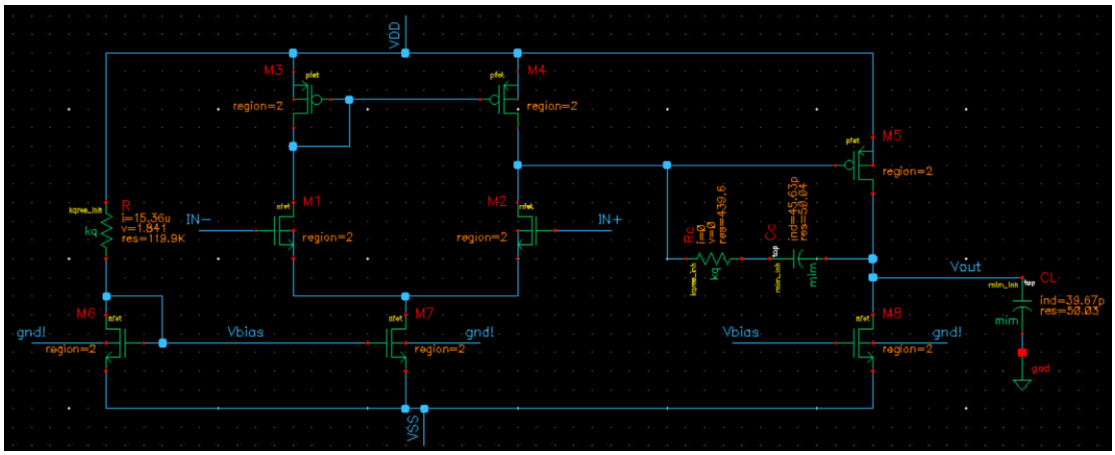
	Total width (μm)	Length (μm)	g_m (Ω^{-1})	g_{ds} (Ω^{-1})	Resistance (Ω)	Capacitance (pF)
M_1	56	0.5	2.745m	41.4u		
M_2	56	0.5	2.745m	41.4u		
M_3	34	0.5	1.056m	50.27u		
M_4	34	0.5	1.056m	50.27u		
M_5	155	0.5	5.409m	132.1u		
M_6	7	0.5	479.3u	1.002m		
M_7	35	0.5	3.269m	69.75u		
M_8	83.5	0.5	8.619m	124.8u		
R					120K	
R_c					440	
C_c						7.2

Circuit Operation Point





All the transistors are in saturation region.



DC Power Consumption

The total DC power consumption of the circuit is determined by the currents drawn from the power supplies and their respective voltages.

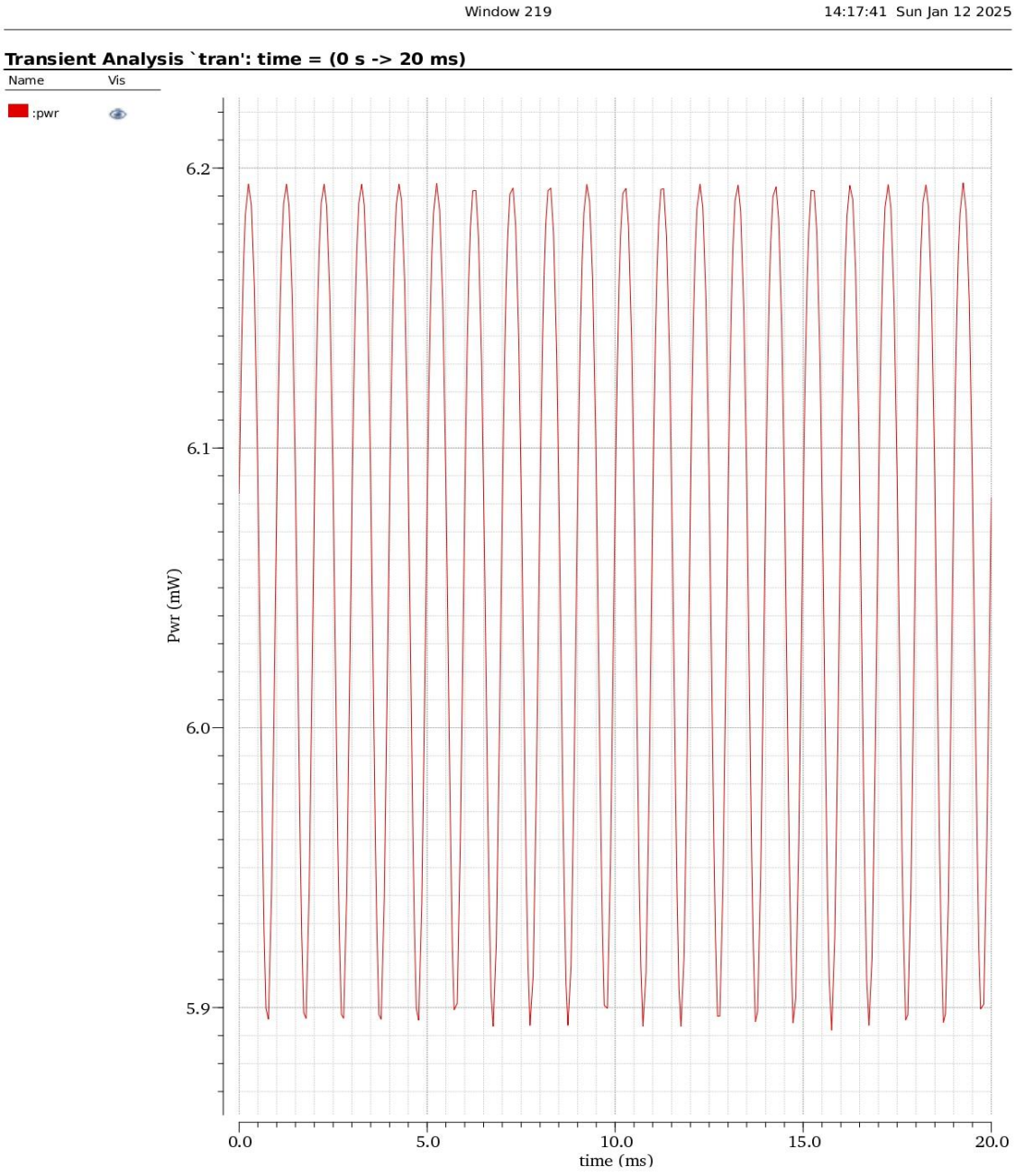
Using the following standard formula, the total power is calculated by considering the contributions from both the positive V_{DD} and negative V_{SS} supply rails:

$$P_{total} = V_{DD} \cdot I_{DD} + |V_{SS}| \cdot I_{SS}$$

The simulation provides an accurate estimation of the circuit's power consumption under DC conditions:

average(getData(":pwr" ?result "tra...

	Expression	Value
0	average(getData(":pwr" ?result "tran"))	6.063E-3

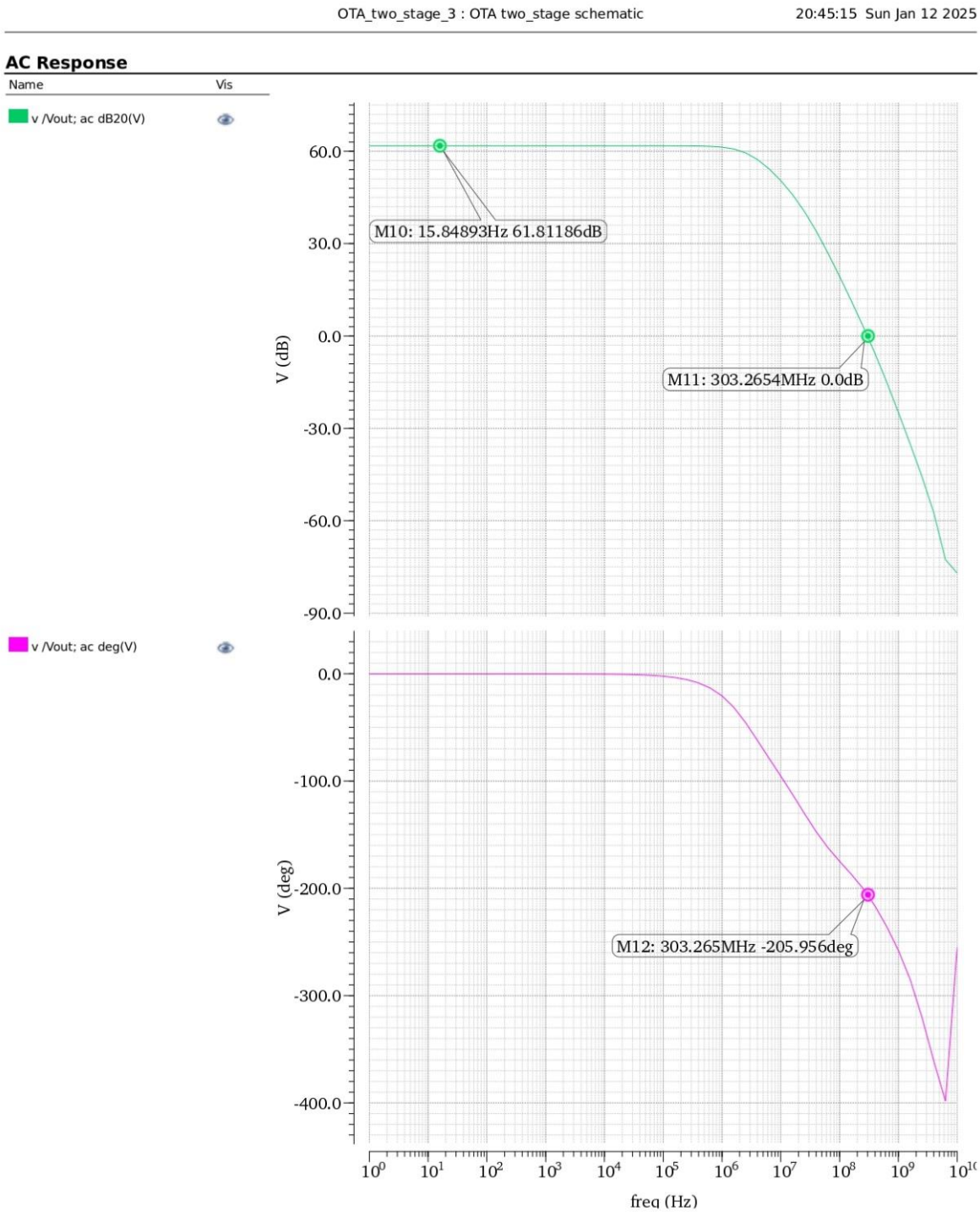


AC Simulation: Gain and Phase response

An AC analysis was conducted to determine the amplifier's frequency response. The results indicate that the amplifier achieves a low-frequency gain of **61.8 dB**, a gain-bandwidth product of **303.26 MHz**, and exhibits the expected phase behavior across the frequency range.

These results confirm that the amplifier's performance aligns with the required metrics.

Important note: This simulation was performed without the compensation loop. The effect of using R_c and C_c on the gain and phase came later in the "Stability Simulation" section.



AC Simulation: CMRR

The Common-Mode Rejection Ratio (CMRR) quantifies an amplifier's ability to reject signals that appear simultaneously at both inputs, relative to how it amplifies differential signals.

Mathematically, it is the ratio of the differential gain A_{diff} to the common-mode gain A_{cm}:

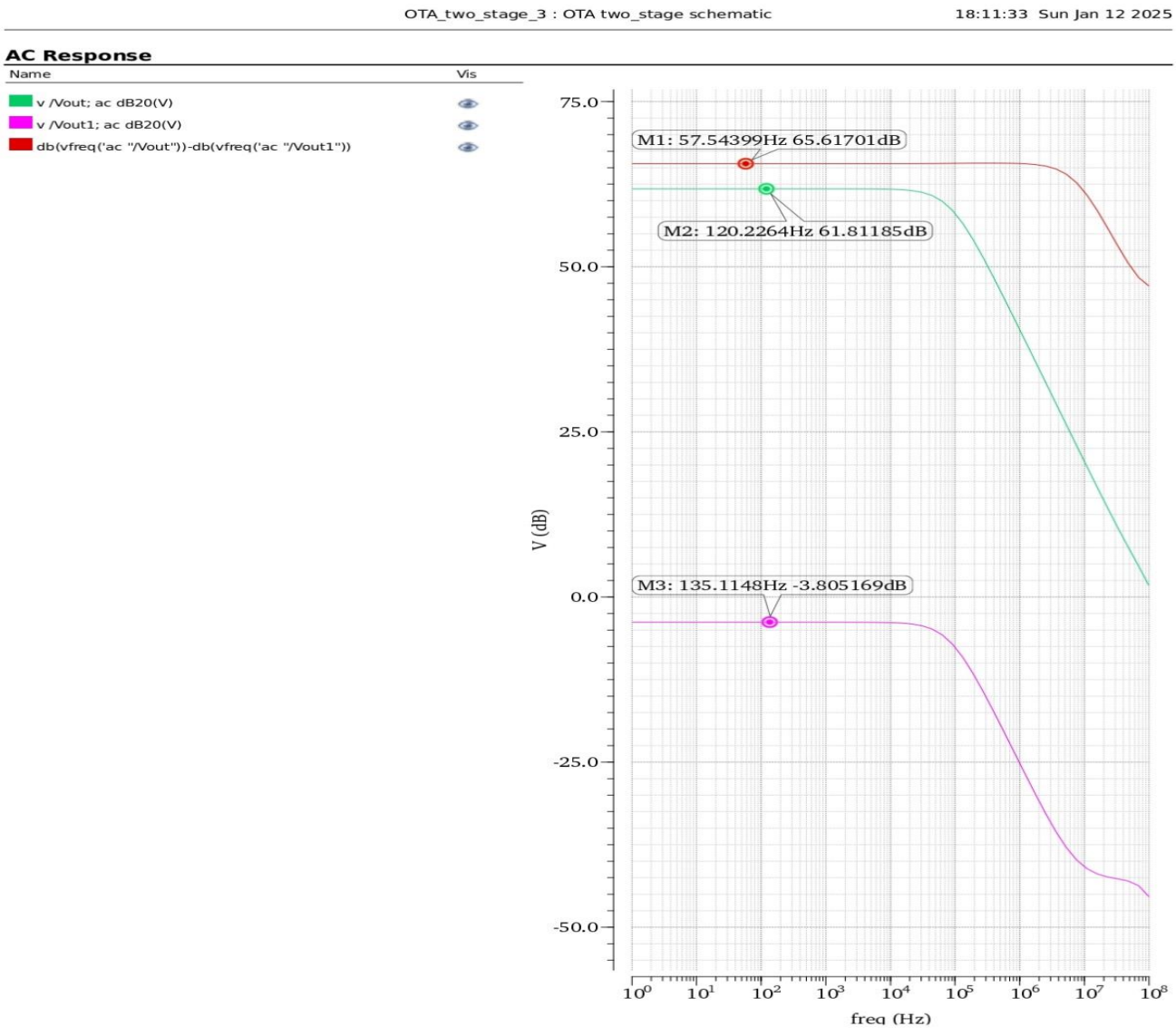
$$CMRR = \frac{A_{diff}}{A_{cm}}$$

Often, we express it in decibels (dB) as:

$$CMRR_{dB} = 20log_{10}(CMRR) = 20log_{10}\left(\frac{A_{diff}}{A_{cm}}\right) = 20log_{10}(A_{diff}) - 20log_{10}(A_{cm})$$

The calculated CMRR from the simulation was **65.61701 dB**.

Green - A_{diff} Pink - A_{cm} Red - CMRR



AC Simulation: I/O impedance

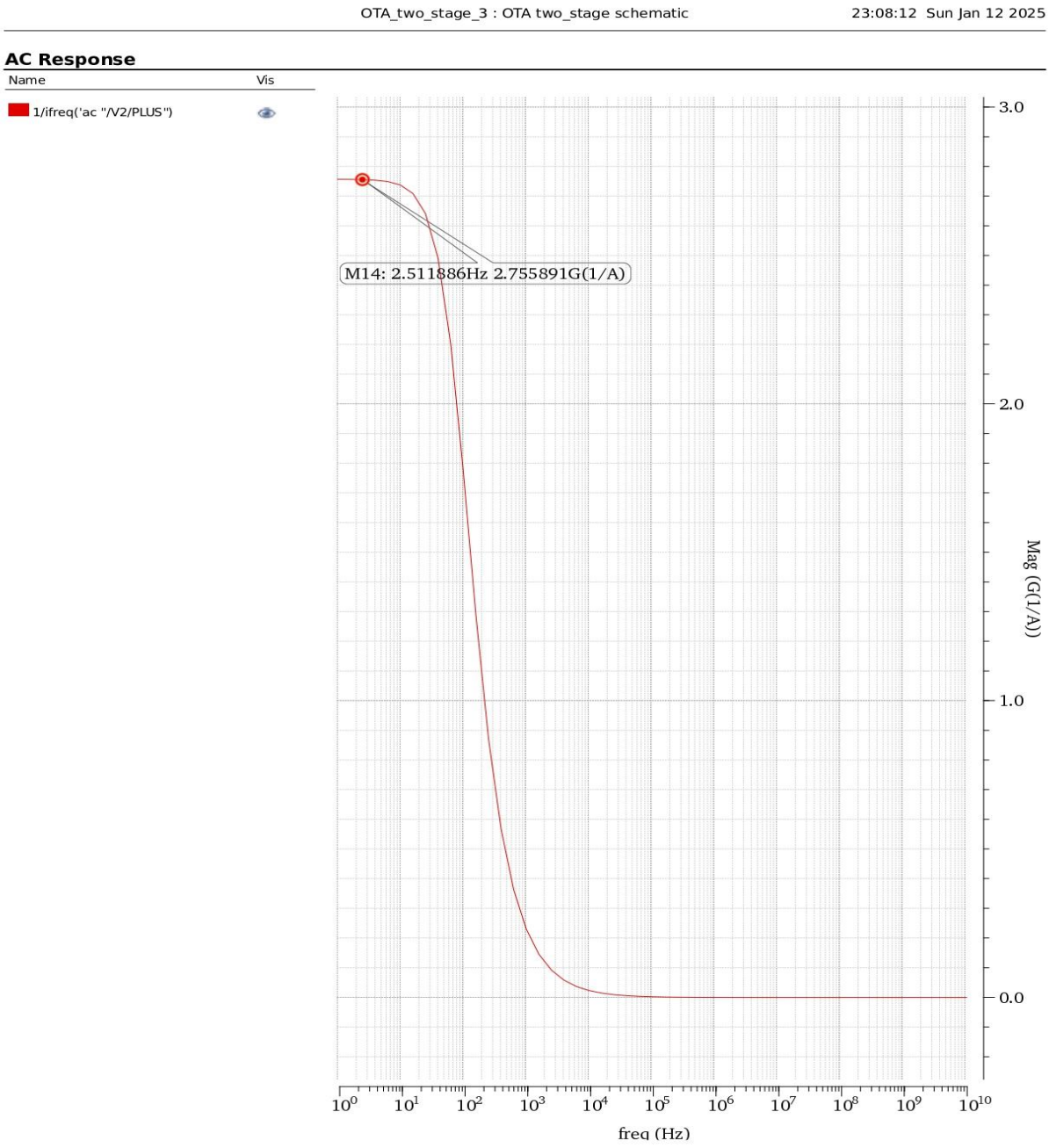
The impedance measurements were conducted by introducing a small-signal test source. The test source applied a small AC stimulus, and the resulting voltage and current were measured. The impedance was then calculated using the relationship:

$$Z = \frac{V}{I}$$

In the measurement, an AC signal with a magnitude of 1V was applied. With this setup, the impedance can be directly calculated as the reciprocal of the resulting current:

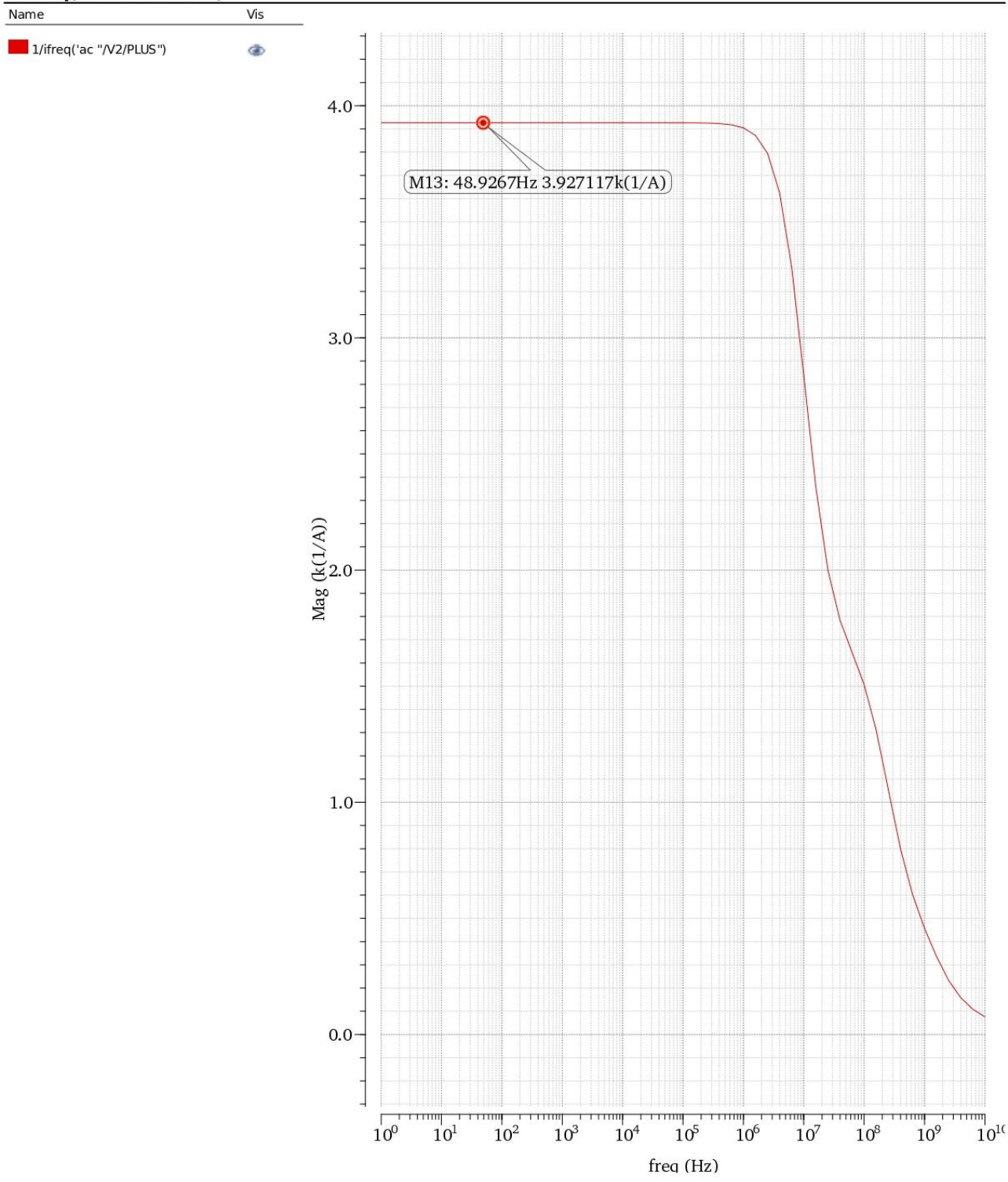
$$Z = \frac{1}{I}$$

$R_{in,max} = 2.7[G\Omega]$:



$R_{out,max} = 3.9[k\Omega]$:

1/ifreq('ac "/V2/PLUS")



Transient Simulation: Output Voltage Swing for a differential input signal of 0.5mV amplitude and 1kHz frequency

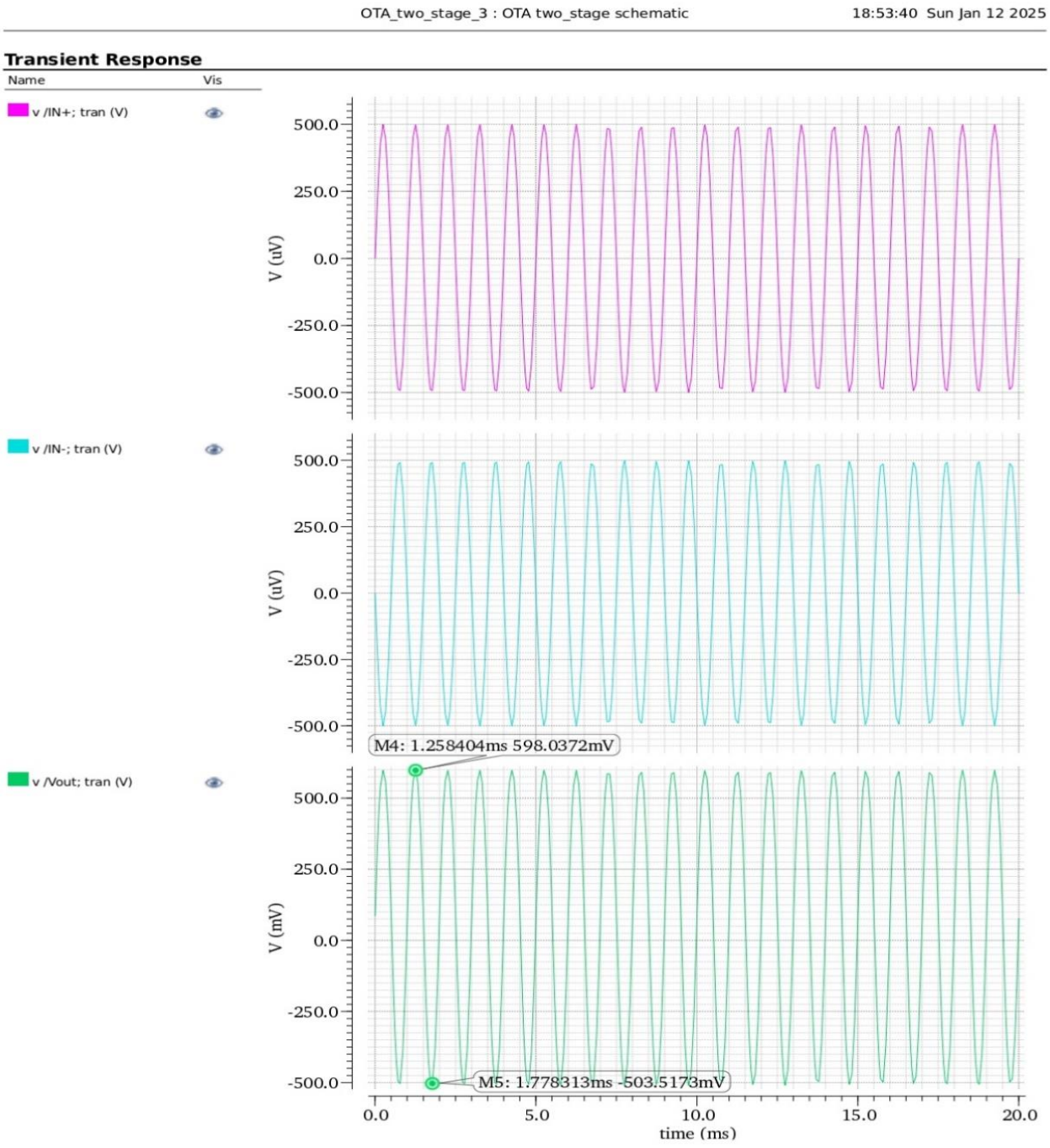
voltage swing shows the range the circuit's output can achieve without distortion or clipping. It reflects the amplifier's ability to reproduce the input signal.

From the simulation results we got a sine wave with:

- Maximum voltage: $V_{max} = 598.0372\ mV$
- Minimum voltage: $V_{min} = -503.5173\ mV$

the voltage swing is calculated as:

$$V_{pp} = 598.0372\ mV - (-503.5173\ mV) = 1101.5545\text{mV} \approx 1.1\text{V}$$

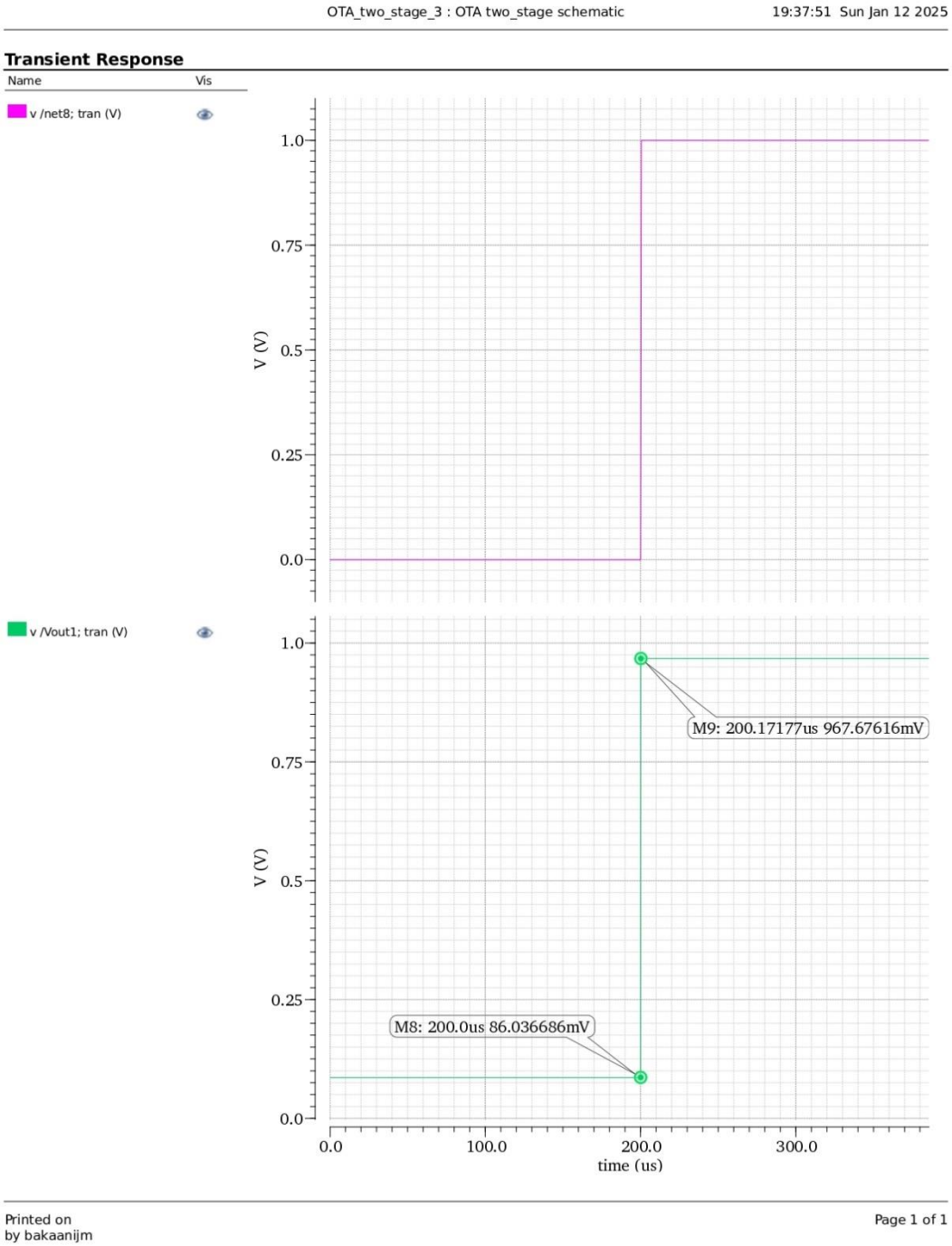


Transient Simulation: Slew Rate

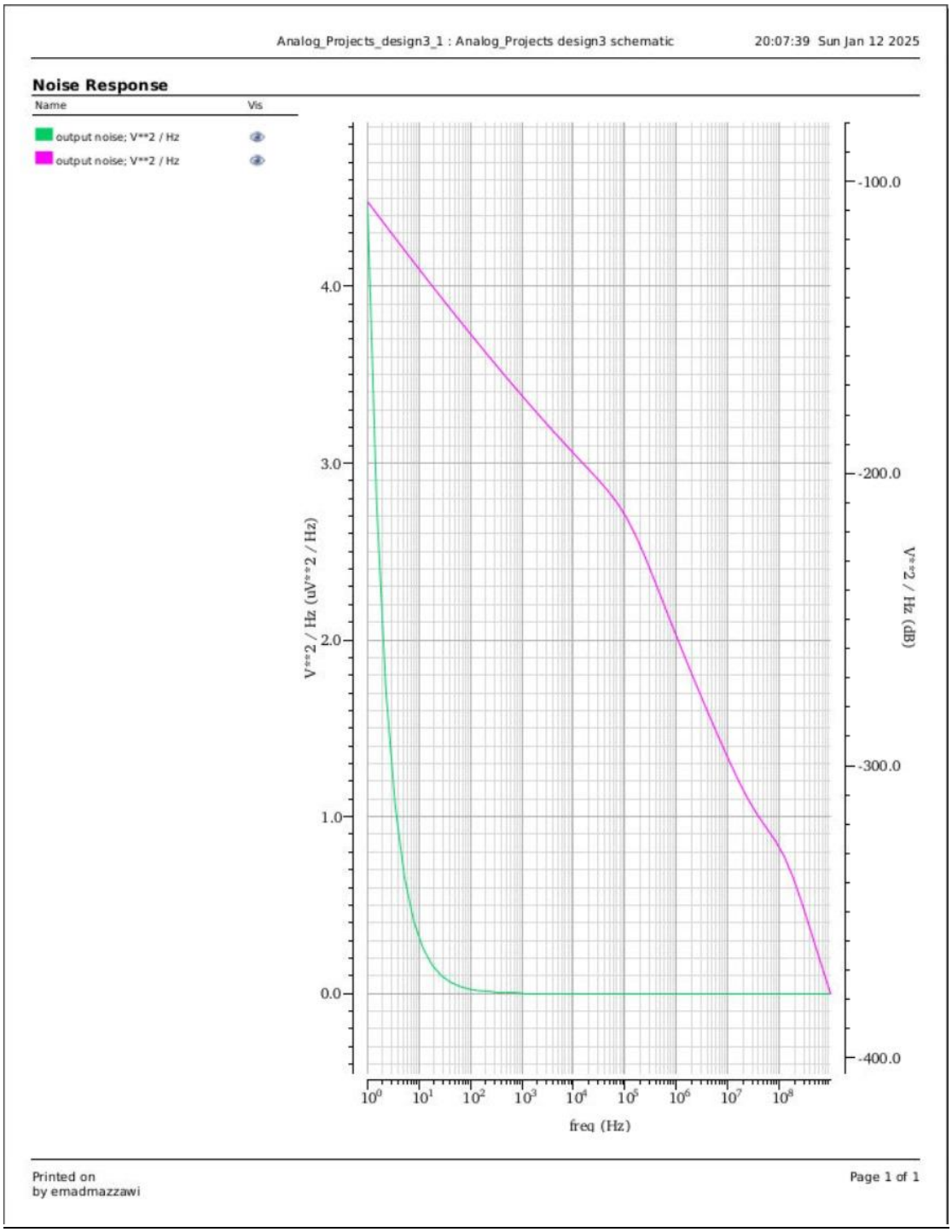
To evaluate the slew rate of the amplifier, a transient simulation was performed using an 1V impulse source as the input signal. The impulse signal ensures a rapid change at the input, driving the amplifier into a slew-limited region.

The slope of the steepest part of the output voltage was calculated to determine the slew rate:

$$Slew\ Rate = \frac{\Delta V_{out}}{\Delta t} = \frac{967.67616mV - 86.036686mV}{200.17177\mu s - 200\mu s} = 5.13\ \left[\frac{V}{\mu s}\right]$$

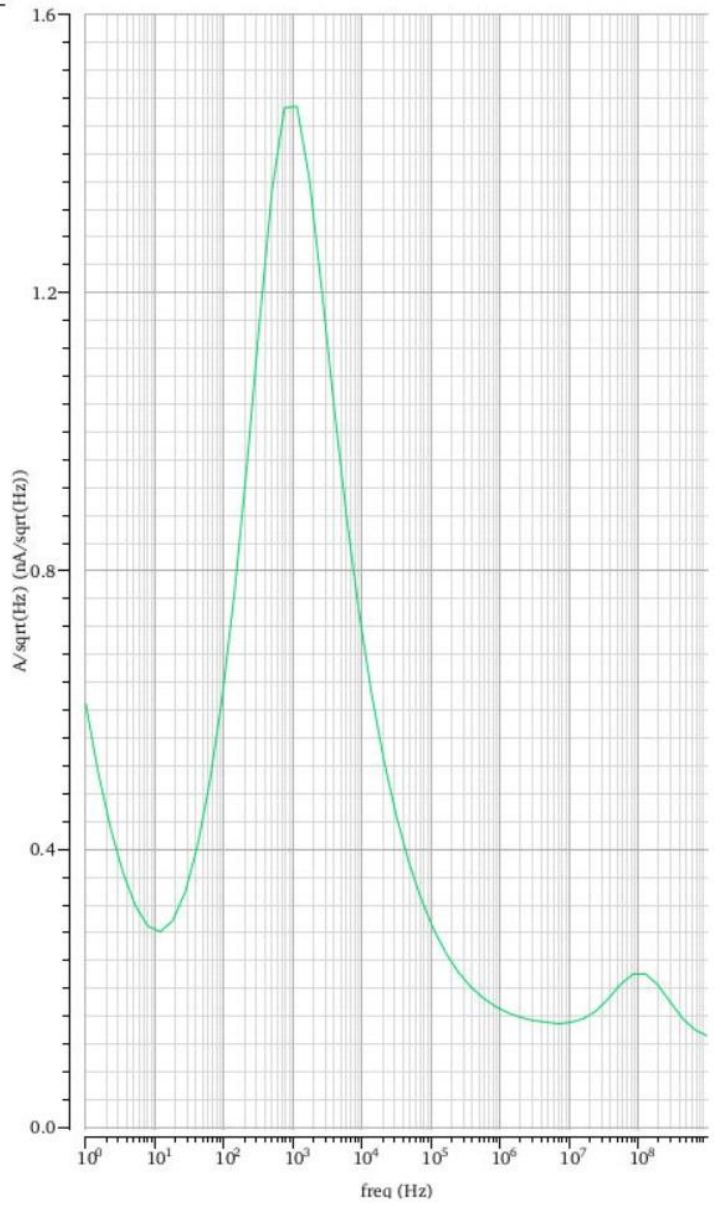


Noise Simulation: Output Referred Voltage and Current Noise

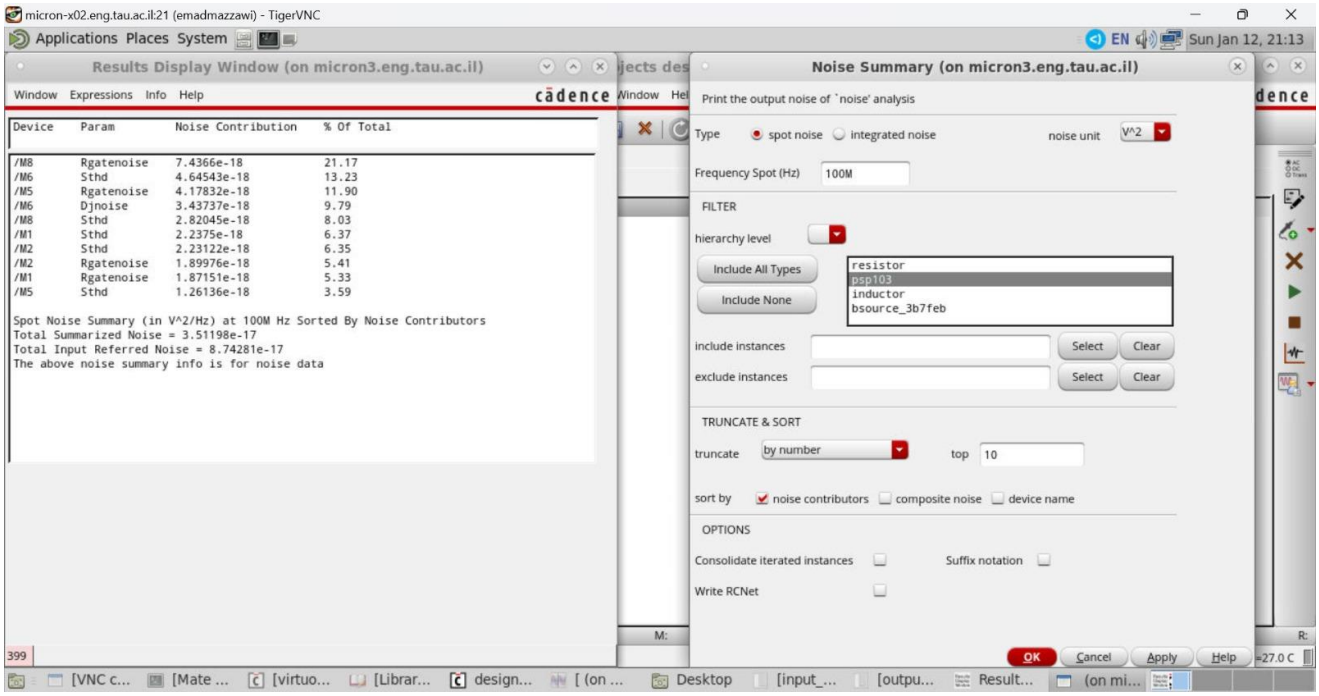


Noise Response

Name	Vis
input noise; V / sqrt(Hz)	



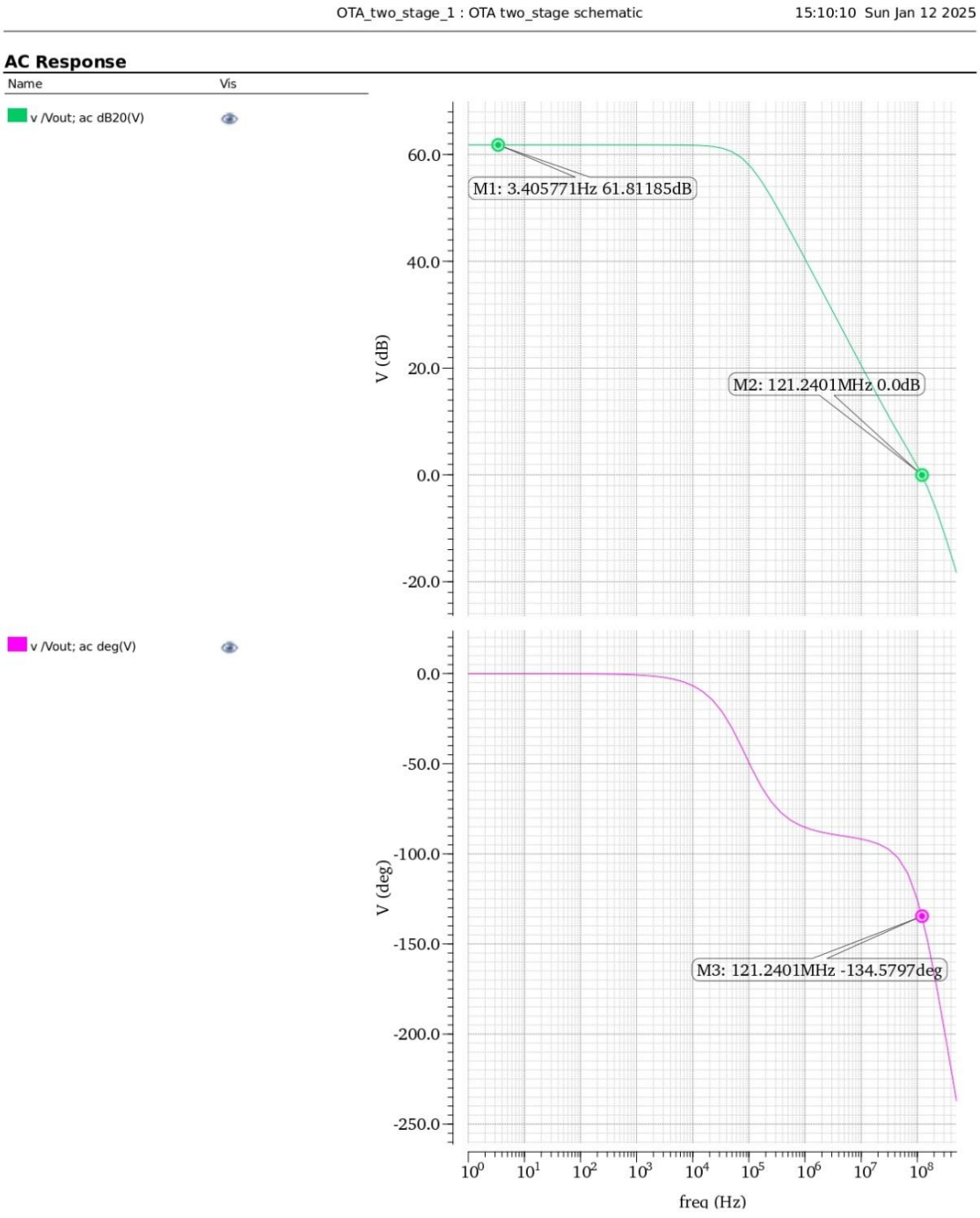
Noise Simulation: noise summary



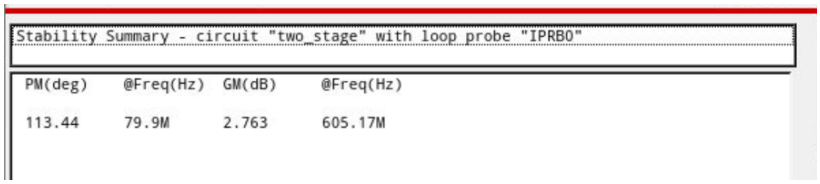
Stability Simulation

After adding the compensation loop, the stability of the two-stage OTA was analyzed. The compensation network ensures a sufficient phase margin by introducing a dominant pole, enabling reliable closed-loop operation. The following simulation illustrates the stability improvements achieved:

The results show that the amplifier attains a low-frequency gain of **61.8 dB**, a gain-bandwidth product of **121.24 MHz**, and demonstrates the anticipated change in the phase response to give us a more stable OTA:



Performing stability measurements will provide the following stability parameters:



And our amplifier is stable enough.

Summery

Parameter	Required Value	Design Achieved Value	Physical
Minimum small signal Gain - A_0	60	61.8	dB
Minimum GBW	100	121.24	MHz
Phase Margin	>45	113.44	$Degrees$
Power Dissipation	Keep as low as possible	6.063	mW