Emad Mazzawi
314744996

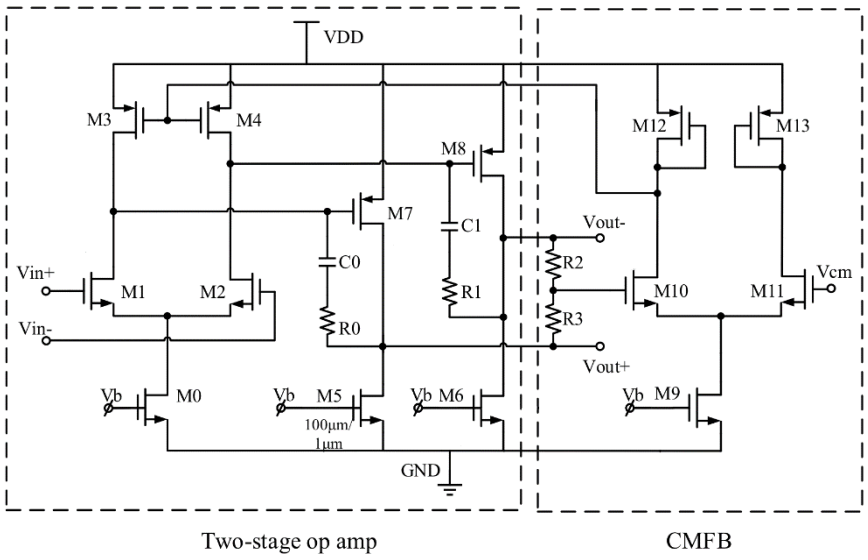
Bakaa Nijm
315925560

Design Exercise 4
Fully differential amplifier design

In this project, we present a fully differential two-stage operational amplifier with a common-mode feedback (CMFB) circuit to stabilize the output common-mode voltage, which satisfies the required SPEC:

Parameter	Value	Physical Units
Single positive supply (VDD)	1.8	Volts
Closed Loop Gain	3	
Dynamic Range at Output, DR	>80	dB
Settling Error	<0.5	mV
Settling Time, Ts	<50	ns
Load Capacitance	10	pF
Phase Margin	>60	Degrees
Power Dissipation	Keep as low as possible	Watts

The design in this project is based on the given schematic:



- Stage 1: Differential Input Pair

Transistors M1 and M2 form an NMOS differential pair with M0 Acting as a current source, setting the tail current for the differential pair. In addition to PMOS devices M3 and M4 that act as active loads/current mirrors for that NMOS differential input.

Thus, the first stage is a conventional NMOS diff-pair loaded by a PMOS current mirror.

- Stage 2: Gain Stage

Transistors M5, M6, M7 and M8 form the “second stage” that provides additional voltage gain and drives the fully differential outputs Vout+ and Vout−.

M5 and M6 provide bias current for the second stage, and M7 and M8 act as active devices to swing the output nodes.

The compensation elements (C0,R0) and (C1,R1) are there to stabilize the two-stage loop, these networks help ensure the amplifier remains stable across its range of operating frequencies.

- Common-Mode Feedback (CMFB) Circuit

Because this is a fully differential amplifier, we need to control the *average* output voltage (common-mode) independently of the differential swing.

The devices M10, M11 sense the average output voltage through the resistor-divider and compare it with the desired common-mode reference Vcm.

The outputs of that sensing pair are fed back into M12 and M13, which steer current so that the output nodes’ average voltage is driven to Vcm. Essentially, the CMFB Prevents unwanted drift in the differential outputs.

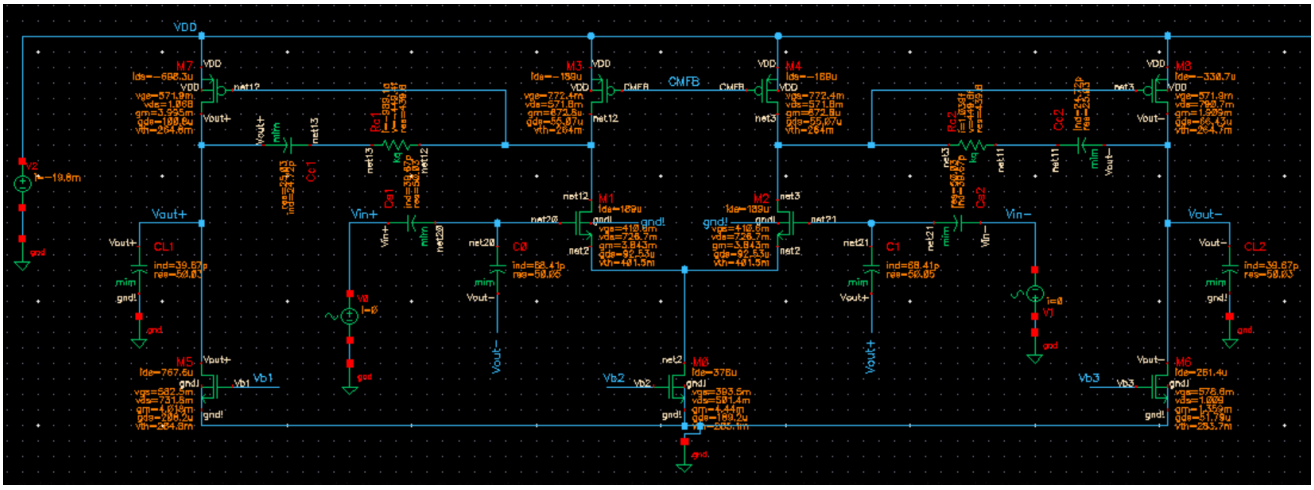
To achieve these parameters, we have chosen to use the Miller CMOS OTA that was originally designed in our third project. However, this time, it is implemented as a fully differential amplifier instead of a single-ended one.

The Common-Mode Feedback (CMFB) circuit is resistor-based, as discussed in our lectures. This topology is advantageous in handling a low supply voltage (VDD) since it consists of only three transistors between VDD and GND, ensuring they operate in the correct OP.

To achieve the required performance, we employed four different bias sub-circuits to establish the appropriate DC voltages, ensuring that the transistors function in the correct region while minimizing noise.

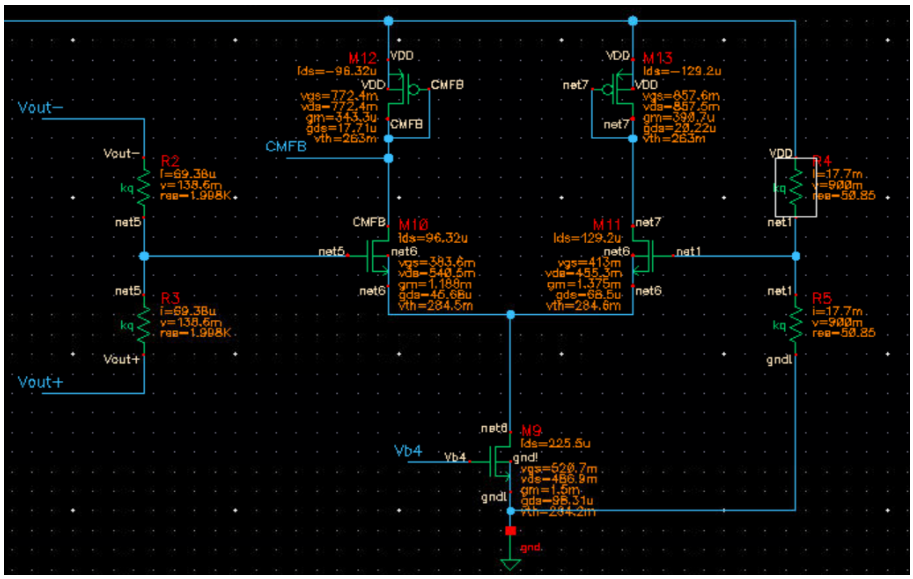
Circuit Schematic and Device Dimensions tables (including operation point)

Amplifier



	W[um]	L[um]	V_{GS}[v]	V_{DS}[v]	G_m	G_{ds}
M0	35	0.5	393.5m	501.4m	4.44m	189.2u
M1	45	0.2	410.6m	726.7m	3.843m	92.53u
M2	45	0.2	410.6m	726.7m	3.843m	92.53u
M3	10	0.5	772.4m	571.8m	672.8u	55.07u
M4	10	0.5	772.4m	571.8m	672.8u	55.07u
M5	15	0.5	582.5m	731.8m	4.018m	208.2u
M6	5	0.5	578.6m	1.009	1.359m	51.79u
M7	80	0.5	571.9m	1.068	3.995m	100.8u
M8	40	0.5	571.9m	790.7m	1.909m	66.43u
R0	440 ohm					
R1	440 ohm					
C0	5p F					
C6	5p F					

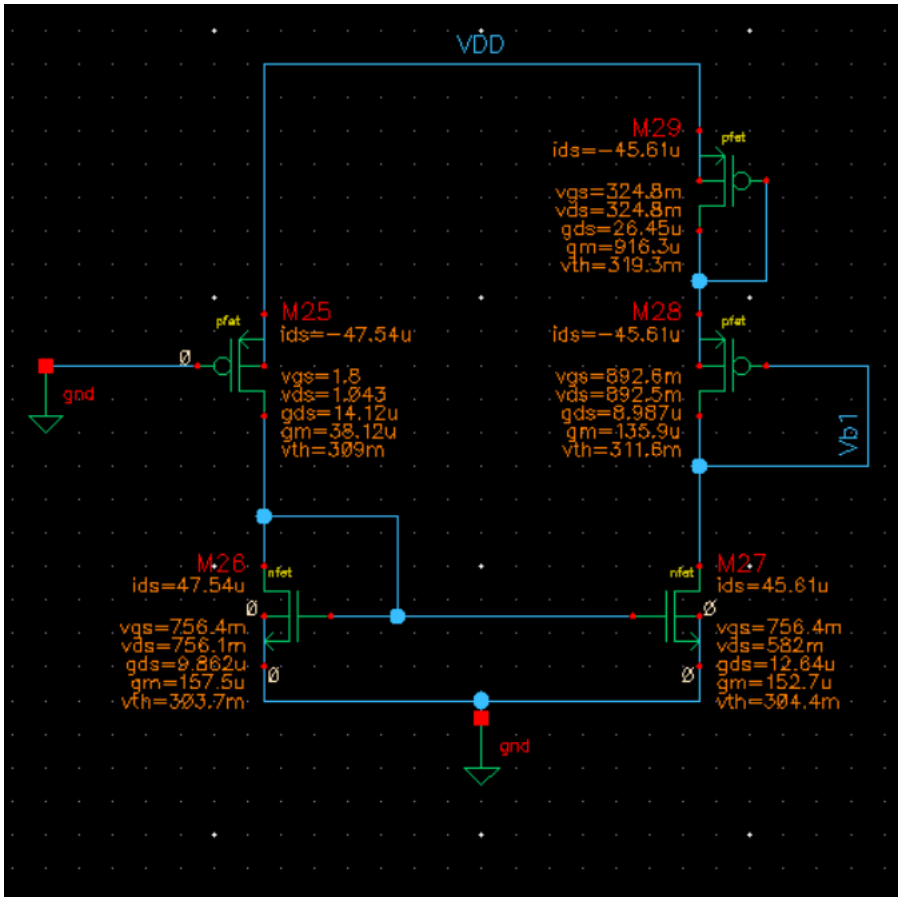
CMFB



	W[um]	L[um]	VGS[v]	VDS[v]	Gm	Gds
M12	5	0.5	772.4m	77.24m	343.3u	17.71u
M13	5	0.5	857.6m	857.5m	390.7u	20.22u
M10	10	0.5	383.6m	540.5m	1.188m	46.66u
M11	10	0.5	413m	455.3m	1.375m	68.5u
M9	7	0.5	520.7m	486.9m	1.5m	98.31u
R2	2 Kohm					
R3	2 Kohm					
R4	58 ohm					
R5	58 ohm					

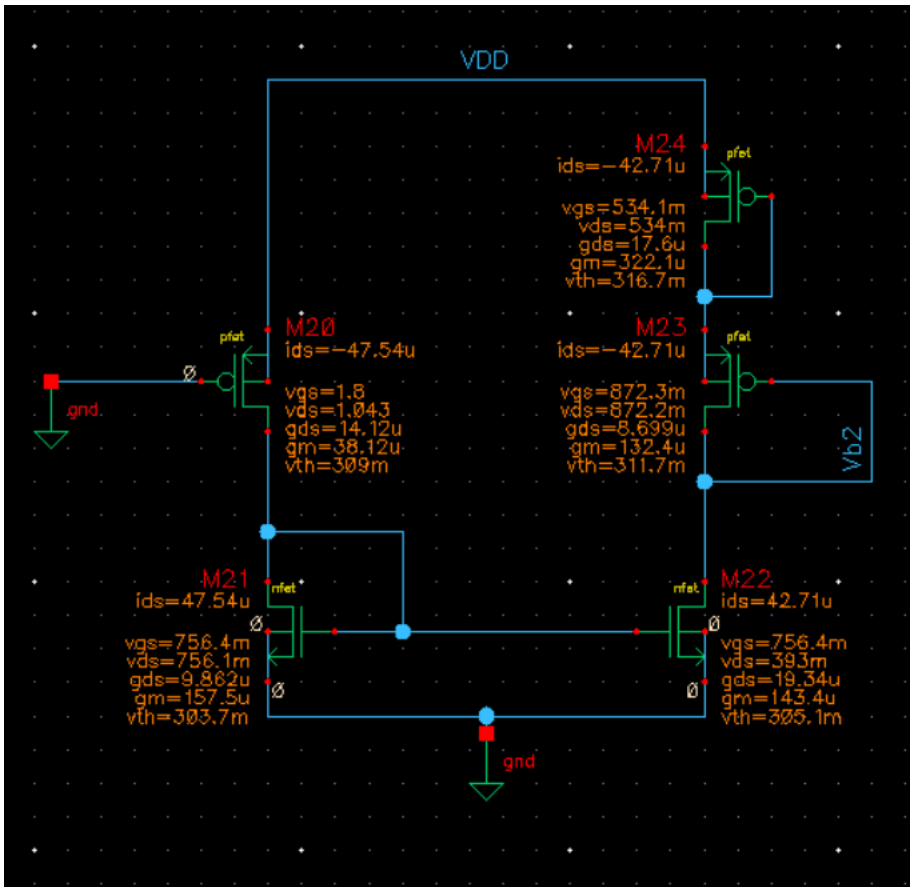
Bais circuits

Vb1



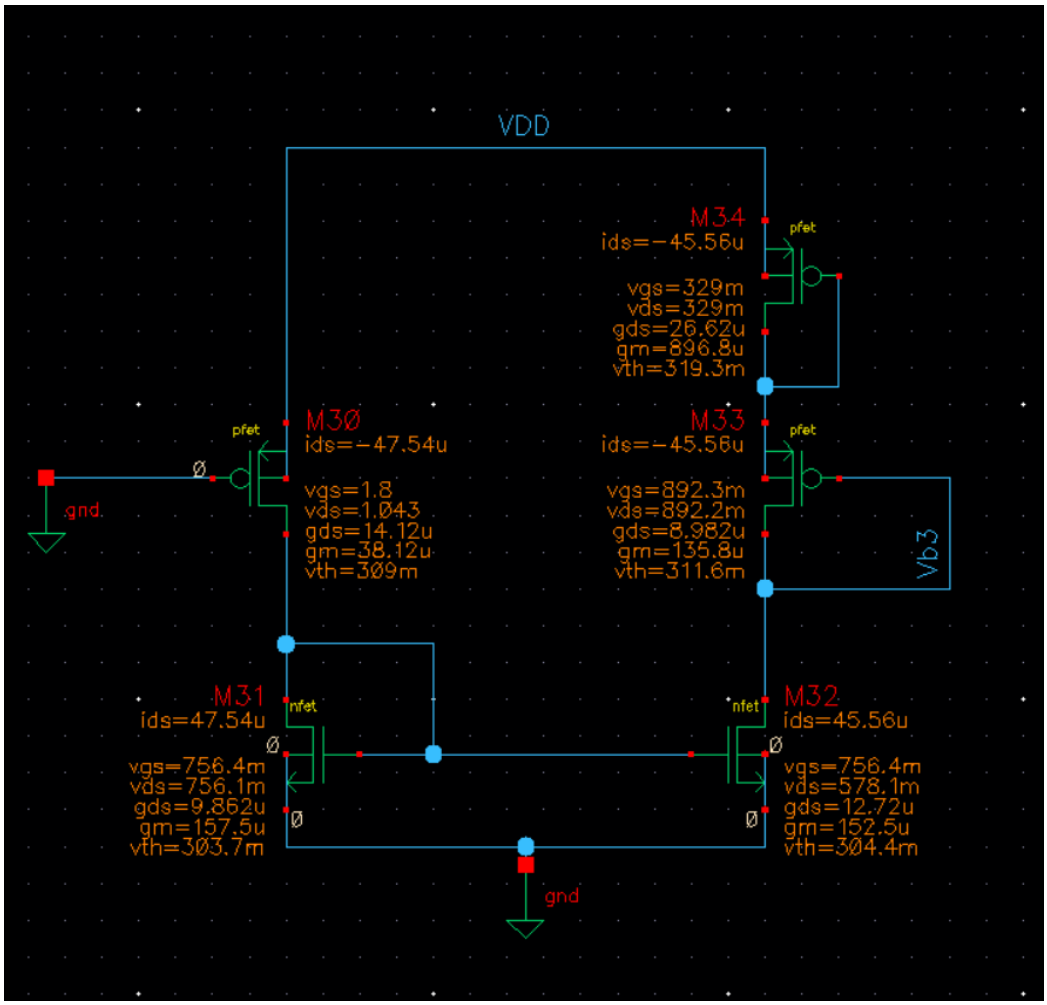
	W[um]	L[um]	VGS[v]	VDS[v]	Gm	Gds
M25	0.2	0.2	1.8	1.043	38.12u	14.12u
M26	0.3	0.2	756.4m	756.1m	157.5u	9.862u
M27	0.3	0.2	756.4m	582m	152.7u	12.62u
M28	0.8	0.2	892.6m	892.5m	135.9u	8.987u
M29	60	0.2	324.8m	324.8m	916.3u	26.45u

Vb2



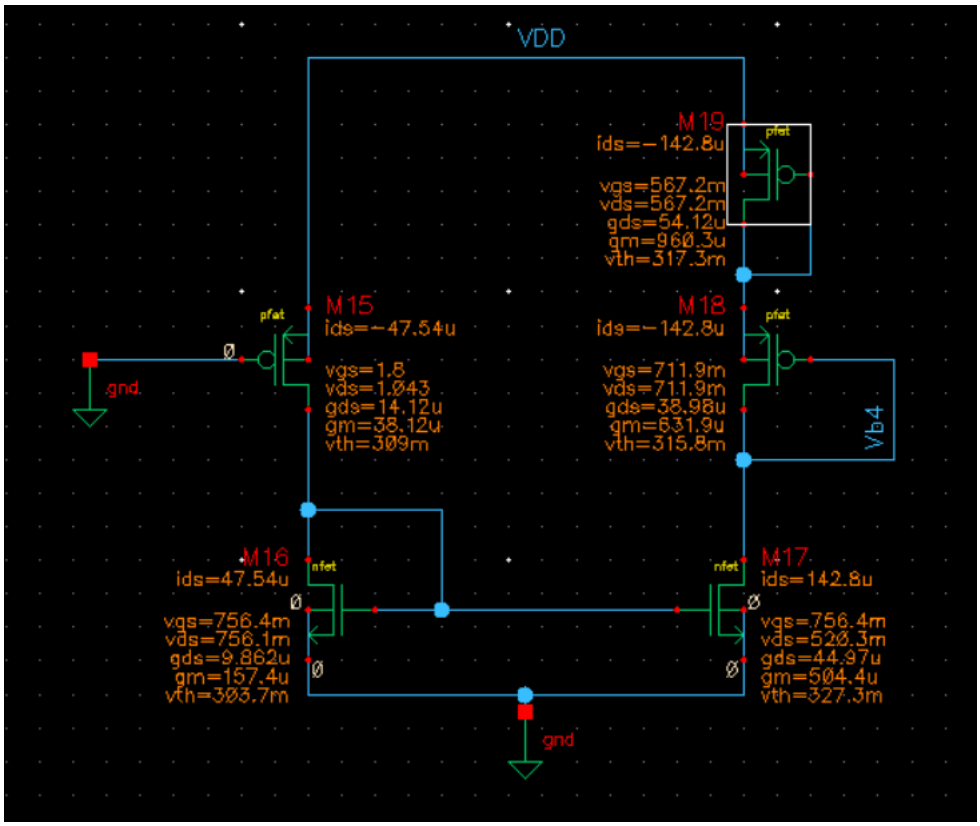
	W[um]	L[um]	VGS[v]	VDS[v]	Gm	Gds
M20	0.2	0.2	1.8	1.043	38.12u	14.12u
M21	0.3	0.2	756.4m	756.1m	157.5u	9.862u
M22	0.3	0.2	756.4m	393m	143.4u	19.34u
M23	0.8	0.2	872.3m	872.2m	132.4u	8.699u
M24	4	0.2	534.1m	534m	322.1u	17.6u

Vb3



	W[um]	L[um]	VGS[v]	VDS[v]	Gm	Gds
M30	0.2	0.2	1.8	1.043	38.12u	14.12u
M31	0.3	0.2	756.4m	756.1m	157.5u	9.862u
M32	0.3	0.2	756.4m	578.1m	152.5u	12.72u
M33	0.8	0.2	892.3m	892.2m	135.8u	8.982u
M34	55	0.2	329m	329m	896.8u	26.62u

Vb4

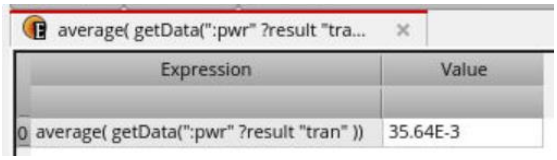


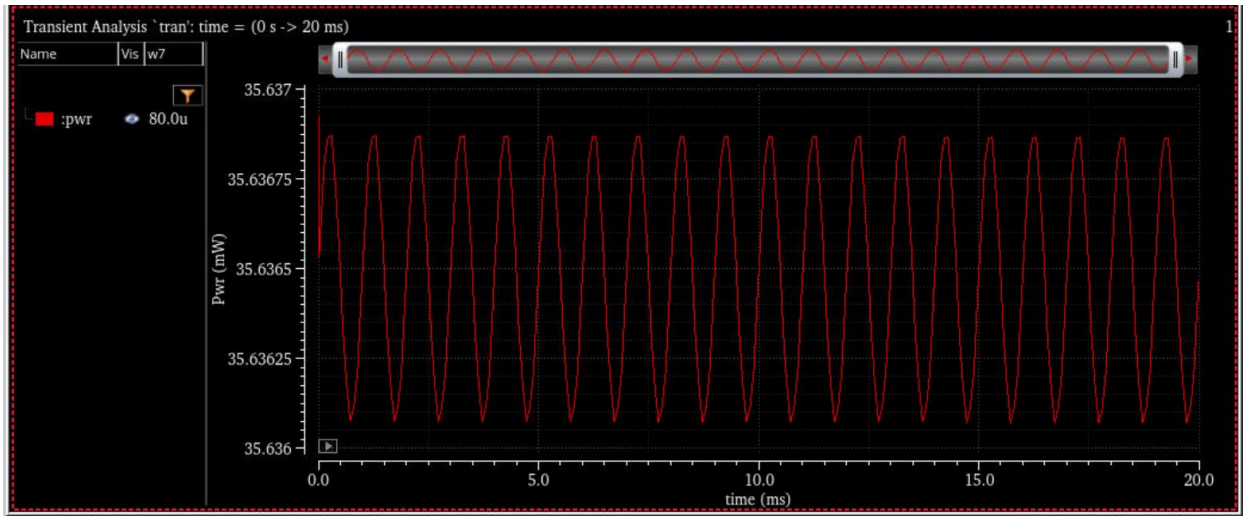
	W[um]	L[um]	VGS[v]	VDS[v]	Gm	Gds
M15	0.2	0.2	1.8	1.043	38.12u	14.12u
M16	0.3	0.2	756.4m	756.1m	157.4u	9.862u
M17	1	0.2	756.4m	520m	504.4u	44.97u
M18	4.5	0.2	711.9m	711.9m	631.9u	38.98u
M19	10	0.2	567.2m	567.2m	960.3u	54.12u

DC Power Consumption

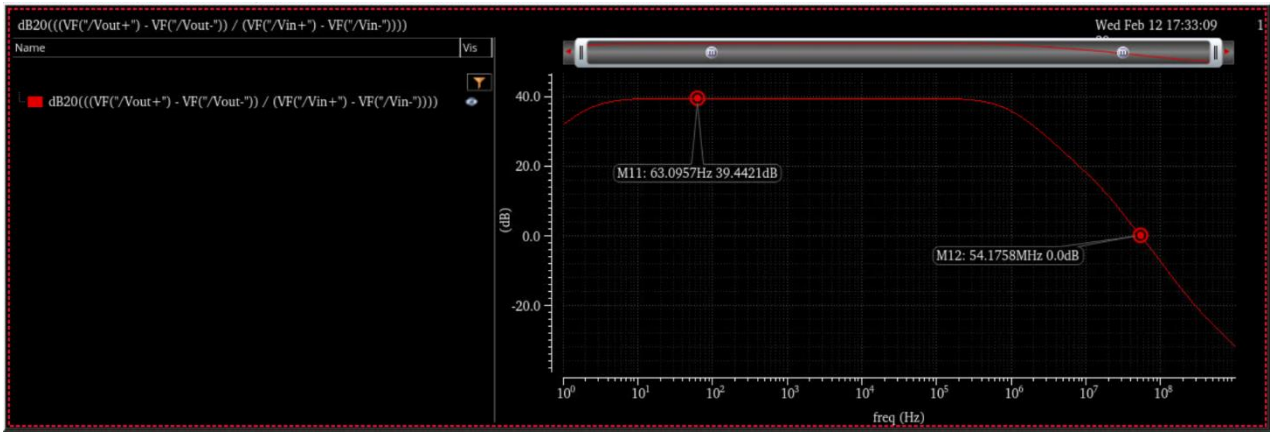
The total DC power consumption of the circuit is determined by the current drawn from the power supply and its respective voltage.

$$P_{total} = V_{DD} \cdot I_{DD}$$





Open loop AC: Gain and GBW



The results show that the amplifier attains a low-frequency gain of **39.44 dB**, a gain-bandwidth product of **54.175 MHz**

Important note : later in the "Stability Simulation" we managed to get the correct form for the gain plot (proper low-pass filter).

Open loop AC: CMRR

The ratio of the differential gain A_{diff} to the common-mode gain A_{cm}:

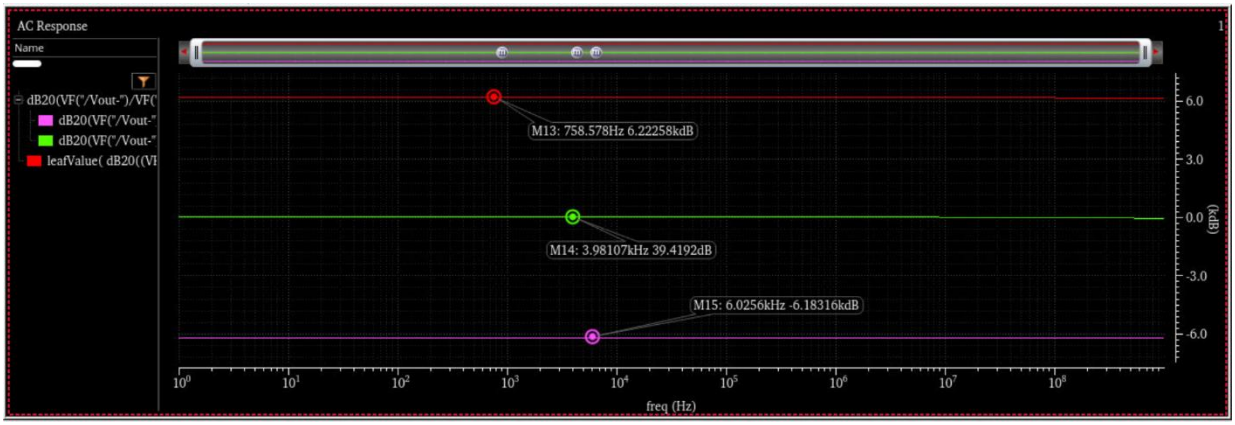
$$CMRR = \frac{A_{diff}}{A_{cm}}$$

Often, we express it in decibels (dB) as:

$$CMRR_{dB} = 20log_{10}(CMRR) = 20log_{10}\left(\frac{A_{diff}}{A_{cm}}\right) = 20log_{10}(A_{diff}) - 20log_{10}(A_{cm})$$

The calculated CMRR from the simulation was **6.2 KdB**.

Green - A_{diff} Pink - A_{cm} Red - CMRR

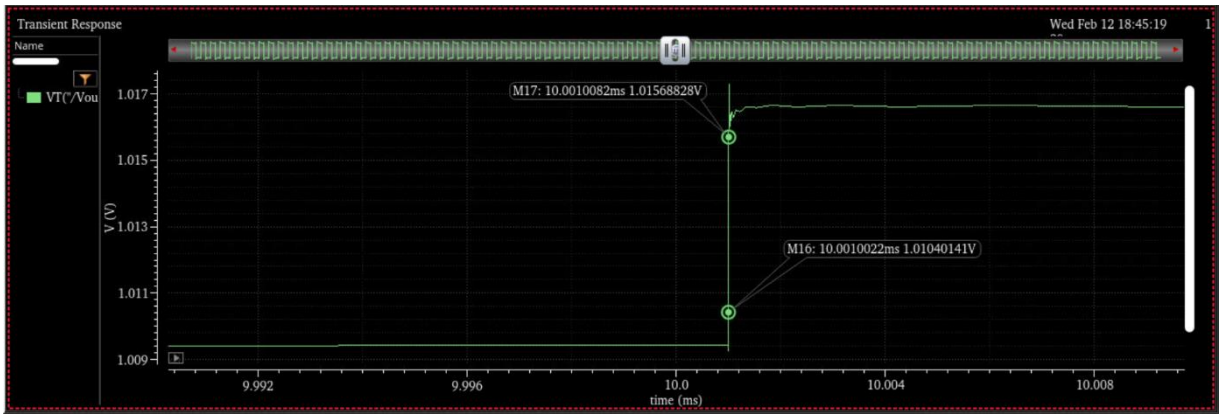


Open loop AC: Slew Rate

To evaluate the slew rate of the amplifier, a transient simulation was performed using an pulse source as the input signal.

The slope of the steepest part of the output voltage was calculated to determine the slew rate:

$$Slew\ Rate = \frac{\Delta V_{out}}{\Delta t} = \frac{1.01568V - 1.0104V}{10.0010082ms - 10.0010022ms} = 0.88\ \left[\frac{V}{\mu s}\right]$$



Noise Simulation

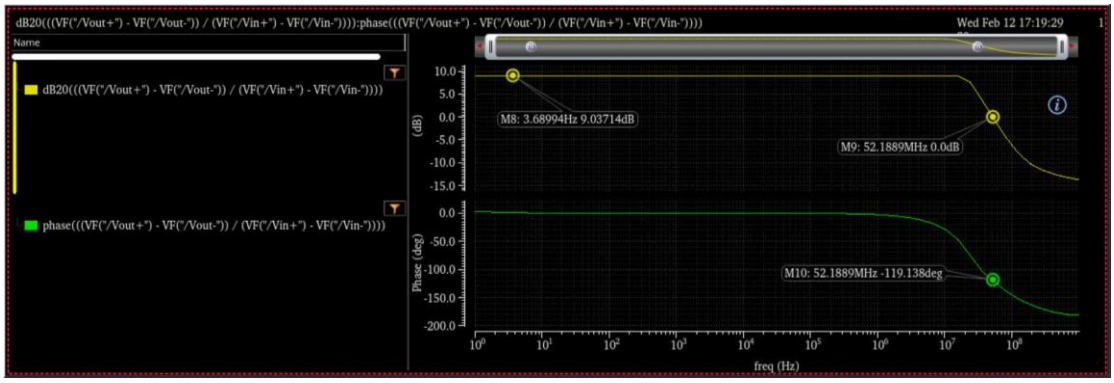
```
Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 1.12667e-06
Total Input Referred Noise = 7.0172e-07
The above noise summary info is for noise data
```

$$DR = 10\ log\left(\frac{P_{peak}}{P_{noise}}\right) = 10\ log\left(\frac{P_{peak}}{1.12e-07}\right)$$

Stability simulation: Closed loop bode

We added a compensation loop to improve the stability of the two-stage fully-differential amp. The following simulation shows the stability improvements achieved:

The results show that the amplifier attains a low-frequency gain of **9.03 dB**, a gain-bandwidth product of **52.188 MHz**, and demonstrates the anticipated change in the phase response to give us a more stable amp:



Stability simulation: PM and GM for closed loop

Phase margin (PM):

phaseMargin(((VF("/Vout+") - VF("/V...

	Expression	Value
0	phaseMargin(((VF("/Vout+") - VF("/Vout-")) / (VF("/Vin+") - VF("/Vin-"))))	61.43

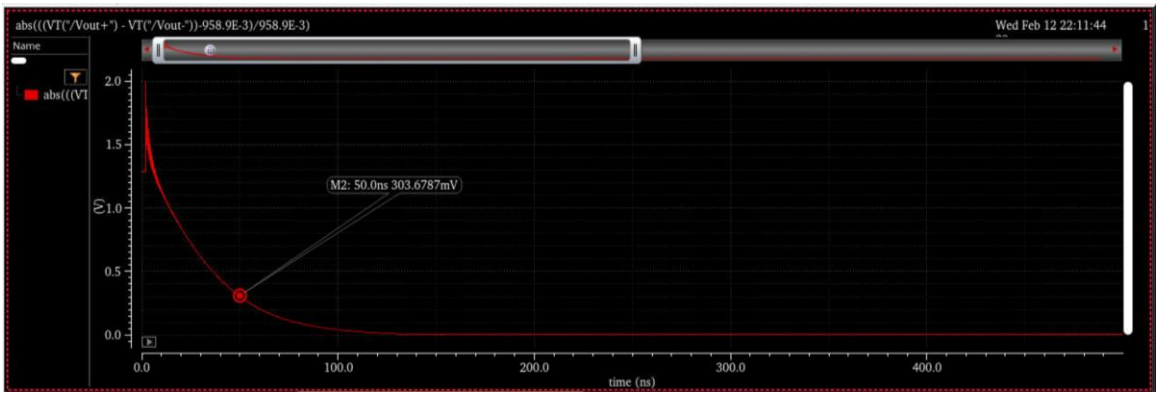
we got $PM > 60^{\circ}$ as requested.

Gain Margin (GM):

gainMargin(((VF("/Vout+") - VF("/Vou...

	Expression	Value
0	gainMargin(((VF("/Vout+") - VF("/Vout-")) / (VF("/Vin+") - VF("/Vin-"))))	-13.23

Settling error



settlingTime((VT("/Vout+") - VT("/Vo...

	time	settlingTime((VT("/Vout+") - VT("/Vout-")) 0 t 500n t 5 t "time")
	s	s
0	102.7E-9	203.9E-9

Maybe we based our simulation on incorrect calculations, leading to higher-than-usual values for the settling error and settling time. However, since the rest of the simulations seem to be working fine, this issue might be due to specific conditions or parameters that need to be adjusted.