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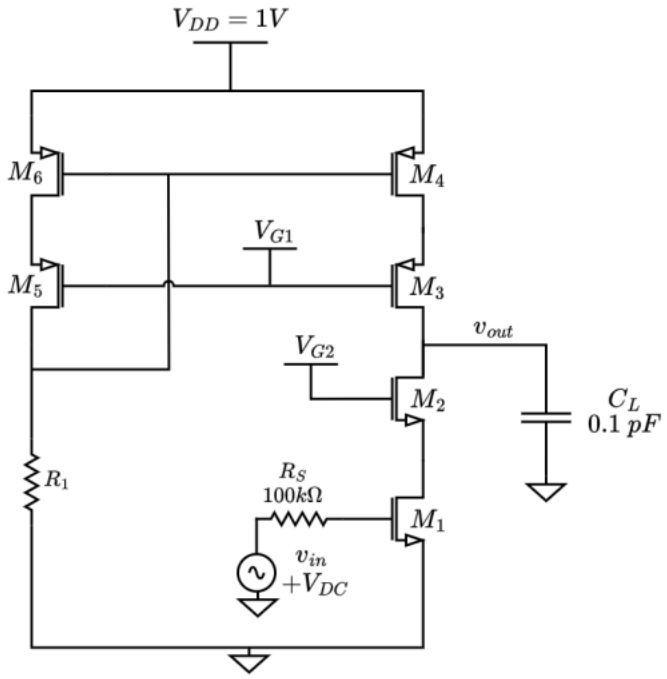
Design Exercise 2
Low Power Sensor Amplifier

This report details the design and simulation of a low-power sensor amplifier implemented using CMOS technology. The amplifier is optimized for low power consumption, making it suitable for sensor applications where energy efficiency is critical. The design was simulated using Cadence Virtuoso to validate its performance under specified conditions.

This project focuses on the design as illustrated in the provided schematic diagram:



The design specifications are:

	DC Gain	3-dB BW	Max Power consumption
Value	$40\ dB$	$2\ MHz$	$20\ \mu W$

The design of the sensor amplifier involves carefully selecting transistor sizes and passive component values to meet the desired performance specifications. This approach ensures the circuit functions within its intended performance range while keeping the transistors in their optimal operating states.

Design Consideration

Transistors M_1 and M_2 form a differential pair, with M_1 connected to the input signal. M_3 and M_4 act as current mirror, providing an active load for the differential pair. And finally, M_5 and M_6, together with R_1, form a current mirror that provides a constant current to the differential pair.

A small-signal analysis of transistors M_1 and M_2 provides general expressions for the gain and bandwidth of the circuit:

$$Gain = G_m \cdot R_{out} \approx g_{m1} \cdot g_{m2} \cdot r_{o1} \cdot r_{o2}$$

$$BW \approx \frac{1}{2\pi \cdot R_{out} \cdot C_L} \approx \frac{1}{2\pi \cdot g_{m2} \cdot r_{o1} \cdot r_{o2} \cdot C_L}$$

In our design, we chose to allocate one-third of the supply voltage (VDD) to transistors $M_1$and M_2. To ensure that both transistors operate in the saturation region, they must satisfy the following condition:

$$V_{GS} > V_{th} \quad , \quad V_{DS} > V_{GS} - V_{th}$$

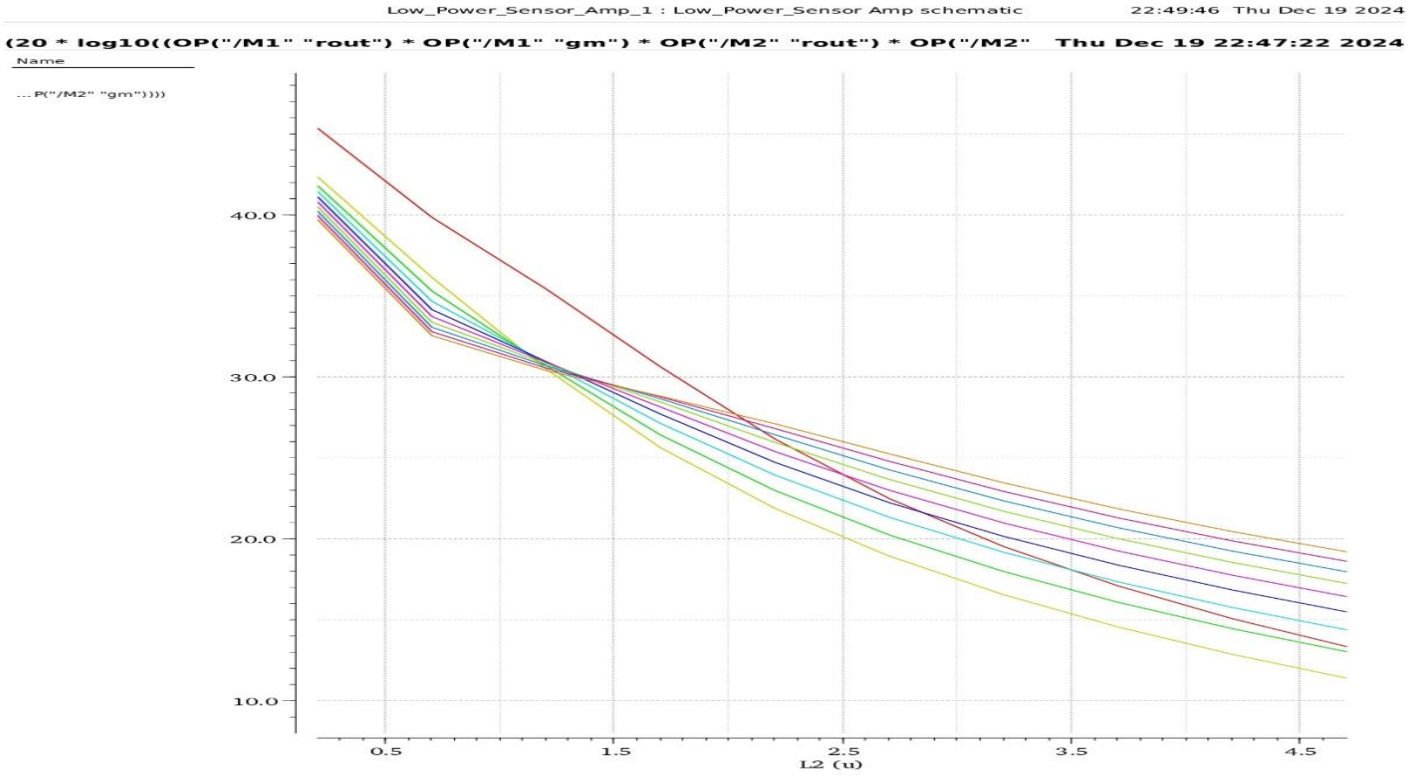
Thus, the following constraints must hold:

$$V_{th} < V_{DC} < 0.16 + V_{th} \quad , \quad 0.16 + V_{th} < V_{G2} < 0.33 + V_{th}$$

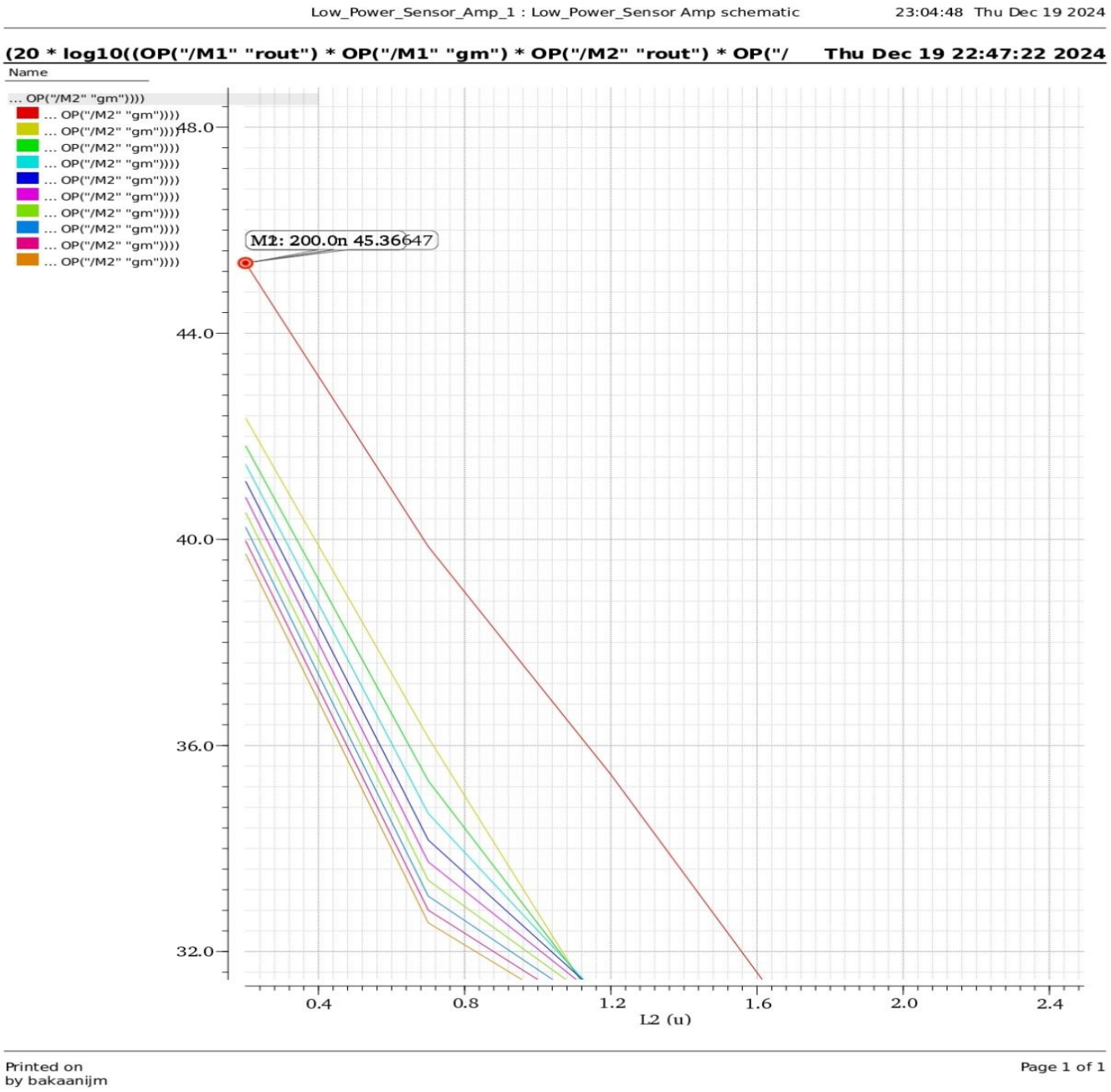
For the biasing point, we used: $V_{DC} = 400mV$ and $V_{G2} = 600mV$, which satisfy these conditions.

Next, we performed sweep on L_1, L_2, W_1 and W_2 to achieve the desired gain and bandwidth. Initially, a DC simulation was conducted to select values for L_1 and L_2 that provide a gain greater than 40dB. **This decision was made with the understanding that our amplifier not only includes these two transistors but also incorporates a current mirror, which reduces the overall output resistance and thus impacts the gain.**

The following shows the results of the DC simulation:



And a zoomed-in view is shown below:

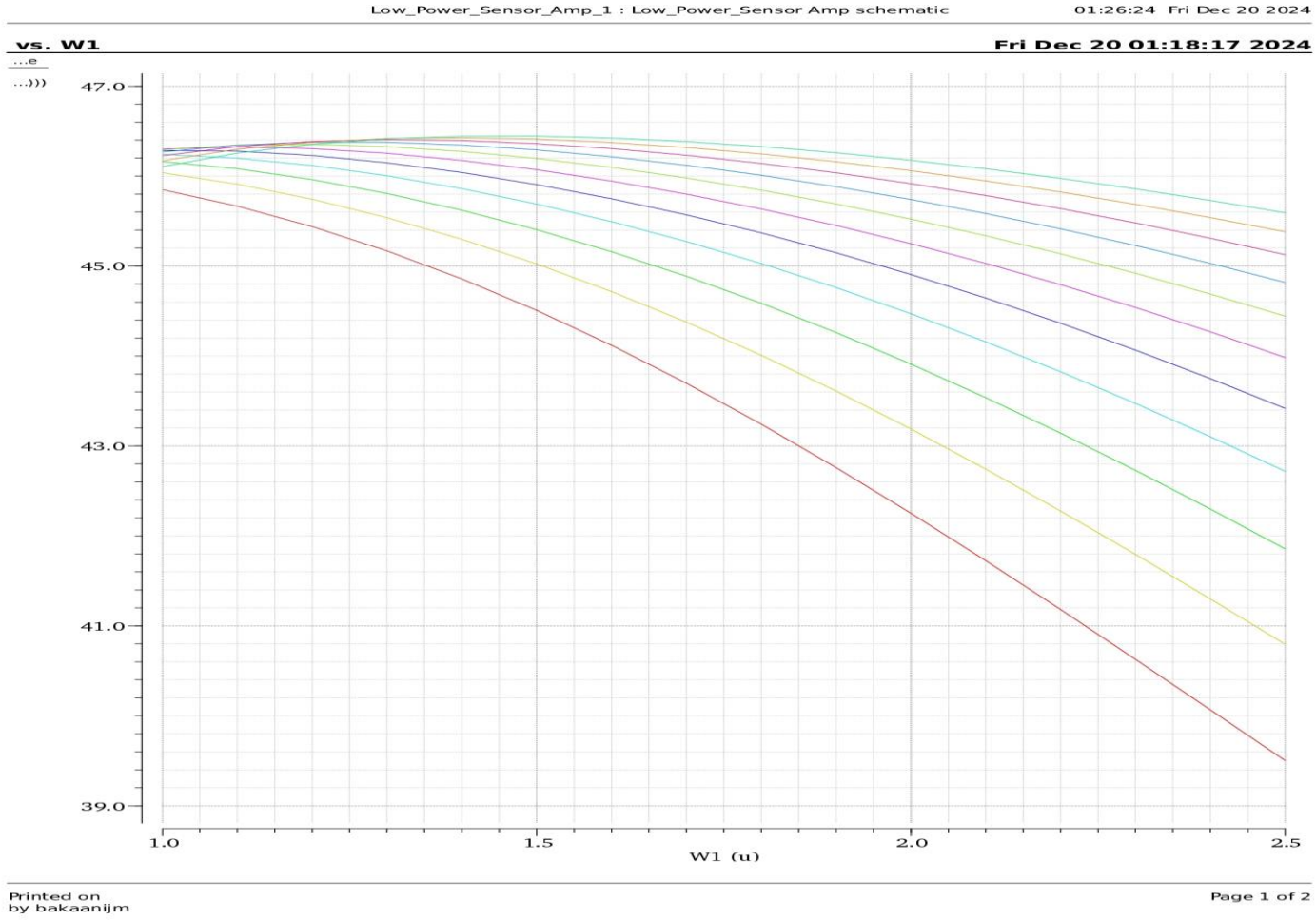


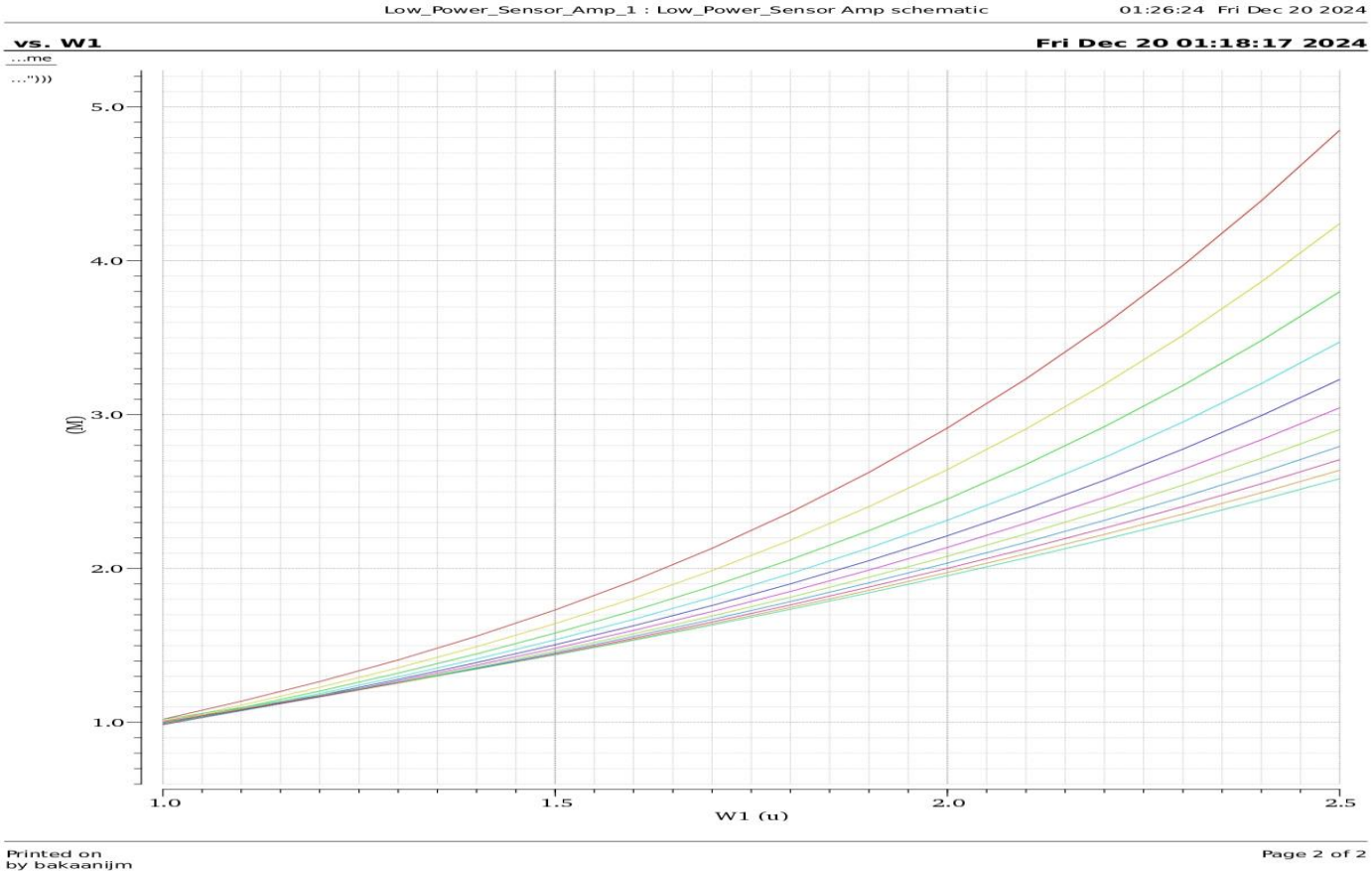
We chose $L_1 = 0.2\mu m$ and $L_2 = 0.2\mu m$, which resulted in a gain of 45.37dB.

By sweeping on the widths, **we aimed to achieve a slightly lower bandwidth, allowing the connection to the rest of the circuit to bring the bandwidth to the desired value by reducing the output resistance.** But to ensure both transistors at the saturation region we found that the most suitable widths would be $W_1 = 1.3\mu m$, $W_2 = 1\mu m$.

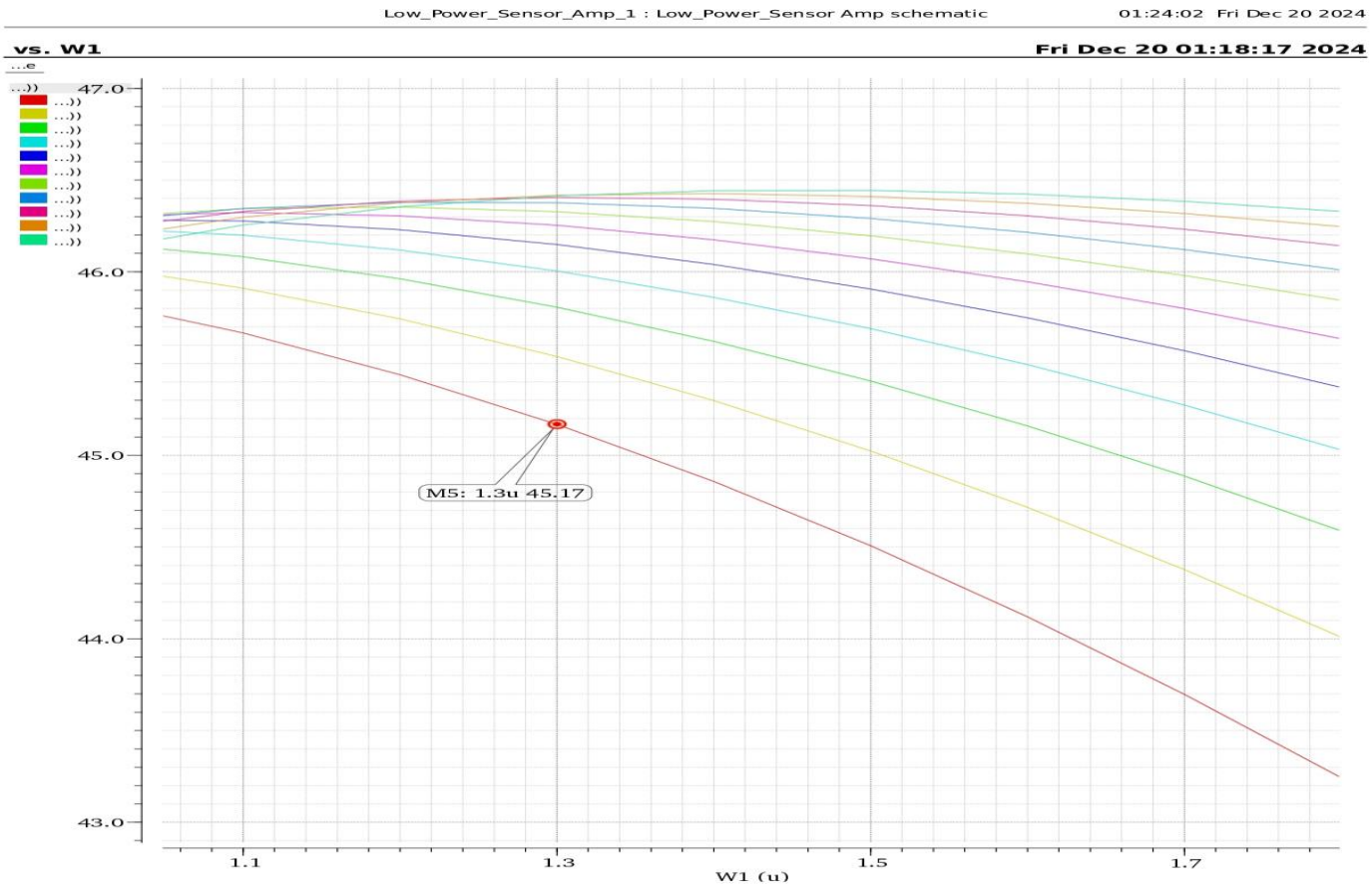
However, this choice resulted in a lower gain compared to the previous sweep on L, though the gain still exceeded 40dB, and the largest bandwidth achievable with these values was $1.406\ MHz$.

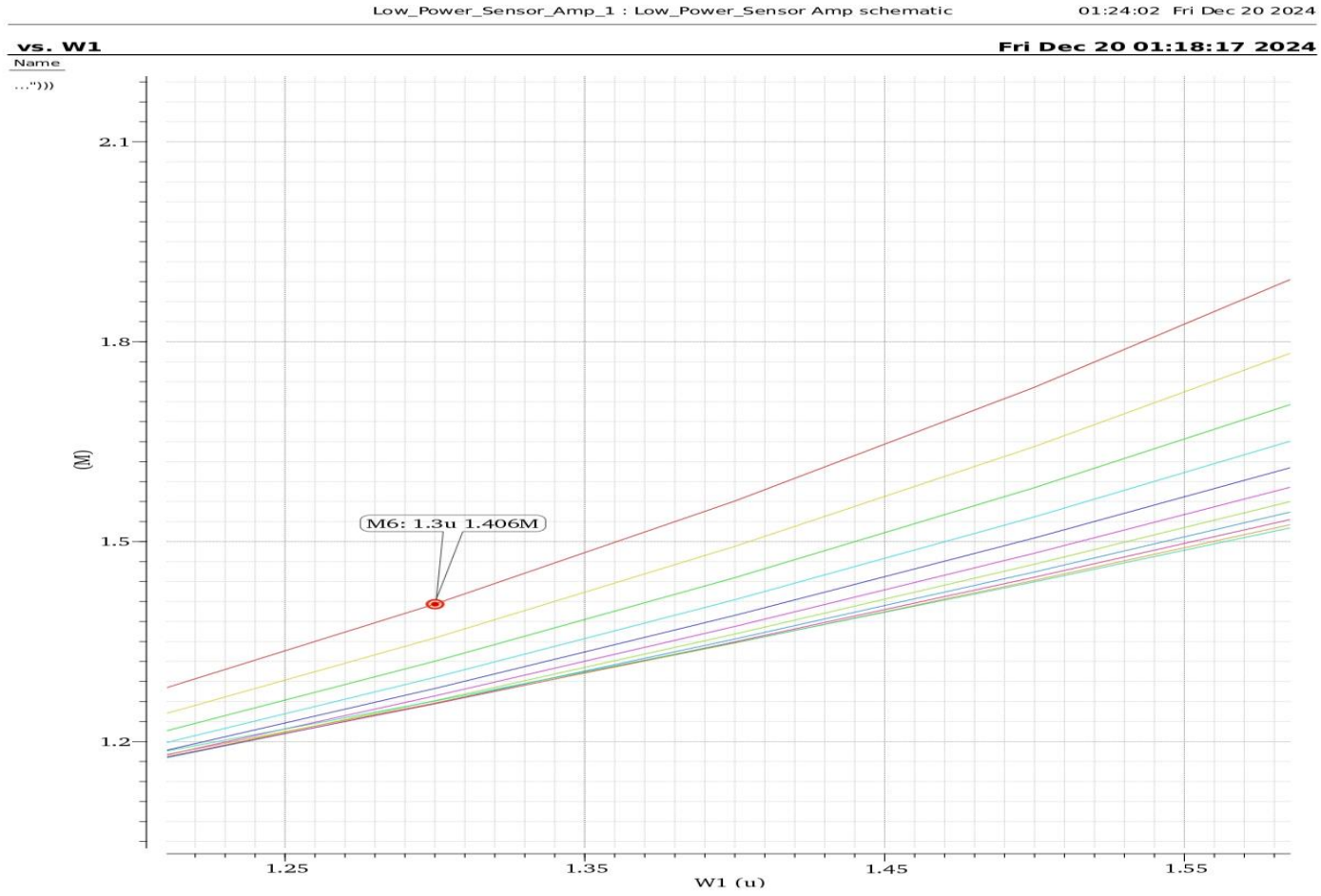
The DC sweep on W's:





a zoomed-in view:

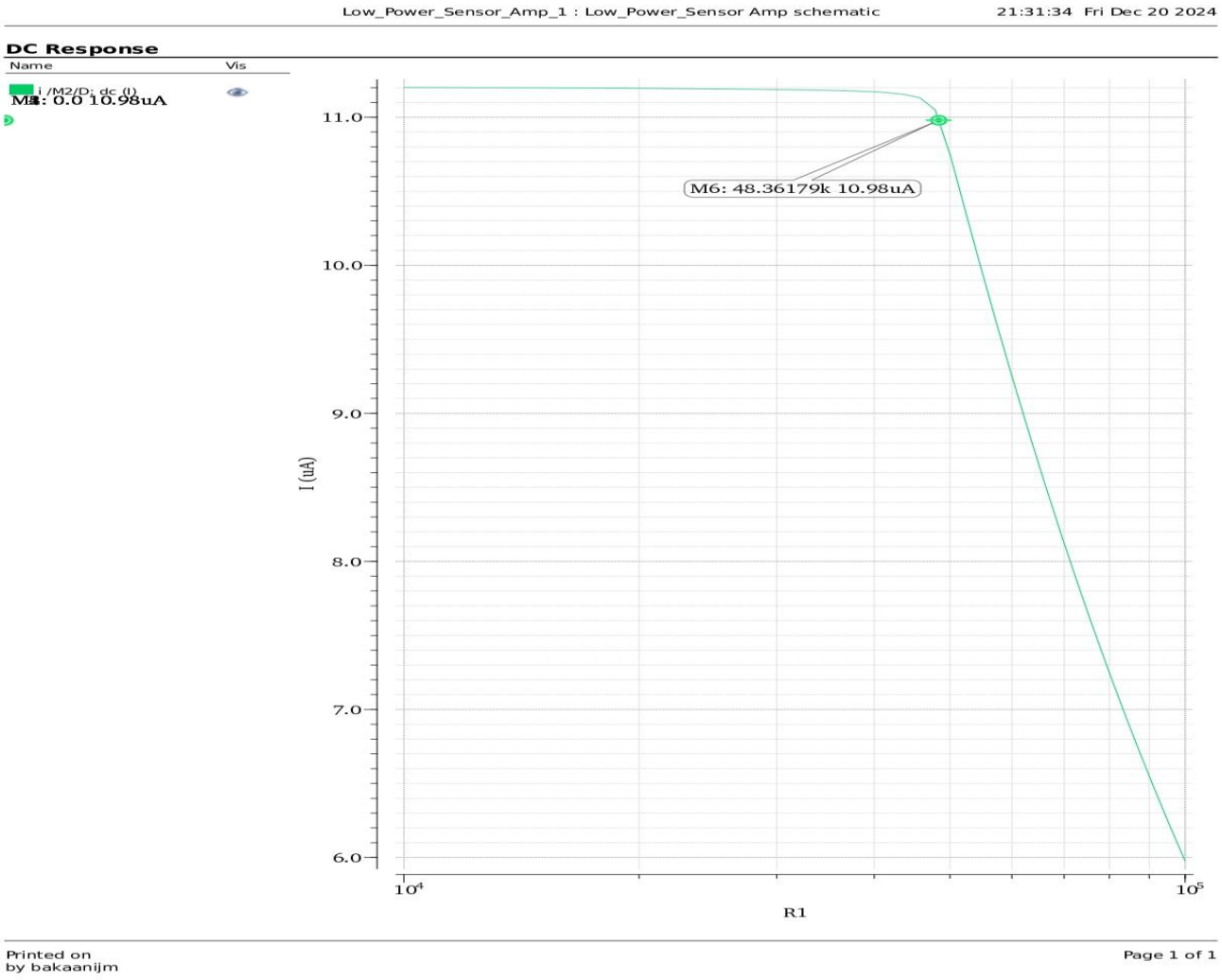




The remaining transistors in the circuit are PMOS, and their sizes were determined based on the general design rule that PMOS transistors are typically twice the size of NMOS transistors.

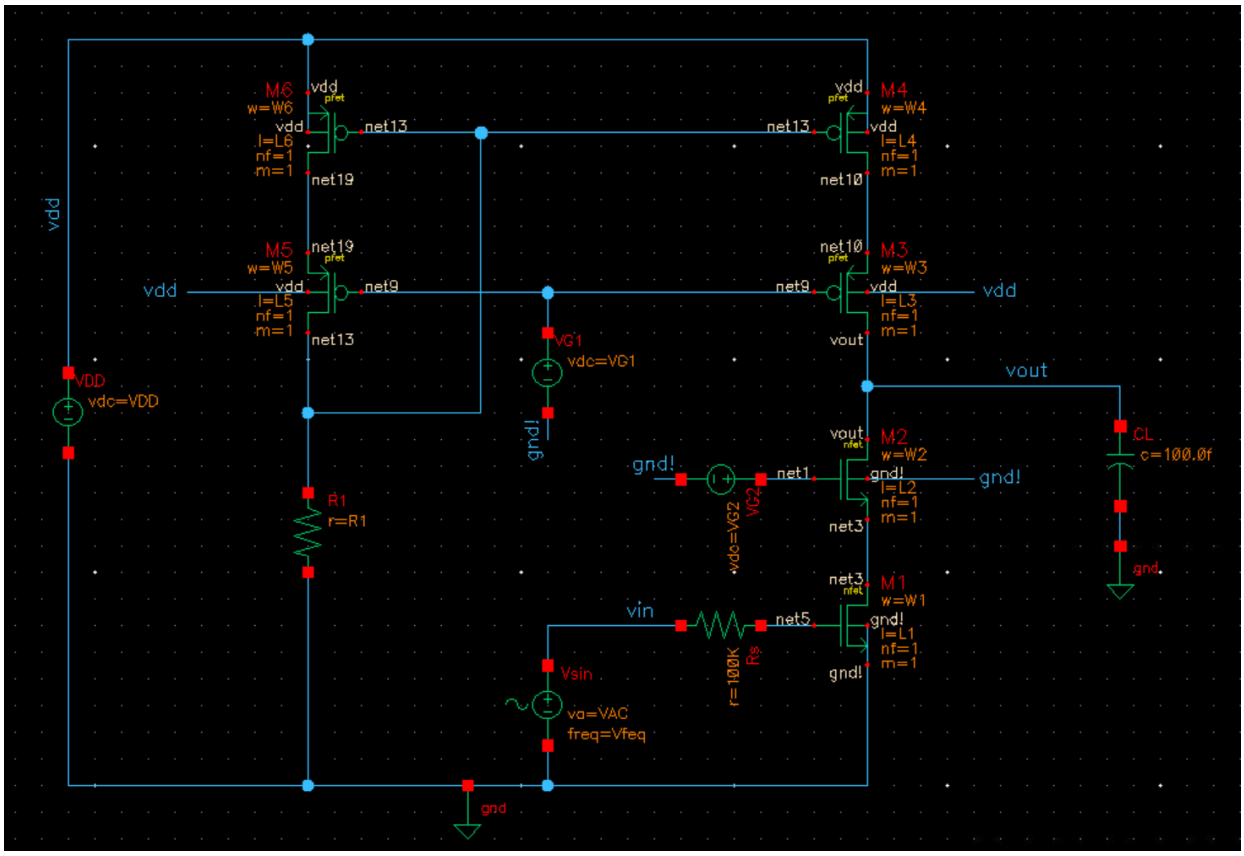
Finally, the resistor value was determined by sweeping over a specified interval to ensure that the DC current for M_1 and M_2 was maintained.

Based on the simulation results, $R_1 = 48.36179\ K\Omega$ was selected:



Important Note The values provided are initial estimates chosen based on the desired performance in the different sections of the circuit. Once the full circuit was connected, further tuning of these values was necessary to achieve the target specifications for gain, bandwidth, and power consumption.

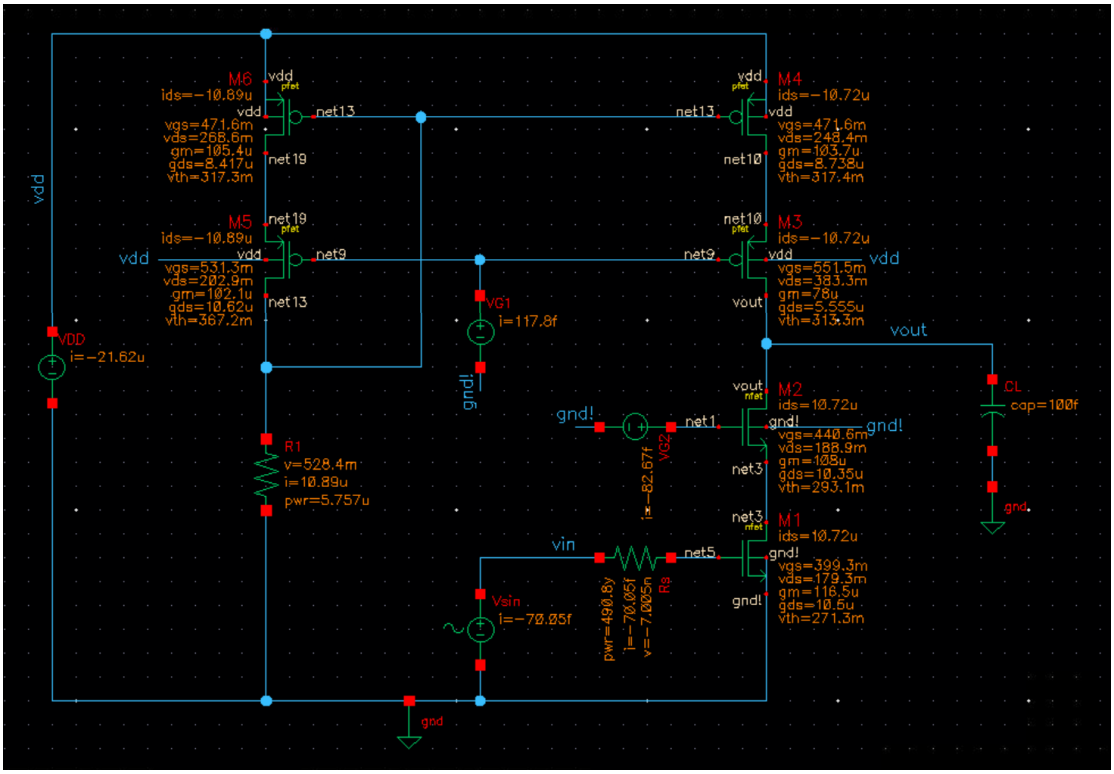
Circuit Schematic



Device Dimensions table

	Total width (μm)	Length (μm)	V_{GS} (V)	V_{DS} (V)	g_m (Ω^{-1})	g_{ds} (Ω^{-1})	Resistance (Ω)	Voltage (V)
M_1	1.3	0.6	399.3m	179.3m	116.5u	10.5u		
M_2	1.1	0.6	440.6m	188.9m	108u	10.35u		
M_3	2.1	0.4	551.5m	383.3m	76u	5.555u		
M_4	2.1	0.2	471.6m	248.4m	103.7m	8.738u		
M_5	2.1	0.2	531.3m	202.9m	102.1u	10.62u		
M_6	2.1	0.2	471.6m	268.6m	105.4u	8.417u		
R_1							48.5 k	
V_{DC}								0.3993
V_{G1}								0.2
V_{G2}								0.62

Circuit Operation Point



All the transistors are in saturation region.

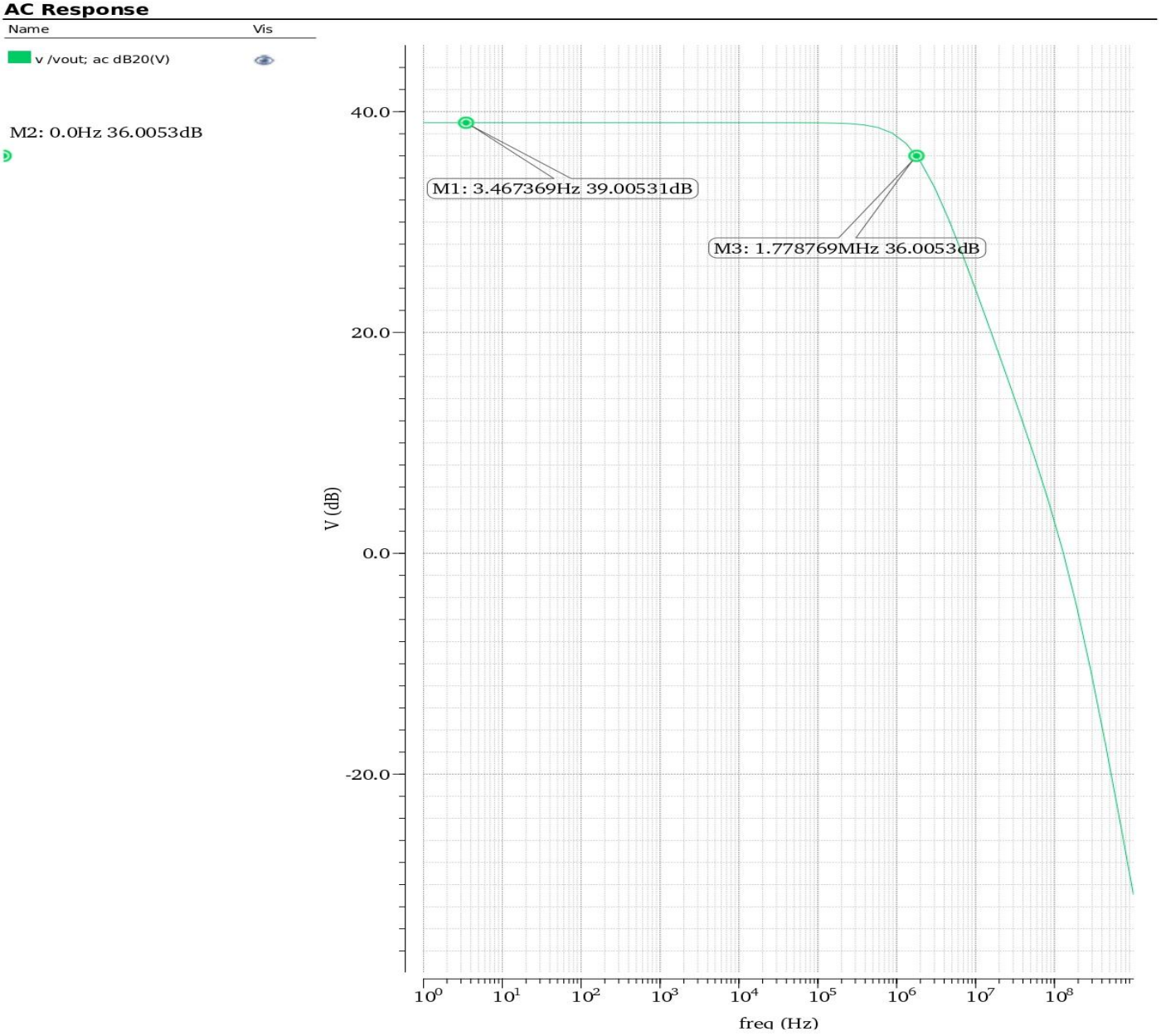
Gain Plot

To verify the performance of the designed amplifier, a gain simulation was conducted. This simulation aims to evaluate the amplifier's ability to achieve the desired gain under specified operating conditions.

When we simulated the entire circuit, as expected, the gain decreased, and the bandwidth increased. However, the changes were not as significant as anticipated, and the results did not align with the scale we had hoped for.

The results of this simulation provide insight into the frequency-dependent behavior of the circuit and validate the design choices made during the development process:

AC Response



The designed amplifier yielded a gain of approximately 39dB, which is slightly lower than the target of 40dB specified for this design. This result indicates a minor shortfall in achieving the intended value but still demonstrates acceptable performance. The lower gain can be attributed to the limitations in the fine-tuning of transistor dimensions and resistor values, which constrained the transconductance and output resistance of the circuit.

In addition, the achieved bandwidth was 1.7MHz, which is slightly lower than the target of 2MHz.

Despite efforts to further tune the circuit to achieve the exact target of 40dB and 2MHz bandwidth, the adjustments did not succeed in increasing the gain or bandwidth without negatively affecting other performance metrics, such as power efficiency. This outcome underscores the inherent trade-offs in the design process and the challenges of meeting all specifications simultaneously.

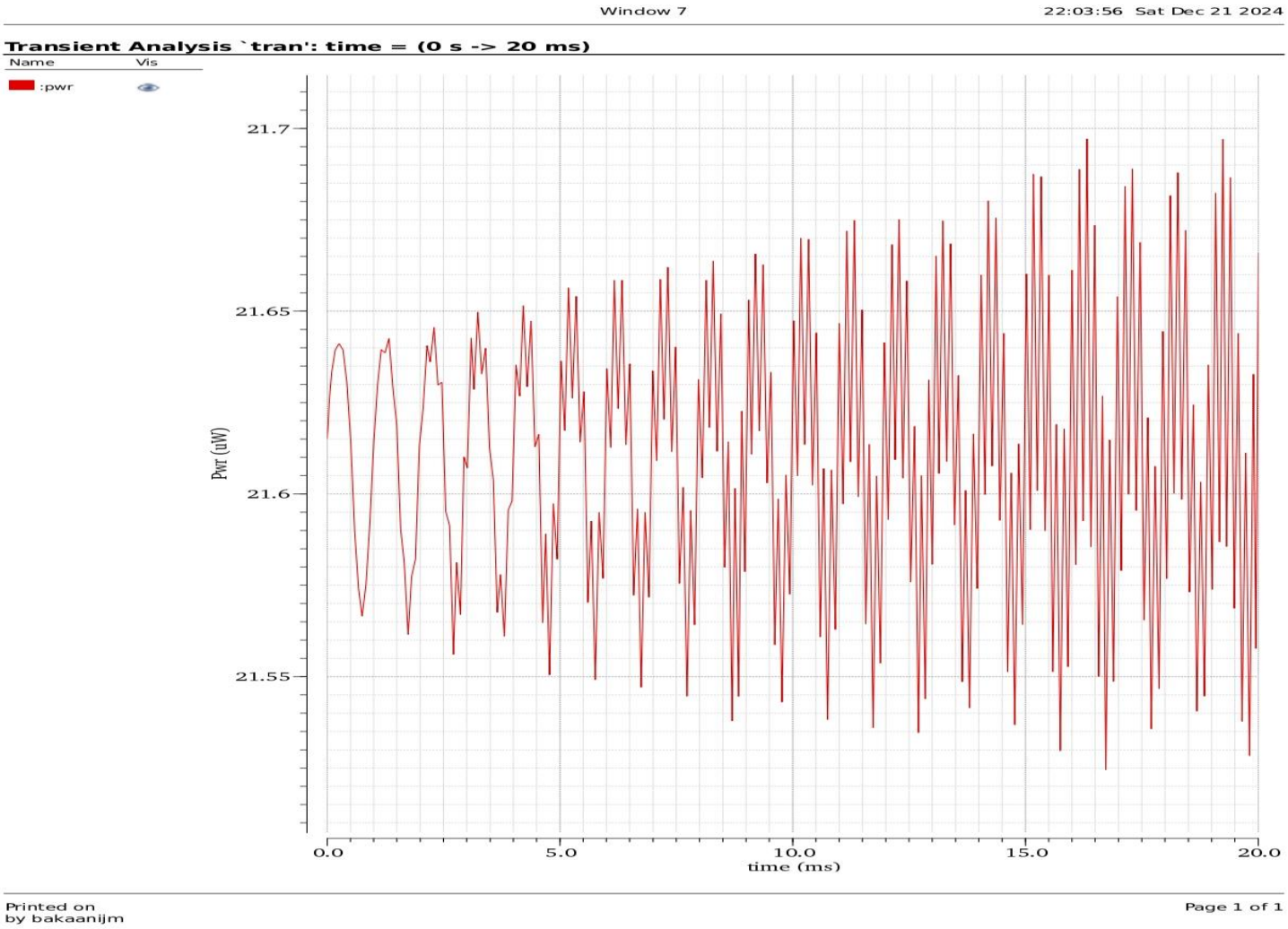
Power Consumption

The power consumption of the designed amplifier was carefully analyzed to ensure compliance with low-power design requirements. This evaluation highlights the energy efficiency of the circuit under the selected operating conditions and its impact on achieving the overall design objectives.

Here are the results of the power consumption simulation:

average(getData(":pwr" ?result "tra...

	Expression	Value
0	average(getData(":pwr" ?result "tran"))	21.61E-6



The target power consumption for the amplifier was set at $20\mu W$. However, the simulation results showed a power consumption of $21.61\mu W$. which is slightly higher than the target by approximately 10%. While this deviation is small, it still indicates that further optimization could be possible. The increase in power consumption is likely due to the need to achieve the desired gain and bandwidth, which inherently involves trade-offs in the design.

Despite this, the power consumption remains relatively low and could still be acceptable for most low-power applications.

Example of an output transient voltage

Given 1KHz input with an amplitude of 1mV.

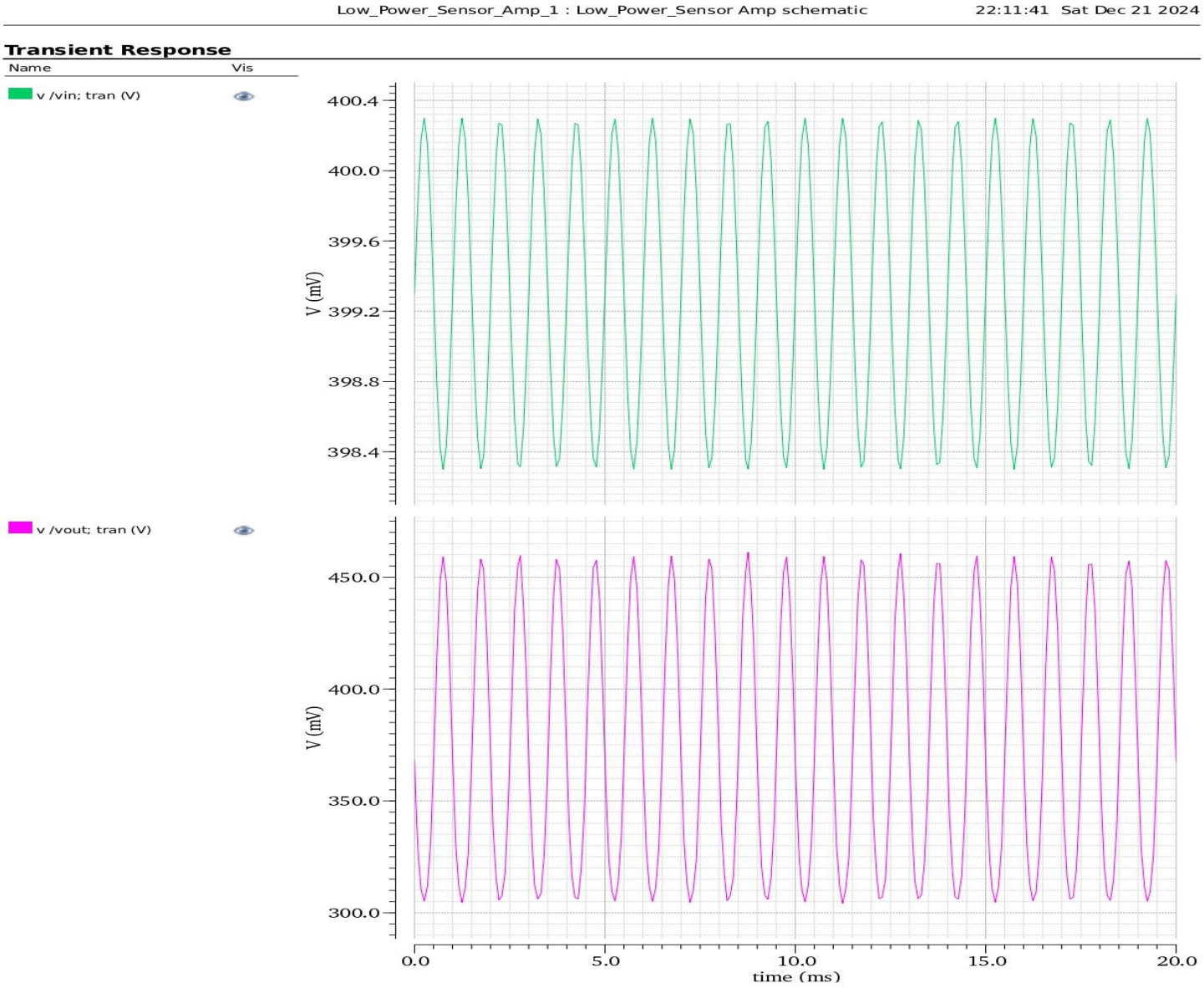
The following transient simulation shows the output response of the amplifier. This simulation illustrates the time-domain behavior of the circuit, allowing us to observe the amplifier's performance, including signal amplification. The input signal V_{in} and output signal V_{out} are plotted over the same time interval to verify the amplifier's functionality.

For a 1mV input signal with a 40dB gain, the AC signal will be amplified to 100mV. The DC level of 399.3mV will remain unchanged, as the amplifier is intended to amplify the AC signal while maintaining the DC bias.

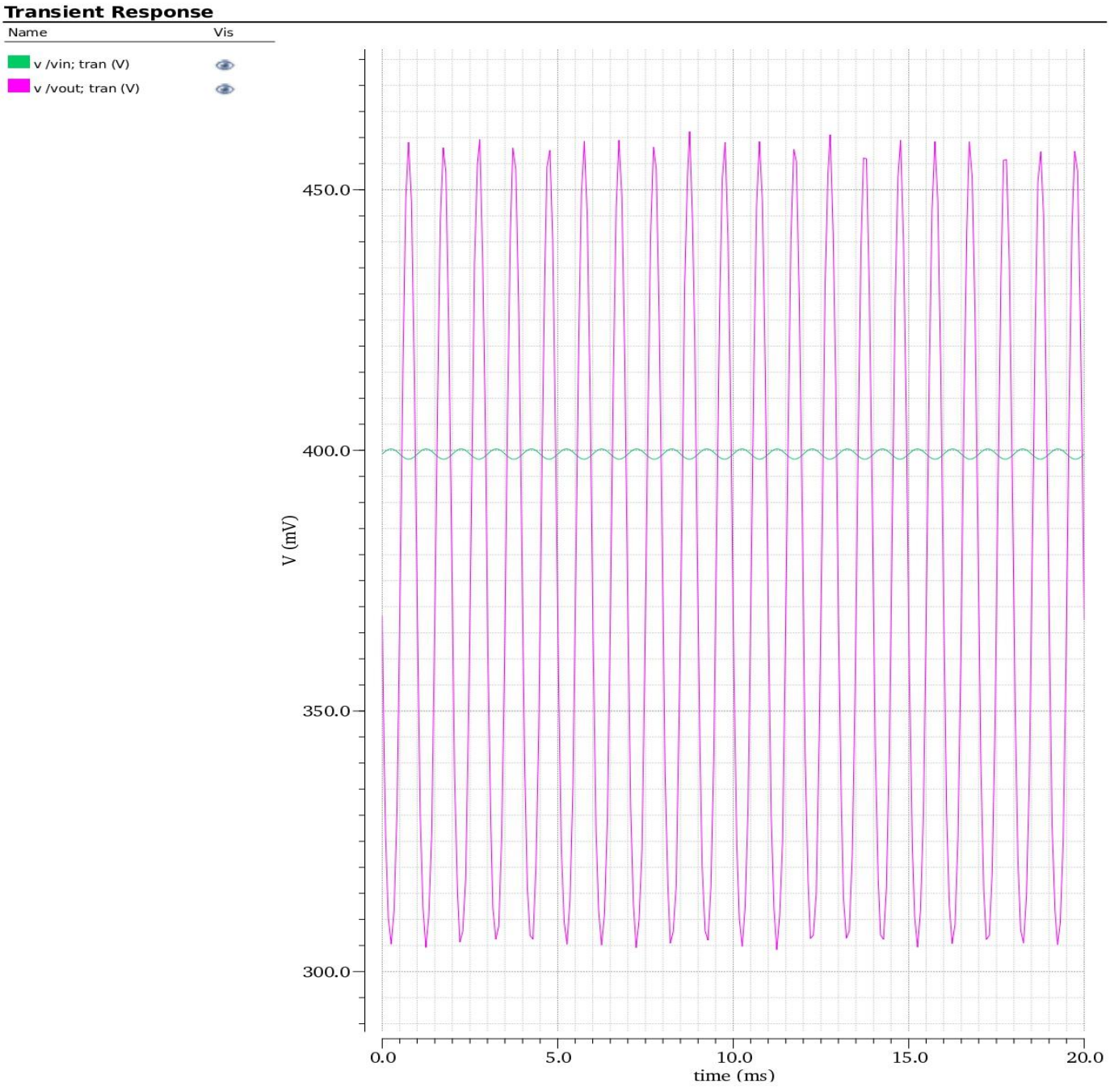
Therefore, the output signal will have a DC level of 399.3mV with an AC component of 100mV, making the total output signal:

$$Output\ voltage = 399.3\,mV + 100\,mV = 499.3\,mV$$

So, the output signal will have a total voltage of 499.3mV as we can see in the transient simulation below:



Here is the simulation showing both signals combined on the same axis:



Due to the gain being lower than 40 dB, the transient simulation produces an output below 499.3mV, though the decrease is not substantial.

The transient simulation results confirm that the amplifier operates as expected, successfully amplifying the input signal with minimal distortion. The output signal maintains the expected amplitude and frequency, demonstrating the circuit's effectiveness in time-domain operation.

Summery

	DC Gain	3-dB BW	Max Power consumption
Required Value	$40\ dB$	$2\ MHz$	$20\ \mu W$
Design Achieved Value	$39\ dB$	$1.77\ MHz$	$21.61\ \mu W$

While the gain is lower than the target, resulting in a slight reduction in signal amplification, the bandwidth is also slightly below the specified value.

These deviations are within reasonable limits, considering the trade-offs made during the design process. The lower gain may require compensation in subsequent stages of the system, while the reduced bandwidth could still align with the system's overall design, depending on the specific application.

Overall, the amplifier partially meets the primary design objectives, but there is room for further refinement to better align with specific application requirements.