Faculty of Engineering & Technology Electrical & Computer Engineering Department

Communications Lab - ENEE4103

Pre-Lab #6

Experiment NO. 6: Pulse Amplitude Modulation (Sampling)

Prepared by:

Eman Asfour 1200206

Instructor: Dr. Alhareth Zyoud

Teacher Assistant: Eng. Shadi Bannoura

Section: 4

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prelab 6	Exp 6 PAM			Grade	out of
5 block diagrams		pulse train	ok	3	3
		Natural sampling	ok		
		Flat top smpling	ok		
		Demodulation fo Nat and Flat	ok		
1	pulse train	pulse train (t and f)		1	1.5
	Natural sampling	s(t) (t and f)		1.5	2
		s(t) for f1 (t and f)			
		s(t) for f2 (t and f)			
		s(t) for %D1 (t and f)			
		s(t) for %D2 (t and f)			
	Flat top smpling	pulse train (t and f)		1	1.5
		s(t) (t and f)			
		s(t) for f1 (t and f)			
		s(t) for f2 (t and f)			
		s(t) for %D1 (t and f)			
		s(t) for %D2 (t and f)			
	Demodulation	normal m and m' (t and f)		1	1
		flat top m and m' (t and f)			
graphs/results	Aliasing	Natural s(t) (t and f)		1	1
		flat top s(t) (t and f)			
		m and m' (t and f)			
				8.5	10

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1. Part 1: Time and Frequency Characteristics of the pulse train

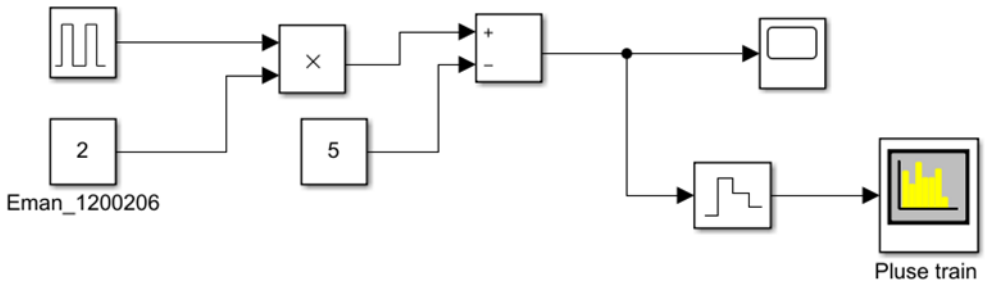

Figure 1: Block digram

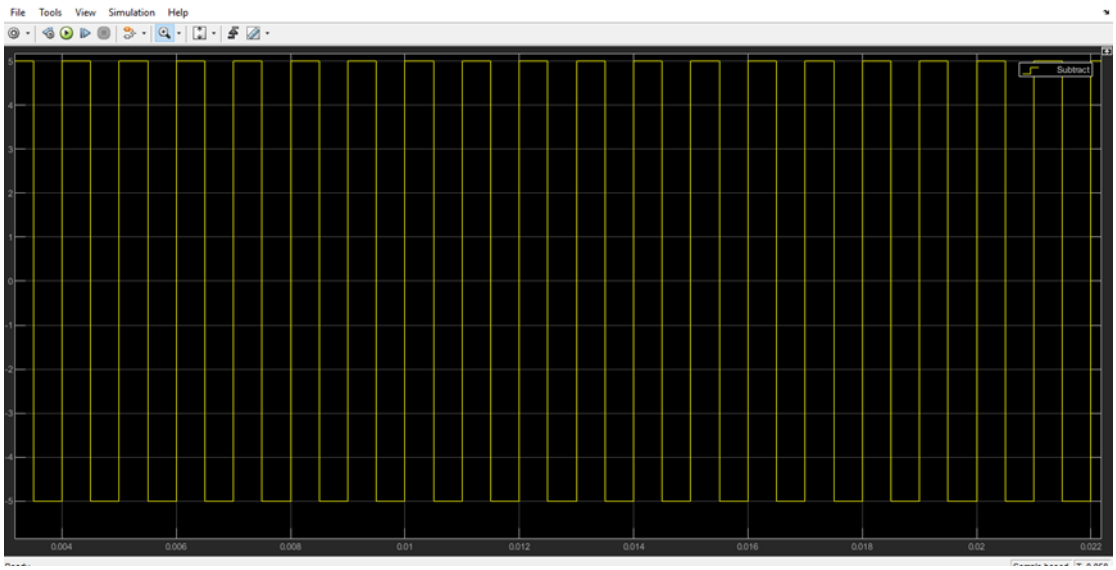

Figure 2: The Output of Dutey Cycle 50% and frequecy 500

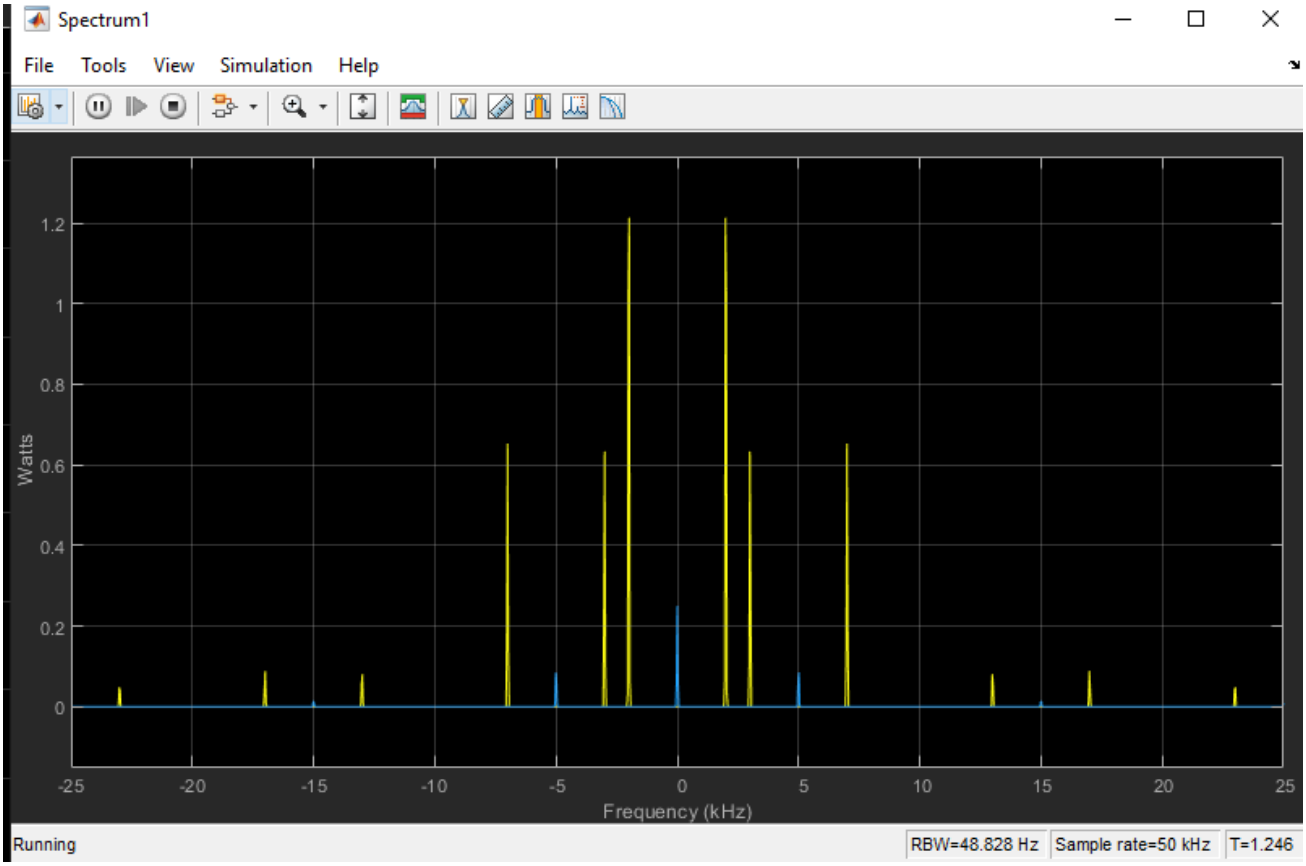

Figure 3:The Running Output in frequency

change duty cycle?

2. Part 2: Characteristics of Pulse Amplitude Modulation (PAM)

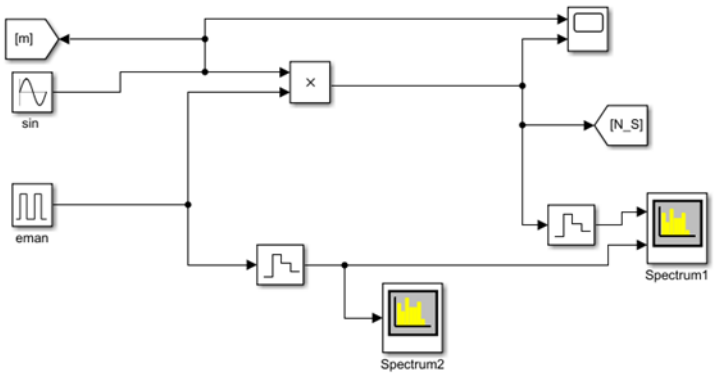

Figure 4 :Block Digram

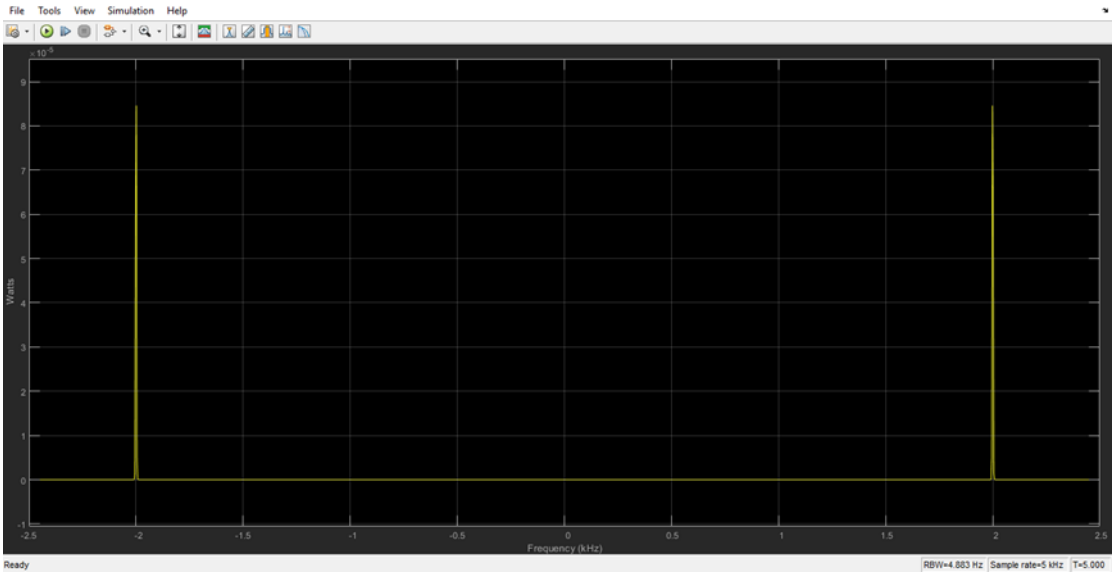

Figure 5:The Connected Circuit output

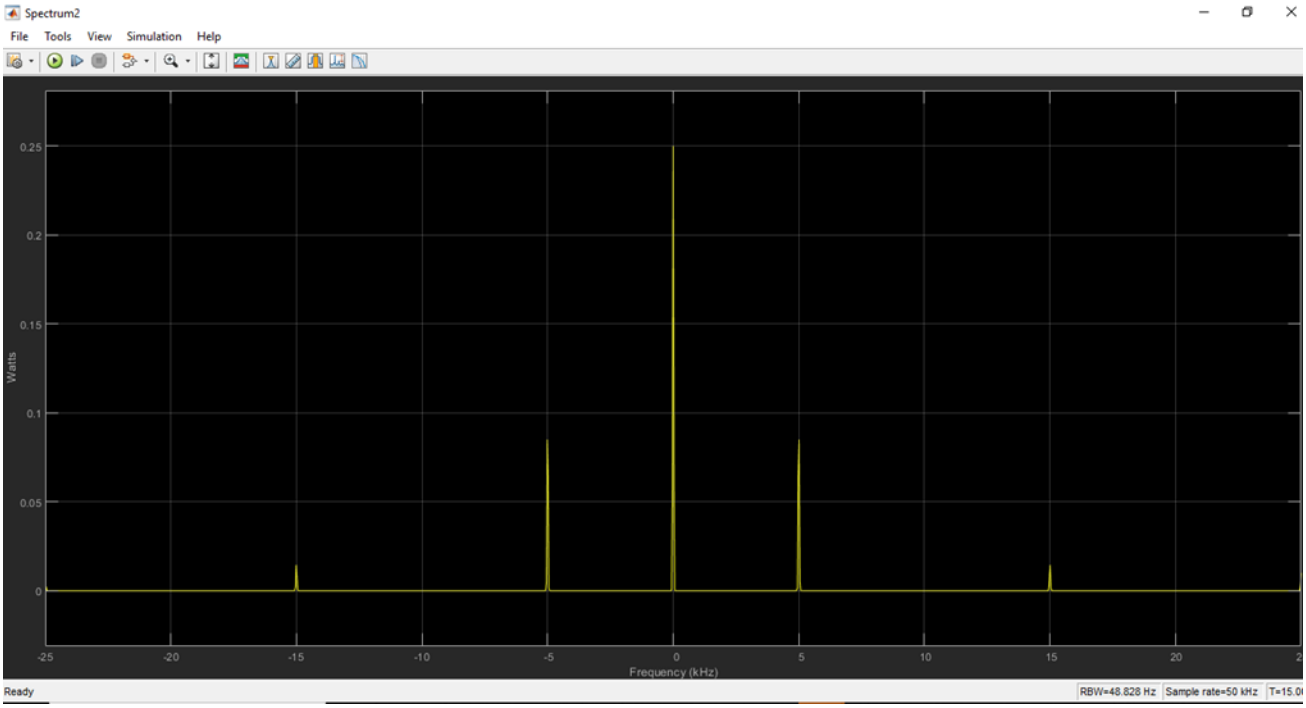

Figure 6:The Running Output

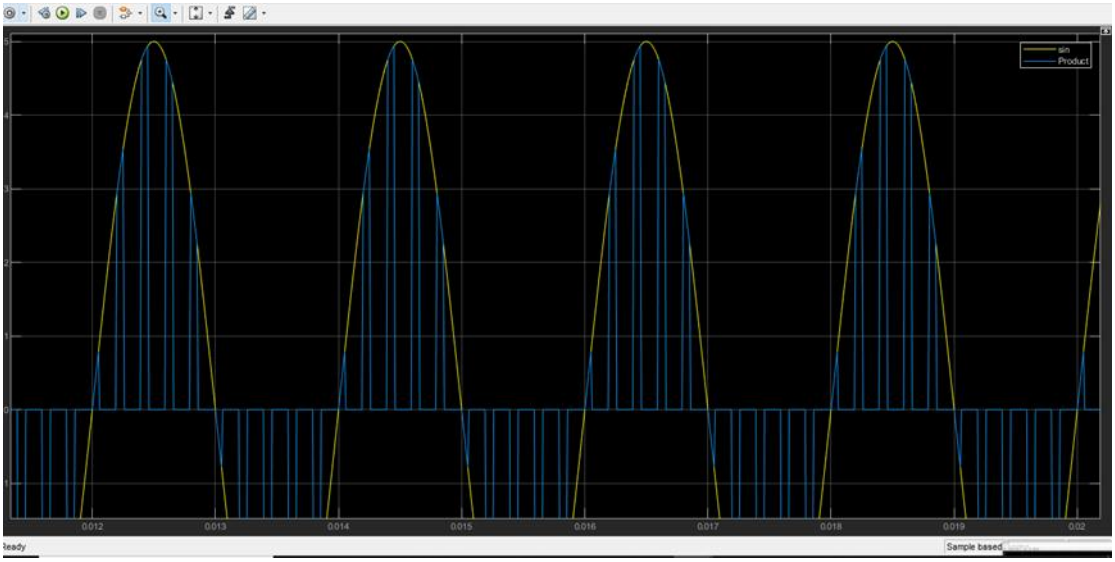

Figure 4: The Running Output with DC=50%

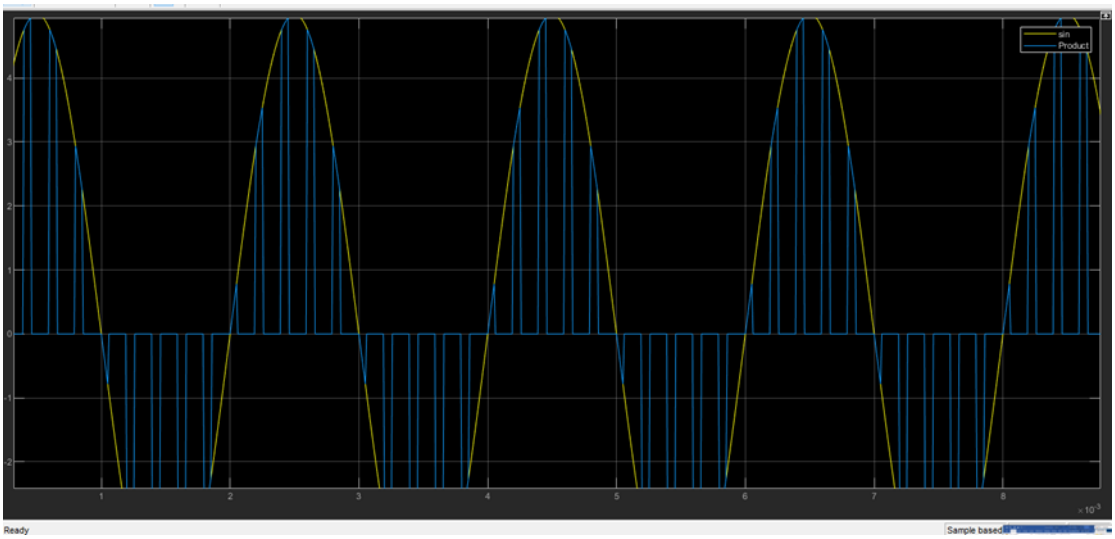

Figure 5: The Running Output

change duty cycle and frequency?

3. Part 3: Characteristics of Pulse Amplitude Demodulation

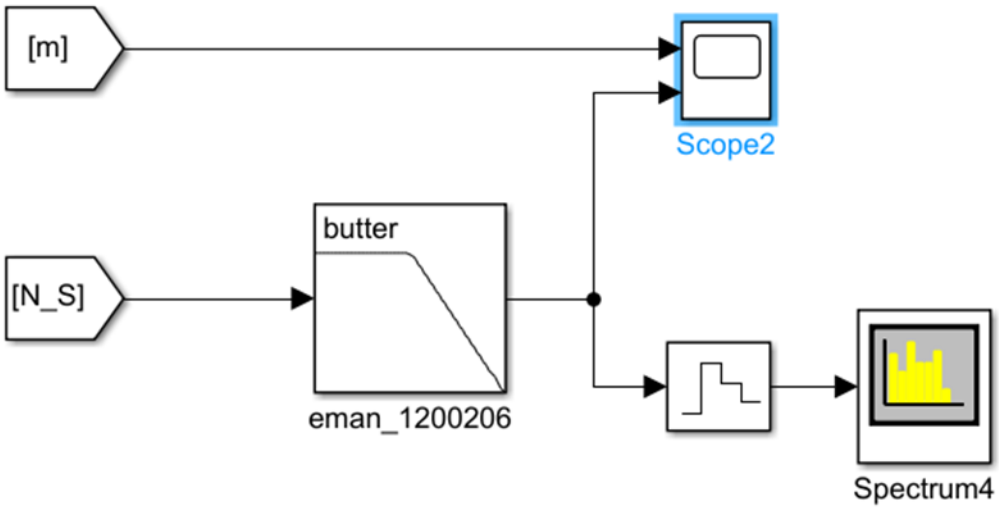

Figure 6: The Block Diagram

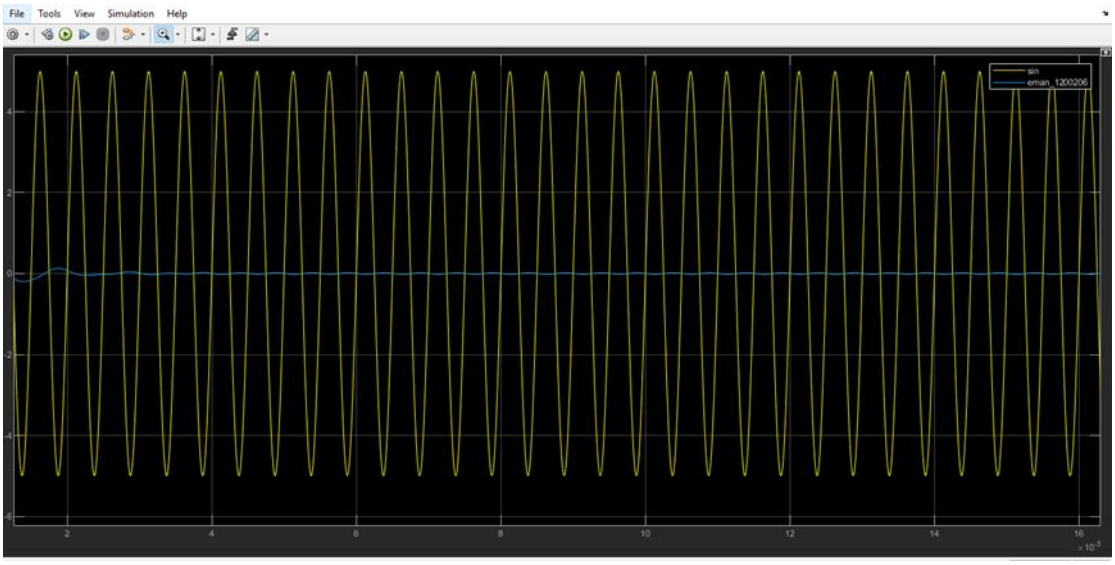

Figure 7: Circuit Output in time domain

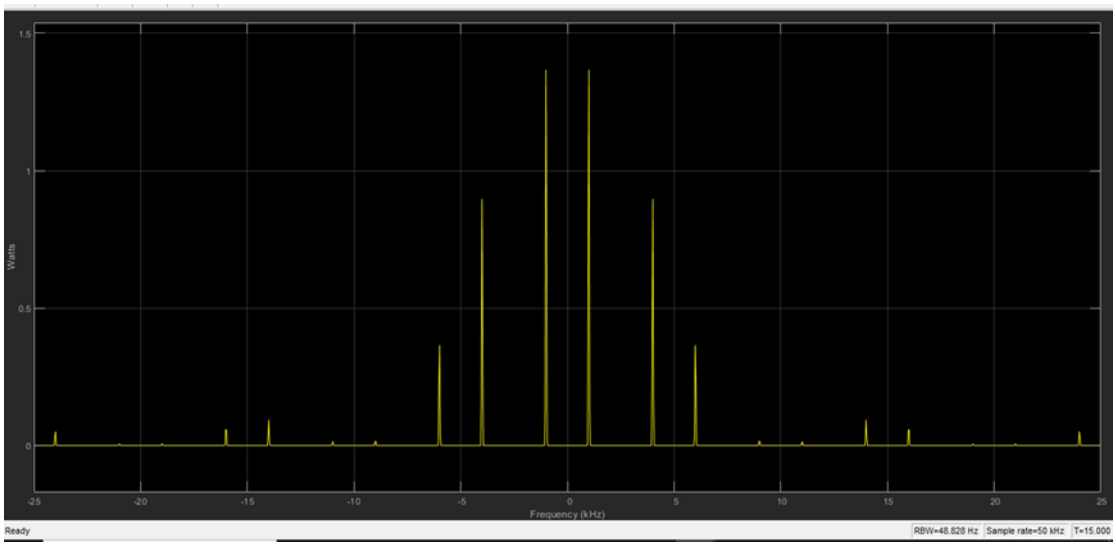

Figure 8: The running output in frequency domain

4. Part 4: Aliasing in the Time and the Frequency Domains:

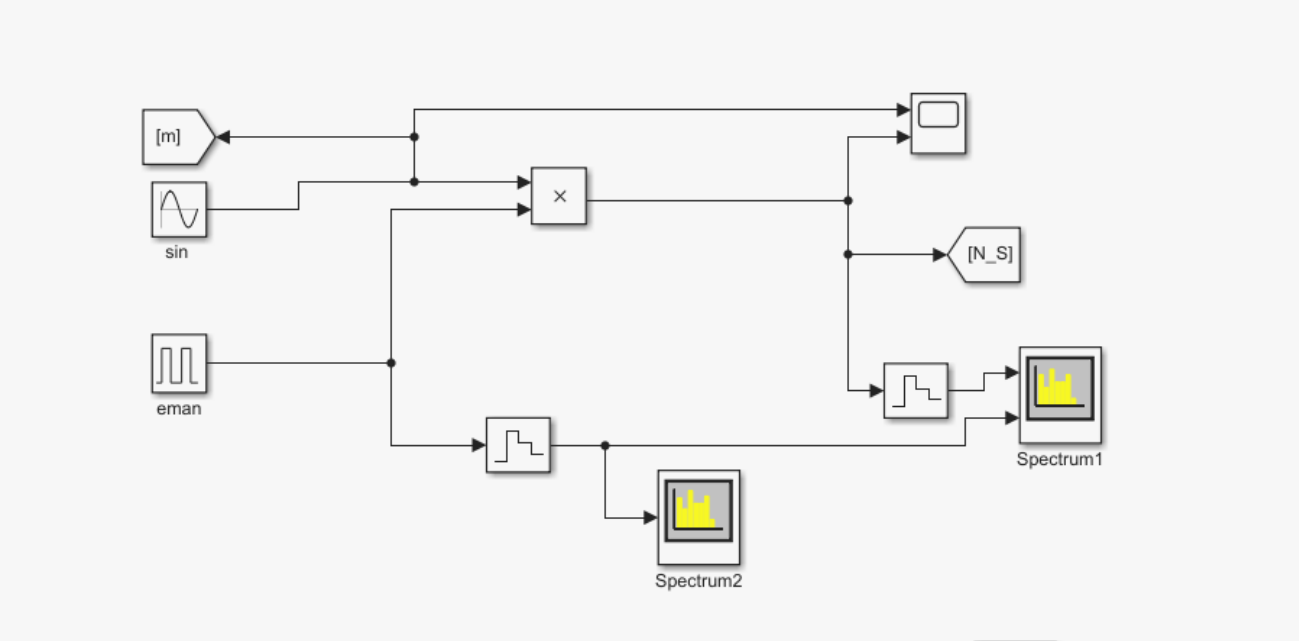

Figure 96: Block Digram Connection

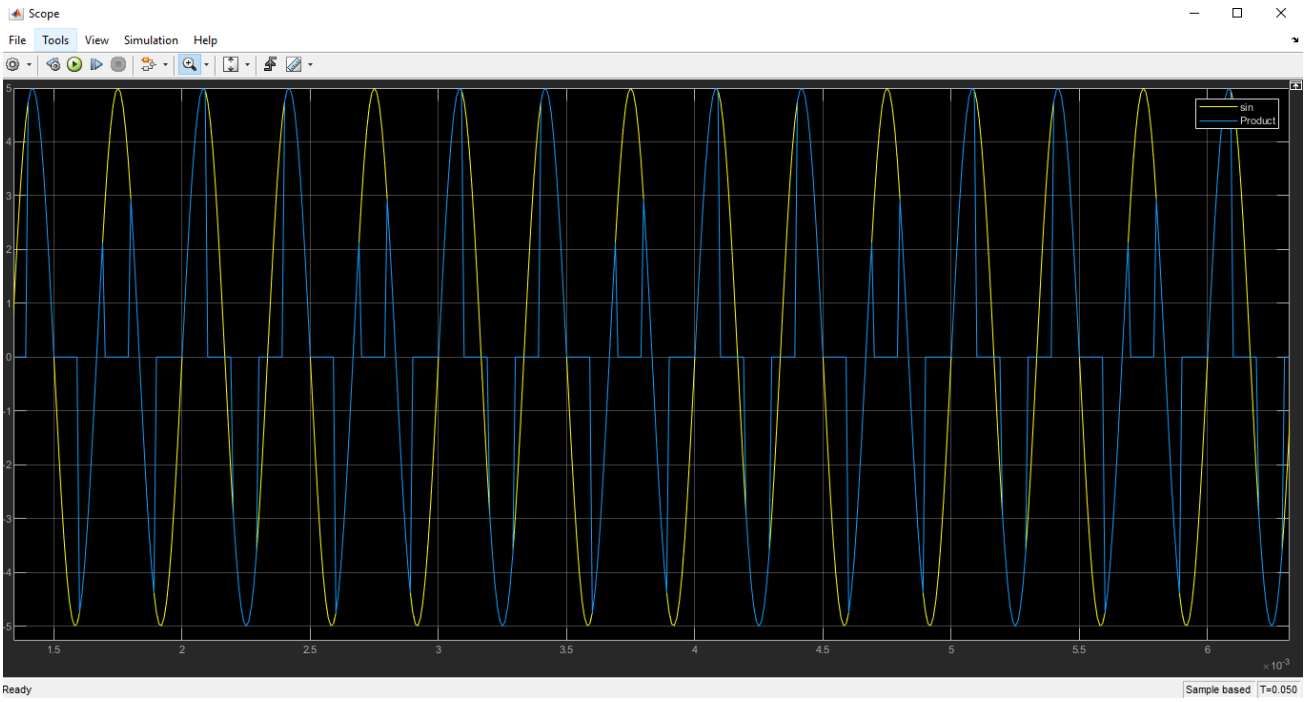

Figure 107: The running output

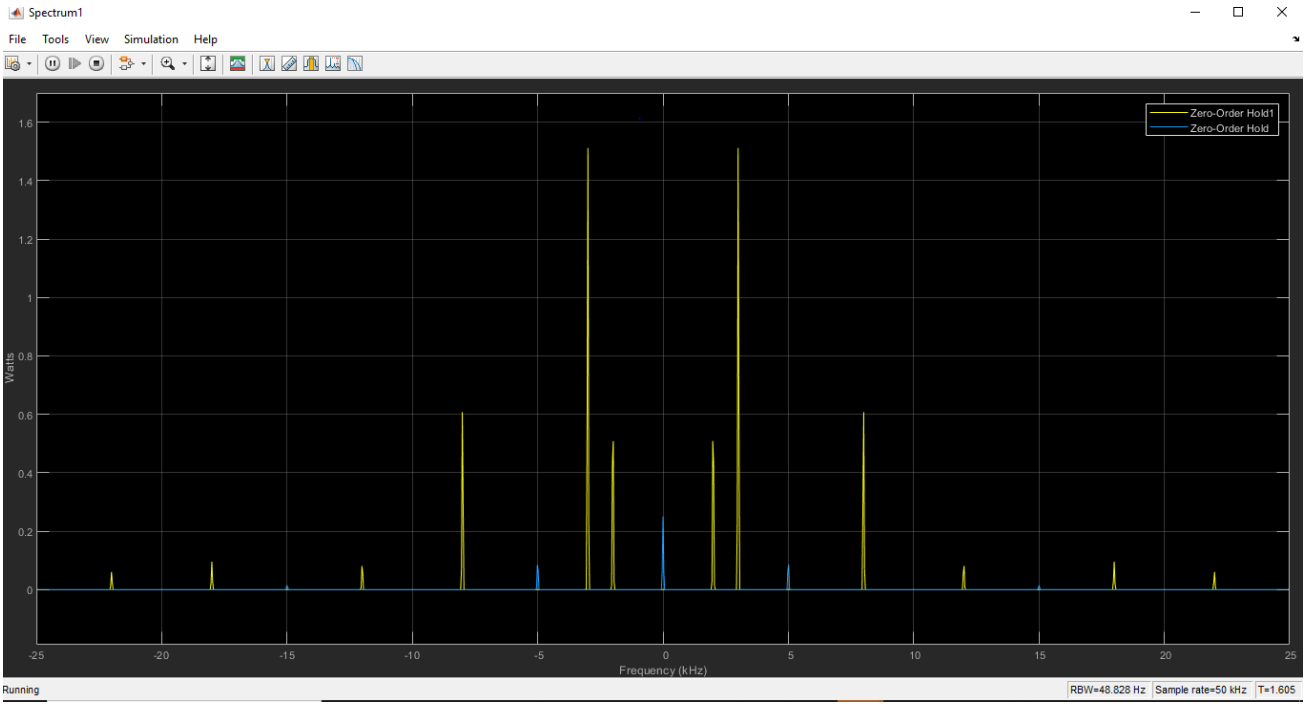

Figure 118: The running output

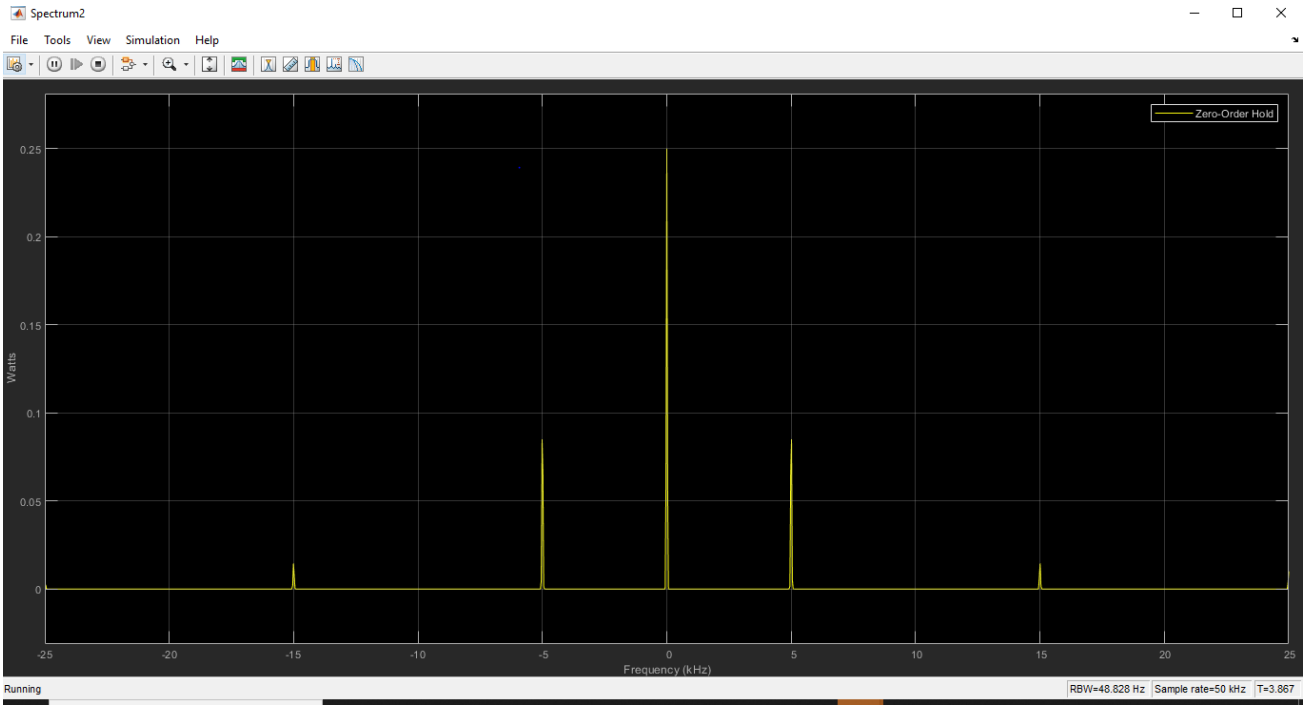

Figure 19: The running output

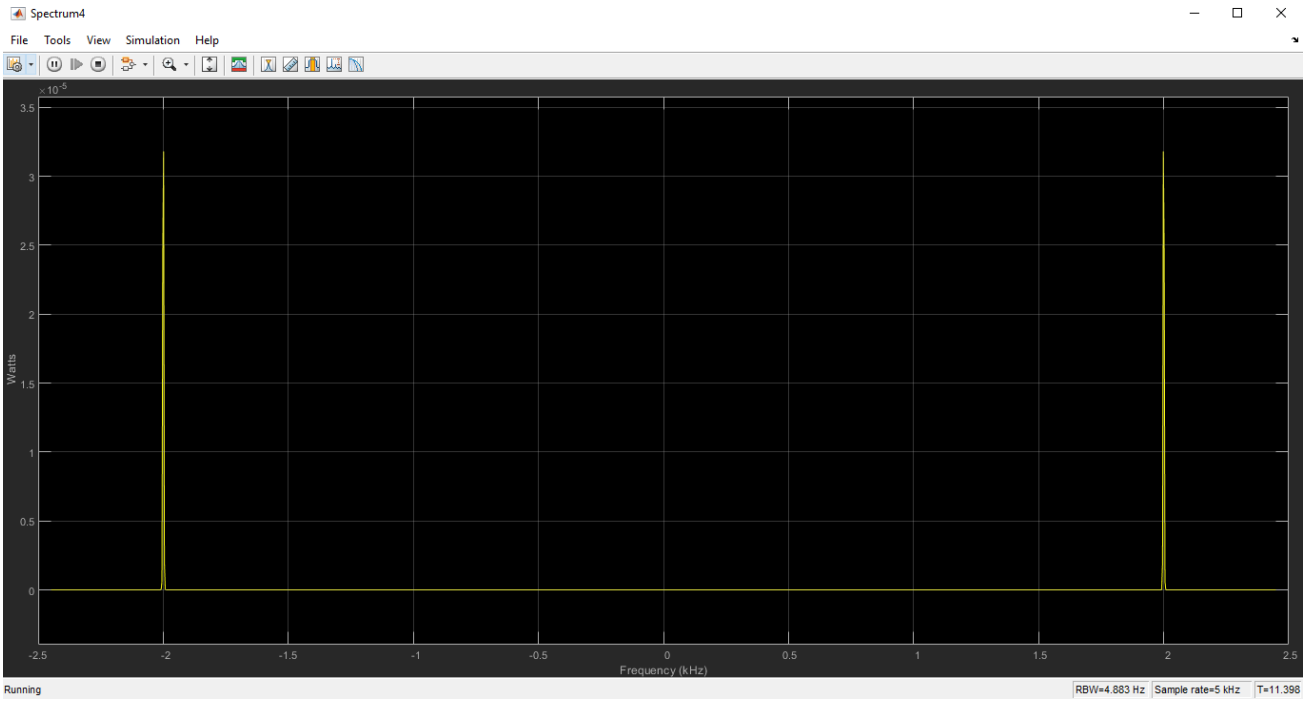

Figure 20: The running output demodualtour

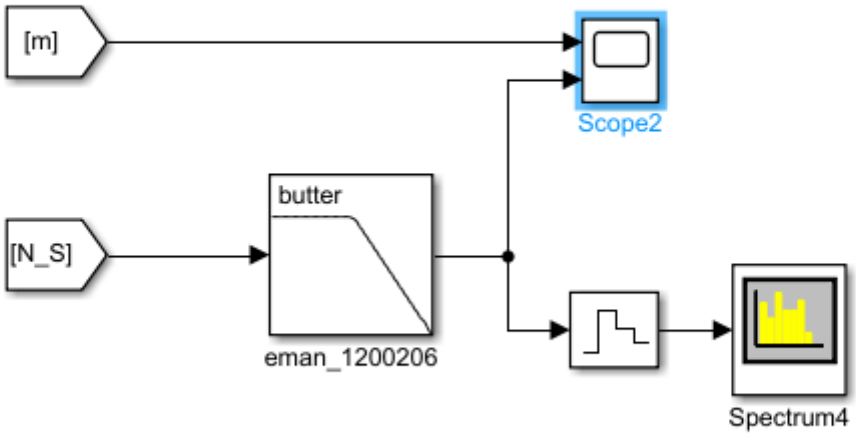

Figure 21: The running output demodulator

5. Part 5: PAM Time Multiplex:

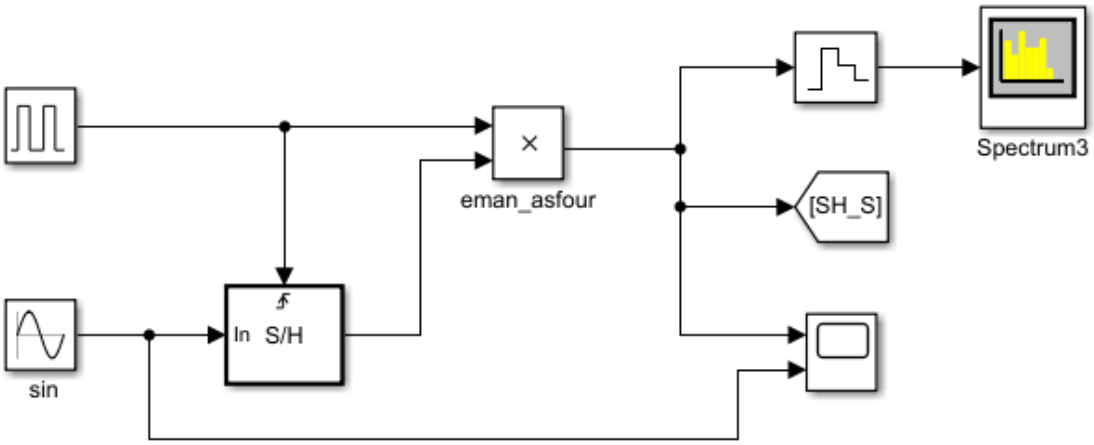

Figure 22: Block Digram Connection

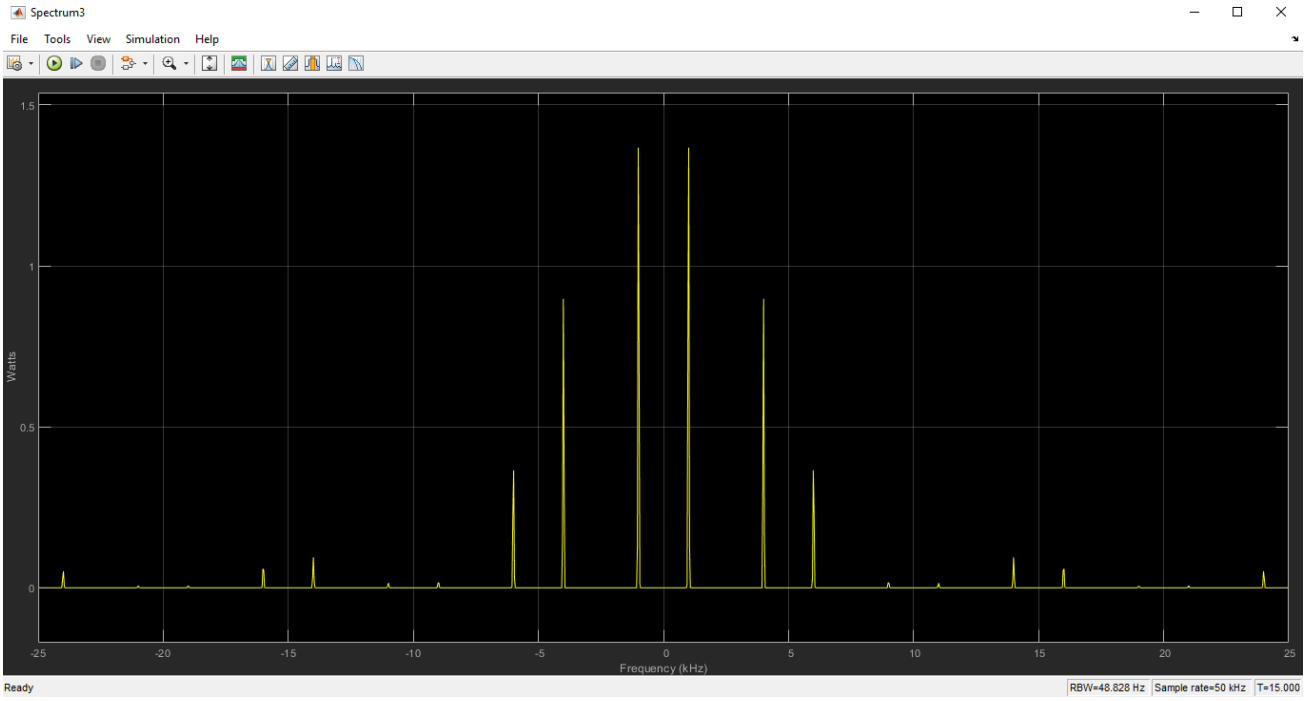

Figure 23: The running output

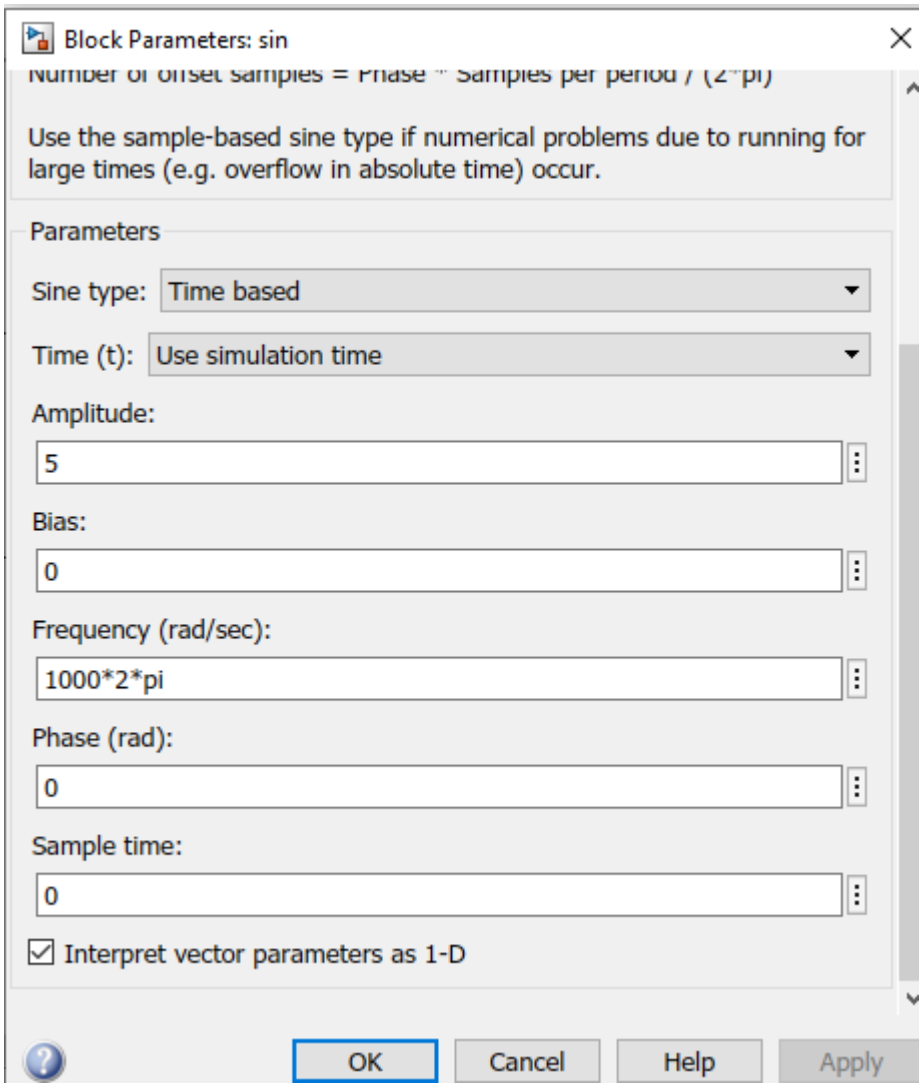

Figure 24: The Setting

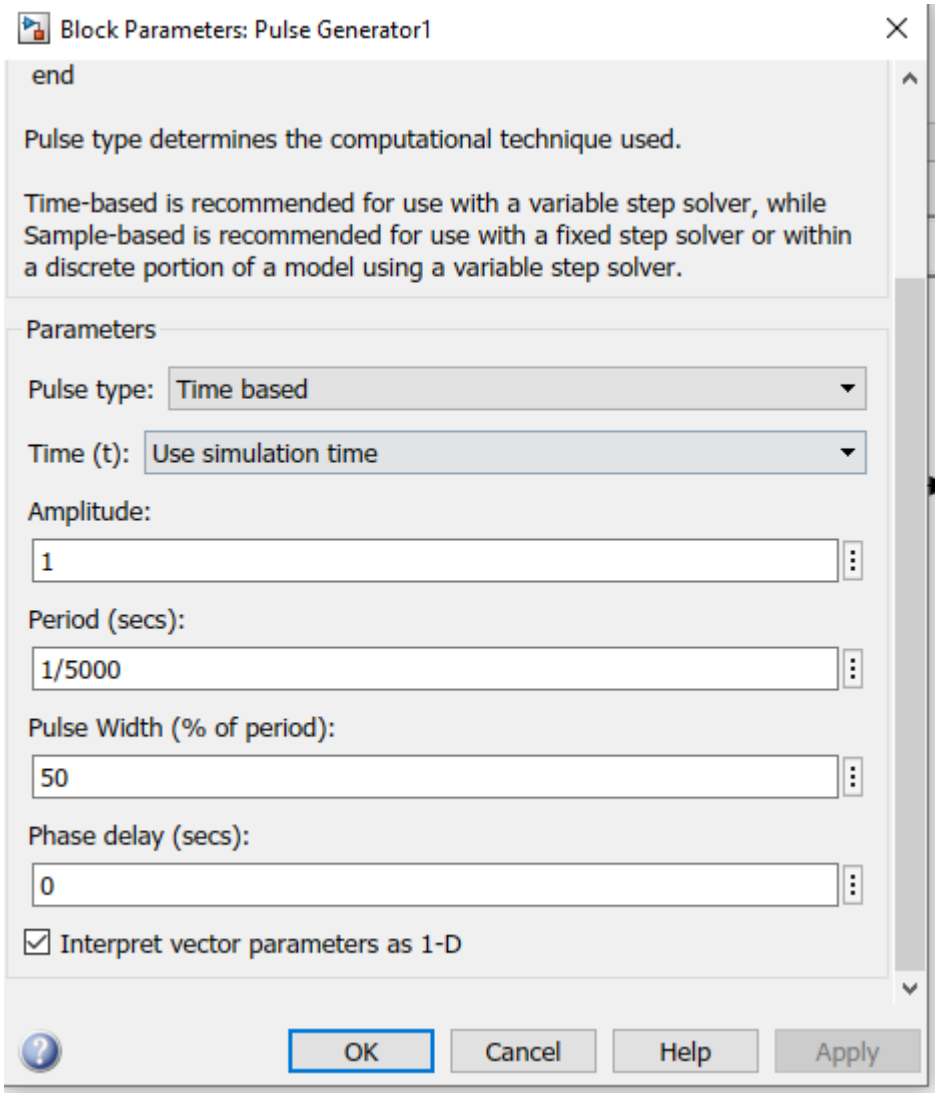

Figure 25: The Setting

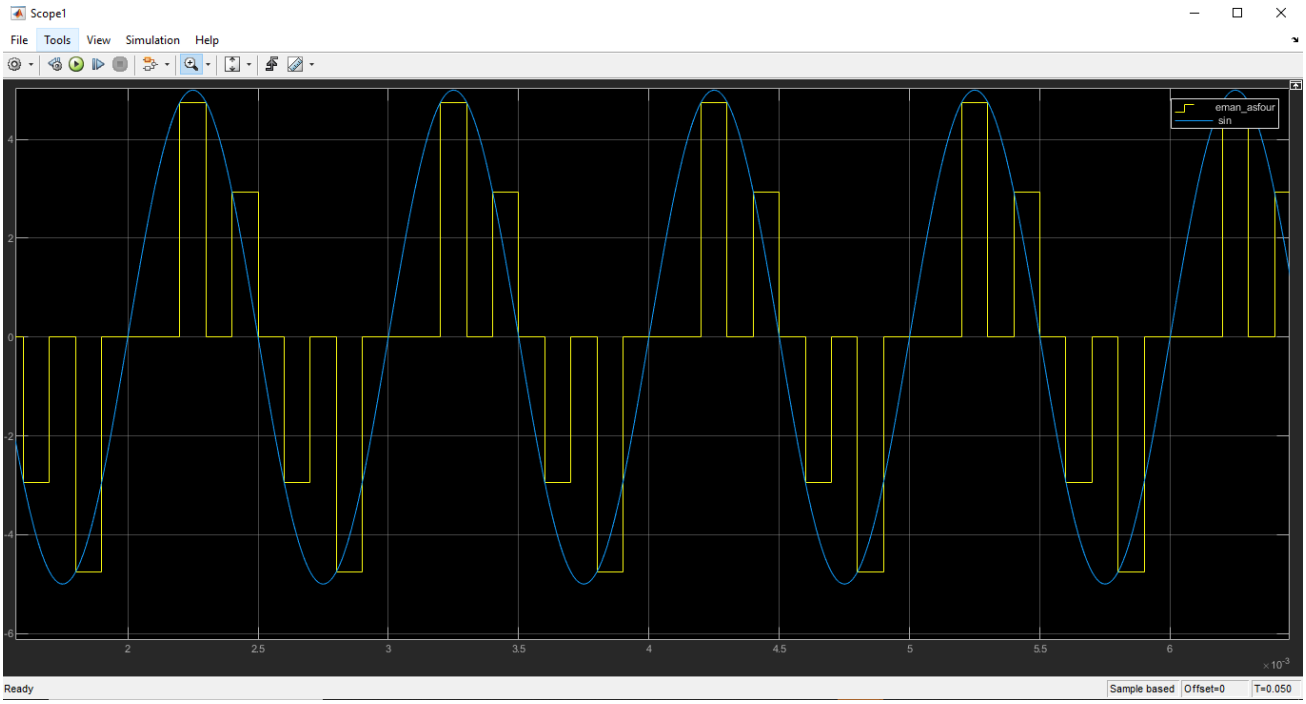

Figure 26: The Output in Frequency domain

change f and duty cycle