Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY (ENCS2110)

“Pre-lab(Experiment5)”

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Design the Logic Diagram, function table of the SR latch using NOR gates, and Explain how it works

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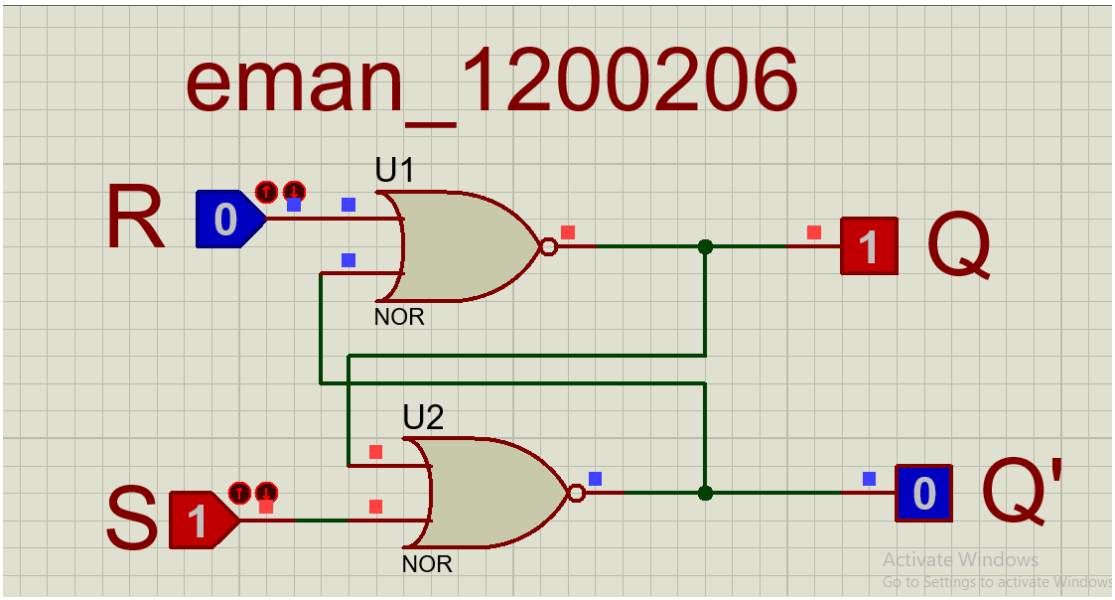

Figure 1:SR_latch implement by NOR

Inputs		Outputs	
S	R	Q	Q
0	0	Q0	Q'
0	1	0	1
1	0	1	0
1	1	x	x

The restricted combination or forbidden state arises when both the Reset (R) and Set (S) inputs of a latch are simultaneously set to 1, resulting in an output of 0 and enforcing Q = Q'. This state triggers issues like race conditions, where the output toggles between 0 and 1, leading to prolonged damped oscillations before settling and causing uncertainty in subsequent stages due to undetermined logic values. To enhance circuit reliability and stability, it is crucial to prevent this state by managing input sequencing, addressing timing concerns, and employing careful circuit design techniques that consider noise margins, feedback paths, and propagation delays. Such measures collectively reduce the chances of encountering the restricted combination state and its associated problems in digital logic .circuits