Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY (ENCS2110)

"Pre-lab 8(Experiment8)"

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Section: 4

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```
module priority_encoder_4x2 (input [3:0] A);
  reg [1:0] Y;
  always @* begin
  Y[1:0] = 2'b00;
  if (A[3] == 1'b1) Y[1:0] = 2'b11;
  else if (A[2] == 1'b1) Y[1:0] = 2'b10;
  else if (A[1] == 1'b1) Y[1:0] = 2'b01;
  else if (A[0] == 1'b1) Y[1:0] = 2'b00;
  end
  endmodule
```

module priority_encoder_4x2 (input [3:0] A);

reg [1:0] Y;

always @* begin

Y[1:0] = 2'b00;

if (A[3] == 1'b1) Y[1:0] = 2'b11;

else if (A[2] == 1'b1) Y[1:0] = 2'b10;

else if (A[1] == 1'b1) Y[1:0] = 2'b01;

else if (A[0] == 1'b1) Y[1:0] = 2'b00;

end

endmodule

```
module seven_segment_display(out,in);
 input [1:0] in;
 output reg [6:0]out;
 always @(in)
begin
case(in)
 0:out=7'b0000001;
 0:out=7'b1001111;
 0:out=7'b0010010;
 0:out=7'b0000110;
 endcase
 end
 endmodule
```

module seven_segment_display(out,in);

input [1:0] in;

output reg [6:0]out;

always @(in)

begin

case(in)

0:out=7'b0000001;

0:out=7'b1001111;

0:out=7'b0010010;

0:out=7'b0000110;

endcase

end

endmodule

```
1  module D_Flip_Flop (input D,Clk);
2   reg Q;
3   always @(posedge Clk)
4   begin
5   Q <= D;
6   end
7  endmodule
```

module D_Flip_Flop (input D,Clk);

reg Q;

always @(posedge Clk)

begin

Q <= D;

end

endmodule

```
module mux_2x1 (input sel, input a, input b, output y);
 assign y = sel ? b : a;
endmodule
```

module mux_2x1 (input sel, input a, input b, output y);

assign y = sel ? b : a;

endmodule

```
1  module comparator(out, in);
2      input [6:0] in;
3      output reg out;
4
5      always @(in)
6      begin
7          if (in == 7'b0100100)
8              out = 1'b1;
9          else
10             out = 1'b0;
11     end
12 endmodule
13
```

```
module comparator(out, in);
  input [6:0] in;
  output reg out;

  always @(in)
  begin
    if (in == 7'b0100100)
      out = 1'b1;
    else
      out = 1'b0;
  end
```

```
endmodule
```