



Universidade de Brasília  
Instituto de Ciências Exatas  
Dpto. Ciência da Computação  
Organização e Arquitetura de Computadores

## **Projeto da Disciplina - RISC-V Uniciclo em VHDL**

José Roberto Interaminense Soares 19/0130008  
Emanuel Firmino Abrantes 19/0105747

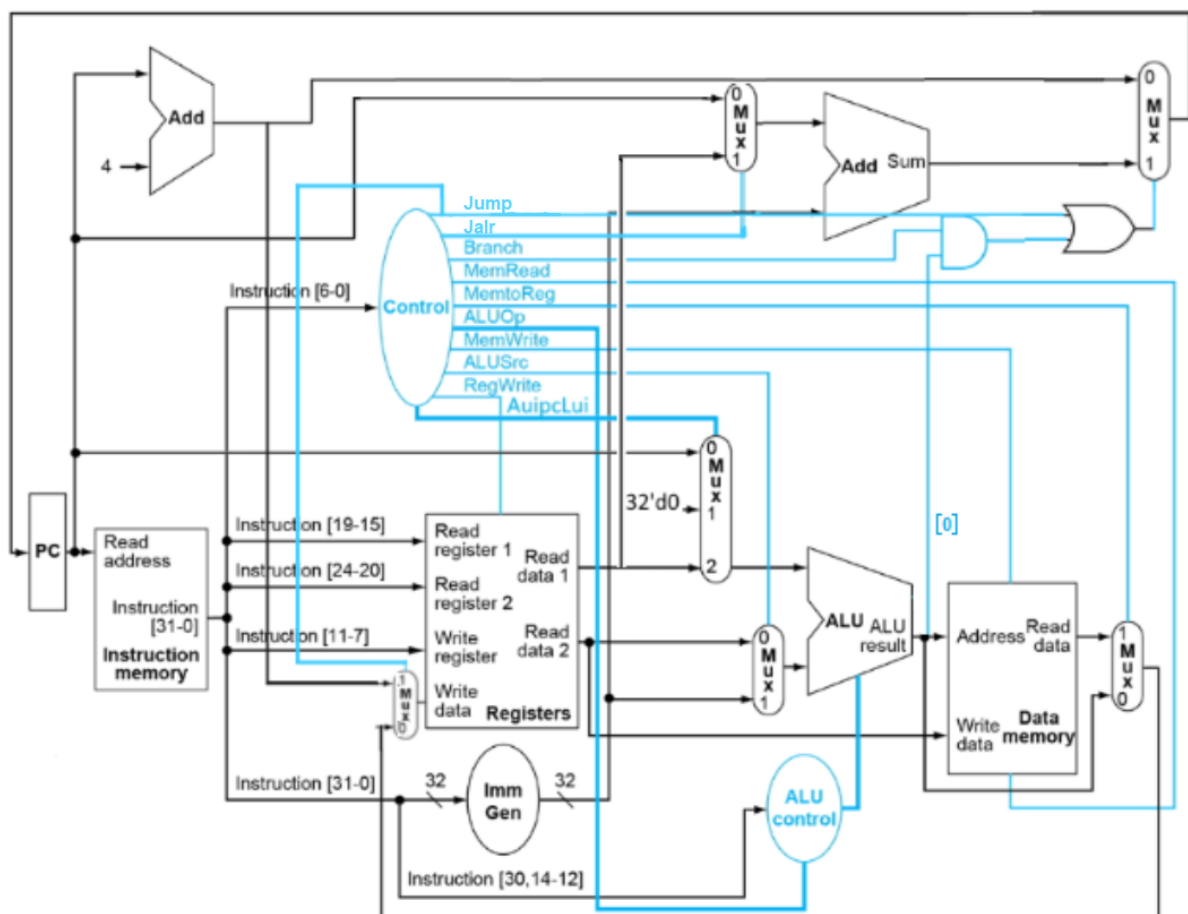
Brasília - DF  
Outubro, 2022

O trabalho teve o objetivo de desenvolver uma versão do processador Risc-V na arquitetura uniciclo utilizando a linguagem de descrição de hardware VHDL. A ferramenta utilizada para desenvolvimento foi o ModelSim, compilando os arquivos na versão de 1076-2008.

As operações implementadas foram as seguintes:

- Geração de constantes: AUIPC, LUI
- Aritméticas: ADD, SUB
- Aritméticas com imediato: ADDI
- Shift: SLL, SRL, SRA
- Comparação: SLT, SLTu
- Comparação com imediato: SLTi, SLTUi
- Subrotinas: JAL, JALR
- Saltos 1: BEQ, BNE
- Memória: LW, SW

O diagrama esquemático utilizado será o seguinte:



**Figura 1.0:** esquema do riscV

Existem portanto 10 sinais de controles, onde da arquitetura original, foram adicionados 3: Jump, JalR, e AuipcLui, que habilitam ou desabilitam os componentes para realizar tais operações.

Os módulos desenvolvidos (em VHDL), que compõem o modelo do RISCV Uniciclo ilustrado acima, são:

- Somador;

Soma duas entradas e retorna valor da soma em `std_logic_vector`.

- Multiplexador 2 para 1;

Recebe duas entradas e um seletor, e retorna multiplexação.

- Multiplexador 3 para 1;

Recebe três entradas e um seletor, e retorna multiplexação.

- Controle da ULA;

Recebe a operação da ULA, `funct3` e `funct7`, retorna opcode.

- ULA (Unidade Lógico/Aritmética);

Recebe o opcode do controle, e realiza a operação.

- Gerador de Imediatos de 32 bits;

Recebe instrução, faz máscara e shift e retorna o imediato.

- Banco de Registradores (32 registradores de 32 bits);

Escreve ou lê dos registradores.

- Controle de Sinais;

Faz o controle dos mux

- PC (Contador de Programa);

Representa o bloco PC.

- Memória de Dados;

Lê arquivo de texto que contém memória de dados.

- Memória de instruções.

Lê arquivo de texto que contém as instruções a serem executadas.

E cada um foi devidamente testado individualmente.

## **Teste inicial para as instruções ADDi e SUB**

Com o objetivo de verificar o pleno funcionamento das instruções ‘addi’ e ‘sub’, o breve trecho de código apresentado abaixo foi elaborado para tal finalidade:

```

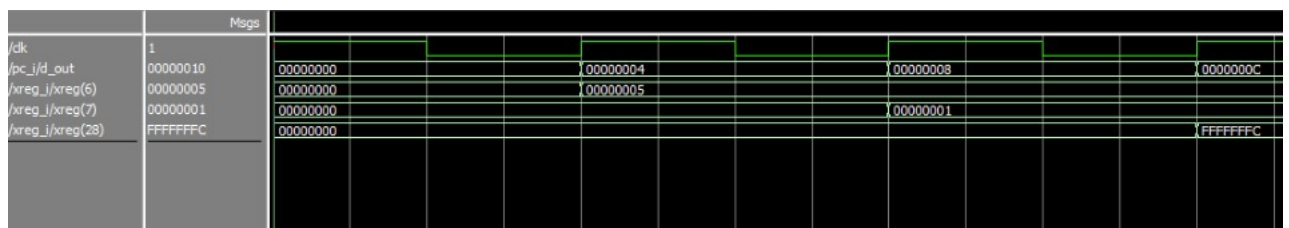
.text

    addi t1, t1, 5
    addi t2, t2, 1
    sub  t3, t2, t1

```

**Figura 2.1:** código de teste para as instruções *addi* e *sub*.

Com a utilização do ModelSim, foi possível obter o resultado das formas de ondas geradas pelo RISC-V Uniciclo desenvolvido, como apresentado abaixo:



**Figura 2.2:** formas de onda geradas pelo processador, obtidas por intermédio do software ModelSim.

Onde:

- xreg(6) equivale ao registrador temporário t1;
- xreg(7) equivale ao registrador temporário t2;
- xreg(28) equivale ao registrador temporário t3.

## Teste Geral

Em um programa real, várias instruções serão utilizadas. Para teste, foi feito um programa com todas as instruções que o processador construído consegue suportar. O programa pode ser visto a seguir:

Programa teste
----------------

```
.data
num_test:    .word    0x00000002
.text
```

```
teste:
    addi t1, t1, 4
    lw t2, num_test
    add t3, t1, t2
    sub t1, t2, t3
    slt t3, t1, t2
    sltu t2, t1, t3
    sra t2, t1, t3
    slti t2, t2, 1
    sll t2, t2, t2
    lui t1, 0x00001
    srl t1, t1, t2
    auipc t3, 0x00000
    beq t1, t3, teste
    addi t1, zero, 2
    bne t1, t2, teste
    jal teste2
```

```
teste2:
    jalr t1, zero, 0
```

---

Os resultados de t1, t2 e t3 a cada instrução foram retirados do Rars e serão comparados com o formato de onda do simulador.

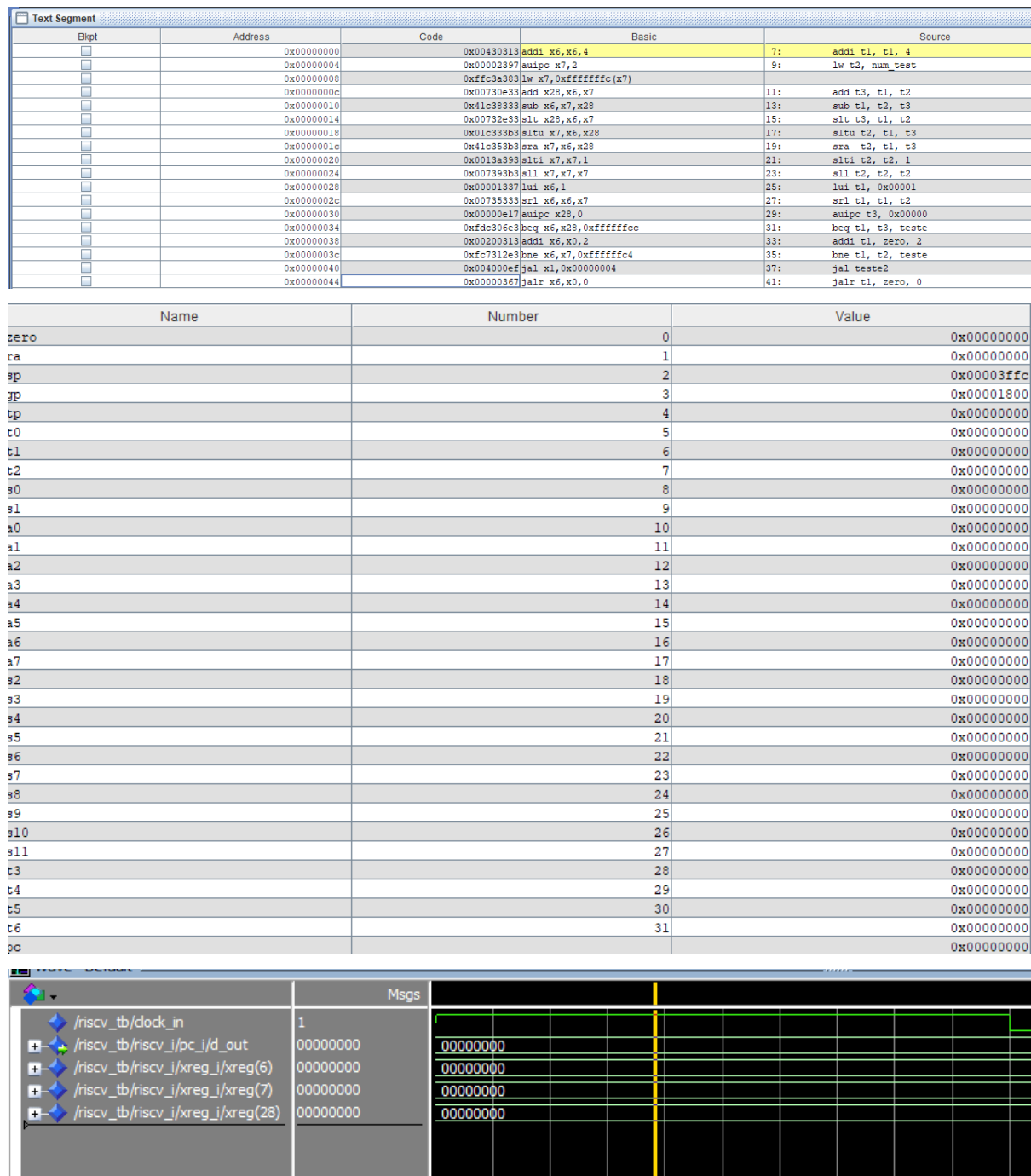
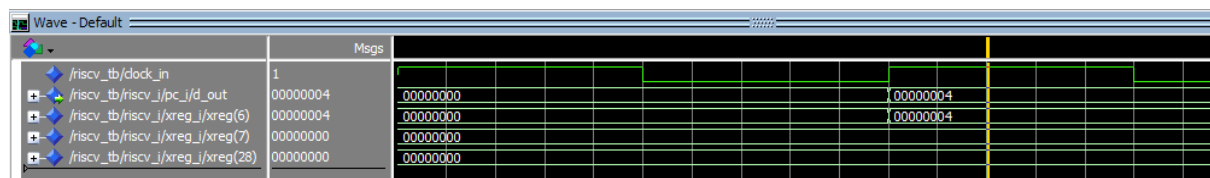


Figura 3.1: execução da instrução addi t1, t1, 4; estado dos registradores; formas de ondas obtidas.

Bkpt	Address	Code	Basic	Source
	0x00000000	0x00430313	addi x6,x6,4	7: addi t1, t1, 4
	0x00000004	0x00002397	auipc x7,2	9: lw t2, num_test
	0x00000008	0xffc3a383	lw x7,0xfffffff(x7)	
	0x0000000c	0x00730e33	add x29,x6,x7	11: add t3, t1, t2
	0x00000010	0x41c38333	sub x6,x7,x28	13: sub t1, t2, t3
	0x00000014	0x00732e33	slt x29,x6,x7	15: slt t3, t1, t2
	0x00000018	0x01c33b33	sltu x7,x6,x28	17: sltu t2, t1, t3
	0x0000001c	0x41c35b33	sra x7,x6,x28	19: sra t2, t1, t3
	0x00000020	0x0013a393	slti x7,x7,1	21: slti t2, t2, 1
	0x00000024	0x00739b33	sll x7,x7,x7	23: sll t2, t2, t2
	0x00000028	0x00001337	lui x6,1	25: lui t1, 0x00001
	0x0000002c	0x00735333	srl x6,x6,x7	27: srl t1, t1, t2
	0x00000030	0x00000e17	auipc x28,0	29: auipc t3, 0x00000
	0x00000034	0xfdc30e33	beq x6,x28,0xfffffffcc	31: beq t1, t3, teste
	0x00000038	0x00200313	addi x6,x0,2	33: addi t1, zero, 2
	0x0000003c	0xfc7312e3	bne x6,x7,0xfffffffcc4	35: bne t1, t2, teste
	0x00000040	0x004000ef	jai x1,0x00000004	37: jai teste2
	0x00000044	0x00000367	jair x6,x0,0	41: jair t1, zero, 0

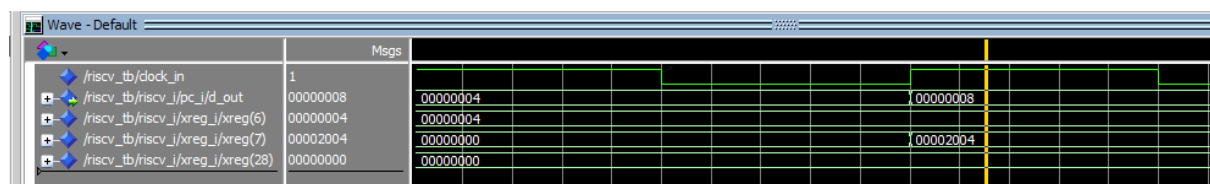
Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0x00000004
t2	7	0x00000000
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000000
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000004



**Figura 3.2:** execução da instrução `auipc`, que calcula o endereço de `num_test`; estado dos registradores; formas de ondas obtidas.

Bkpt	Address	Code	Basic	Source
	0x00000000	0x00430313	addi x6,x6,4	7: addi t1, t1, 4
	0x00000004	0x00002397	auipc x7,2	9: lw t2, num_test
	0x00000008	0xffc3a383	lw x7,0xfffffff(x7)	
	0x0000000c	0x00730e33	add x28,x6,x7	11: add t3, t1, t2
	0x00000010	0x41c38333	sub x6,x7,x28	13: sub t1, t2, t3
	0x00000014	0x00732e33	slt x28,x6,x7	15: slt t3, t1, t2
	0x00000018	0x01c333b3	sltu x7,x6,x28	17: sltu t2, t1, t3
	0x0000001c	0x41c353b3	sra x7,x6,x28	19: sra t2, t1, t3
	0x00000020	0x0013a393	slli x7,x7,1	21: slli t2, t2, 1
	0x00000024	0x007393b3	sll x7,x7,1	23: sll t2, t2, 2
	0x00000028	0x00001337	lui x6,1	25: lui t1, 0x00001
	0x0000002c	0x00735333	srl x6,x6,x7	27: srl t1, t1, t2
	0x00000030	0x00000e17	auipc x28,0	29: auipc t3, 0x00000
	0x00000034	0xfdc30e3	beq x6,x28,0xfffffff	31: beq t1, t3, teste
	0x00000038	0x00200313	addi x6,x0,2	33: addi t1, zero, 2
	0x0000003c	0xfc7312e3	bne x6,x7,0xfffffff4	35: bne t1, t2, teste
	0x00000040	0x004000ef	jai x1,0x00000004	37: jai teste2
	0x00000044	0x00000367	jair x6,x0,0	41: jair t1, zero, 0

Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0x00000004
t2	7	0x00002004
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000000
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000008



**Figura 3.3:** execução da instrução lw t2, num\_test; estado dos registradores; formas de ondas obtidas.



Text Segment					
Bkpt	Address	Code	Basic	Source	
	0x00000000	0x00430313	addi x6,x6,4	7:	addi t1, t1, 4
	0x00000004	0x00002397	auipc x7,2	9:	lw t2, num_test
	0x00000008	0xffc3a383	lw x7,0xfffffff(x7)		
	0x0000000c	0x00730e33	add x28,x6,x7	11:	add t3, t1, t2
	0x00000010	0x41c38333	sub x6,x7,x28	13:	sub t1, t2, t3
	0x00000014	0x00732e33	slt x28,x6,x7	15:	slt t3, t1, t2
	0x00000018	0x01c333b3	sltu x7,x6,x28	17:	sltu t2, t1, t3
	0x0000001c	0x41c353b3	sra x7,x6,x28	19:	sra t2, t1, t3
	0x00000020	0x0013a393	slti x7,x7,1	21:	slti t2, t2, 1
	0x00000024	0x007393b3	sll x7,x7,x7	23:	sll t2, t2, t2
	0x00000028	0x00001337	lui x6,1	25:	lui t1, 0x00001
	0x0000002c	0x00735333	srl x6,x6,x7	27:	srl t1, t1, t2
	0x00000030	0x00000e17	auipc x28,0	29:	auipc t3, 0x00000
	0x00000034	0xfdc306e3	beq x6,x28,0xfffffffcc	31:	beq t1, t3, teste
	0x00000038	0x00200313	addi x6,x0,2	33:	addi t1, zero, 2
	0x0000003c	0xfc7312e3	bne x6,x7,0xfffffff4	35:	bne t1, t2, teste
	0x00000040	0x004000ef	jal x1,0x00000004	37:	jal teste2
	0x00000044	0x00000367	jalr x6,x0,0	41:	jalr t1, zero, 0

Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0x00000004
t2	7	0x00000002
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000000
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x0000000c

Wave - Default			
	Msgs		
/riscv_tb/dock_in	1		
+ /riscv_tb/riscv_i/pc_i/d_out	0000000C	00000008	0000000C
+ /riscv_tb/riscv_i/xreg_i/xreg(6)	00000004	00000004	
+ /riscv_tb/riscv_i/xreg_i/xreg(7)	00000002	00002004	00000002
+ /riscv_tb/riscv_i/xreg_i/xreg(28)	00000000	00000000	

Figura 3.4: execução da instrução add t3, t1, t2; estado dos registradores; formas de ondas obtidas.

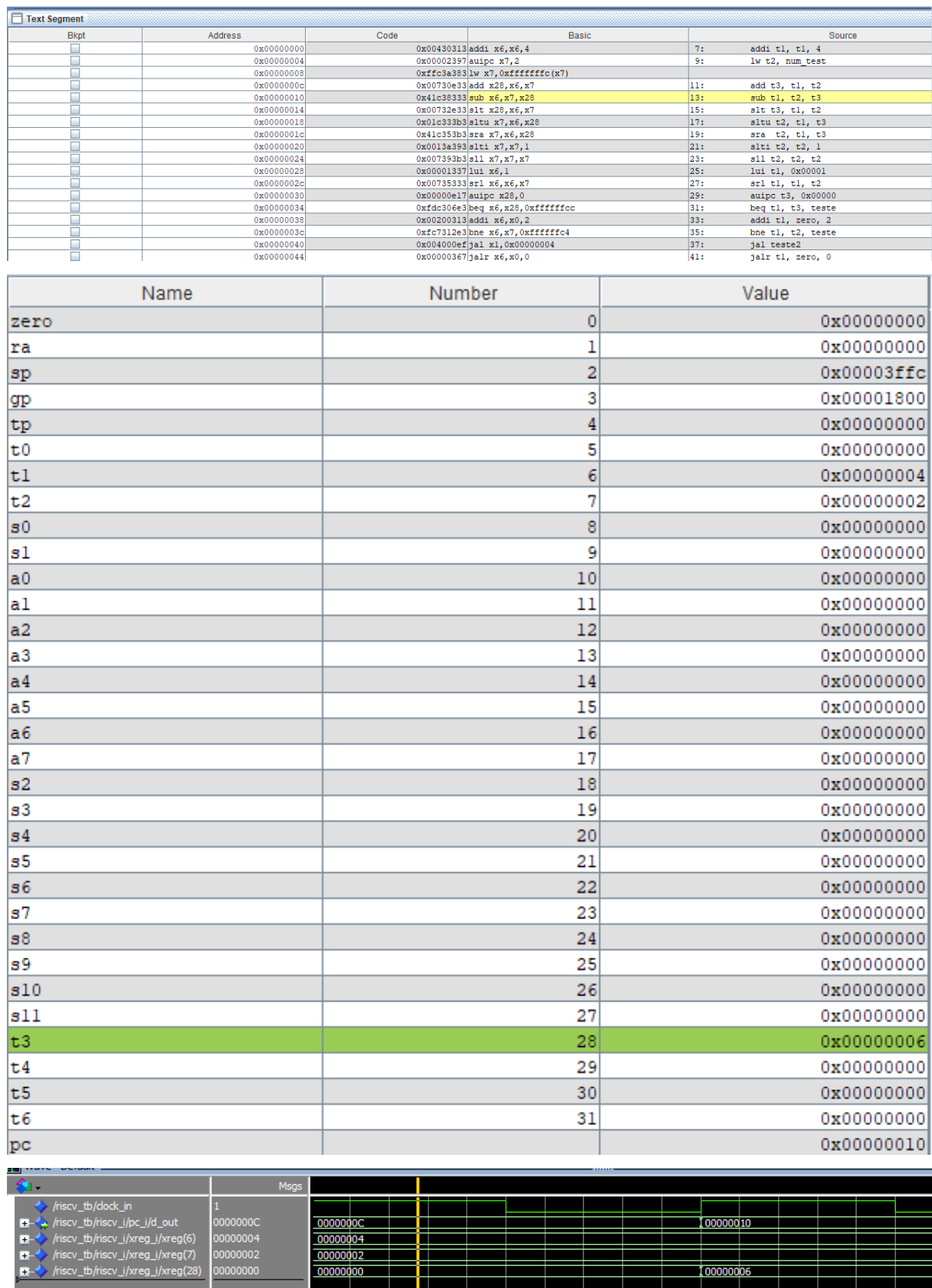


Figura 3.5: execução da instrução sub t1, t2, t3; estado dos registradores; formas de ondas obtidas.

Text Segment					
Bkpt	Address	Code	Basic	Source	
<input type="checkbox"/>	0x00000000	0x00430313	addi x6,x6,4	7:	addi t1, t1, 4
<input type="checkbox"/>	0x00000004	0x00002397	auipc x7,2	9:	lw t2, num_test
<input type="checkbox"/>	0x00000008	0xffc3a383	lw x7,0xffffffff(x7)		
<input type="checkbox"/>	0x0000000c	0x00730e33	add x28,x6,x7	11:	add t3, t1, t2
<input type="checkbox"/>	0x00000010	0x41c38333	sub x6,x7,x28	13:	sub t1, t2, t3
<input type="checkbox"/>	0x00000014	0x00732e33	slt x28,x6,x7	15:	slt t3, t1, t2
<input type="checkbox"/>	0x00000018	0x01c333b3	sltu x7,x6,x28	17:	sltu t2, t1, t3
<input type="checkbox"/>	0x0000001c	0x41c353b3	sra x7,x6,x28	19:	sra t2, t1, t3
<input type="checkbox"/>	0x00000020	0x0013a393	slti x7,x7,1	21:	slti t2, t2, 1
<input type="checkbox"/>	0x00000024	0x007393b3	sll x7,x7,x7	23:	sll t2, t2, t2
<input type="checkbox"/>	0x00000028	0x00001337	lui x6,1	25:	lui t1, 0x00001
<input type="checkbox"/>	0x0000002c	0x00735333	srl x6,x6,x7	27:	srl t1, t1, t2
<input type="checkbox"/>	0x00000030	0x00000e17	auipc x28,0	29:	auipc t3, 0x00000
<input type="checkbox"/>	0x00000034	0xfdc30e3	beq x6,x28,0xffffffff	31:	beq t1, t3, teste
<input type="checkbox"/>	0x00000038	0x00200313	addi x6,x0,2	33:	addi t1, zero, 2
<input type="checkbox"/>	0x0000003c	0xfc7312e3	bne x6,x7,0xffffffff	35:	bne t1, t2, teste
<input type="checkbox"/>	0x00000040	0x004000ef	jal x1,0x00000004	37:	jal teste2
<input type="checkbox"/>	0x00000044	0x000003e7	jalr x6,x0,0	41:	jalr t1, zero, 0

Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0xffffffff
t2	7	0x00000002
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000006
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000014

Wave - Default		Msgs
	/riscv_tb/dock_in	1
	/riscv_tb/riscv_i/pc_i/d_out	0000000C
	/riscv_tb/riscv_i/xreg_i/xreg(6)	00000004
	/riscv_tb/riscv_i/xreg_i/xreg(7)	00000002
	/riscv_tb/riscv_i/xreg_i/xreg(28)	00000000

Figura 3.6: execução da instrução addi t1, t1, 4; estado dos registradores; formas de ondas obtidas.

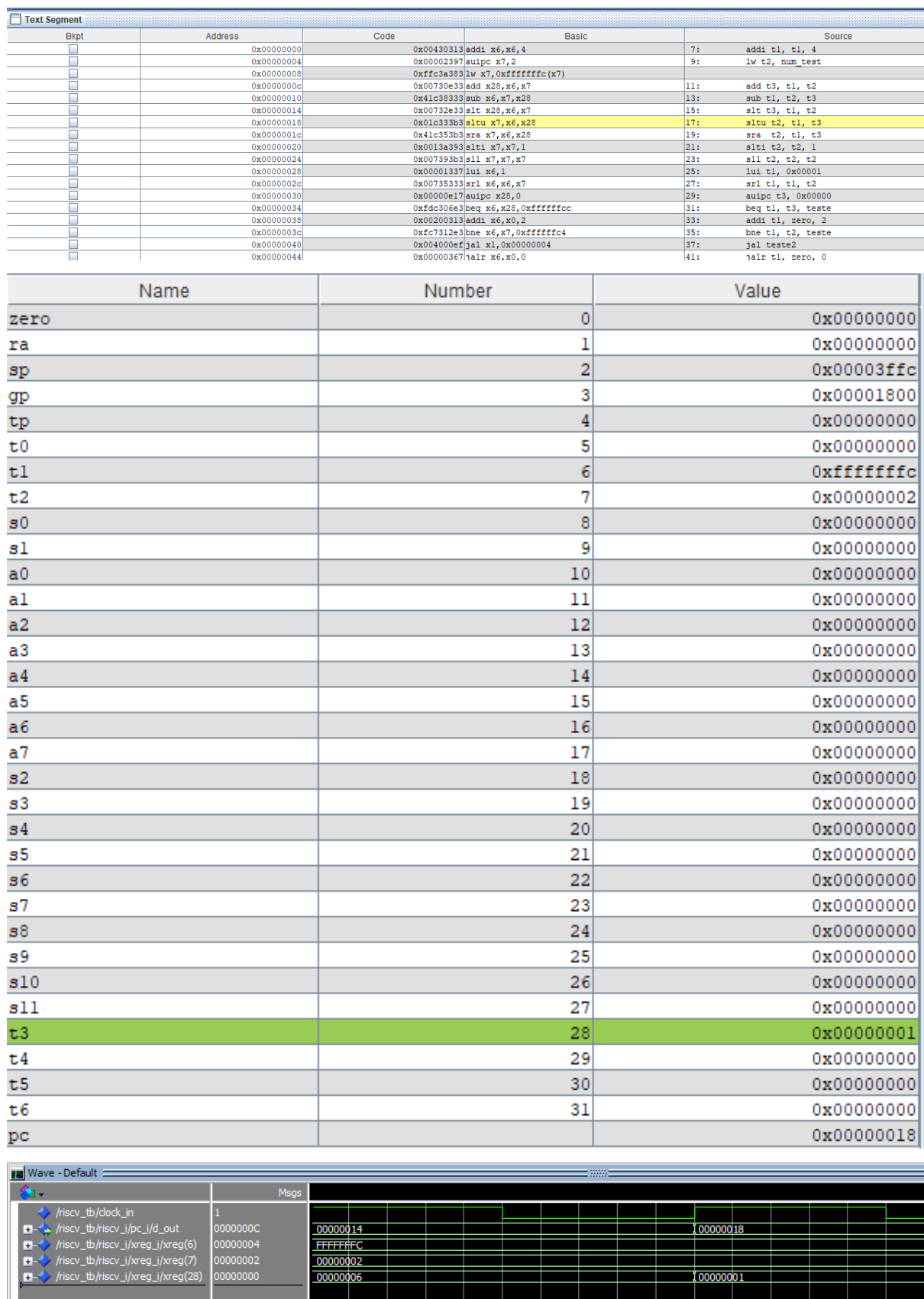


Figura 3.7: execução da instrução sltu t2, t1, t3; estado dos registradores; formas de ondas obtidas.

Bkpt	Address	Code	Basic	Source
	0x00000000	0x00430313	addi x6,x6,4	7: addi t1, t1, 4
	0x00000004	0x00002397	auipc x7,2	9: lw t2, num_test
	0x00000008	0xfff03a383	lw x7,0xfffffff0(x7)	
	0x0000000c	0x00730e33	add x28,x6,x7	11: add t3, t1, t2
	0x00000010	0x41c38333	sub x6,x7,x28	13: sub t1, t2, t3
	0x00000014	0x00732e33	sllt x28,x6,x7	15: sllt t3, t1, t2
	0x00000018	0x01c333b3	slltu x7,x6,x28	17: slltu t2, t1, t3
	0x0000001c	0x41c353b3	sra x7,x6,x28	19: sra t2, t1, t3
	0x00000020	0x0013a393	sllti x7,x7,1	21: sllti t2, t2, 1
	0x00000024	0x007393b3	sll x7,x7,x7	23: sll t2, t2, t2
	0x00000028	0x00001337	lui x6,1	25: lui t1, 0x00001
	0x0000002c	0x00735333	srl x6,x6,x7	27: srl t1, t1, t2
	0x00000030	0x00000e17	auipc x28,0	29: auipc t3, 0x00000
	0x00000034	0xfdc306e3	beq x6,x28,0xfffffff0	31: beq t1, t3, teste
	0x00000038	0x00200313	addi x6,x0,2	33: addi t1, zero, 2
	0x0000003c	0xfc7312e3	bne x6,x7,0xfffffff4	35: bne t1, t2, teste
	0x00000040	0x004000ef	jal x1,0x00000004	37: jal teste2
	0x00000044	0x00000367	jair x6,x0,0	41: jair t1, zero, 0

Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003fff
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0xfffffff0
t2	7	0x00000000
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000001
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x0000001c

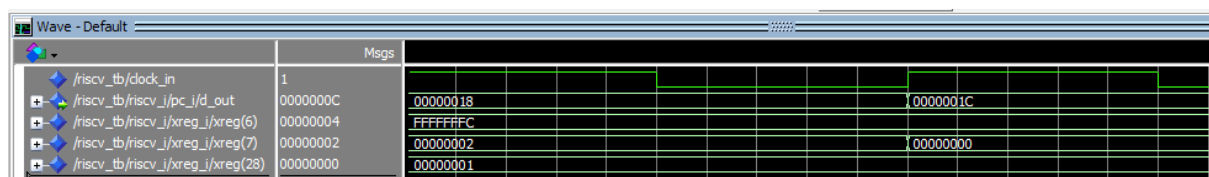


Figura 3.8: execução da instrução sra t2, t1, t3; estado dos registradores; formas de ondas obtidas.

Text Segment					
Brpt	Address	Code	Basic	Source	
	0x00000000	0x00430313	addi x6,x6,4	7:	addi t1, t1, 4
	0x00000004	0x00002397	auipc x7,2	9:	lw t2, num_test
	0x00000008	0xffc3a393	lw x7,0xfffffff(x7)		
	0x0000000c	0x00730e33	add x28,x6,x7	11:	add t3, t1, t2
	0x00000010	0x41c38333	sub x6,x7,x28	13:	sub t1, t2, t3
	0x00000014	0x00732e33	slt x28,x6,x7	15:	slt t3, t1, t2
	0x00000018	0x01c33b3b	sltu x7,x6,x28	17:	sltu t2, t1, t3
	0x0000001c	0x41c35b3b	sra x7,x6,x28	19:	sra t2, t1, t3
	0x00000020	0x0013a393	slti x7,x7,1	21:	slti t2, t2, 1
	0x00000024	0x00739b3b	sll x7,x7,x7	23:	sll t2, t2, t2
	0x00000028	0x00001337	lui x6,1	25:	lui t1, 0x00001
	0x0000002c	0x00735333	srl x6,x6,x7	27:	srl t1, t1, t2
	0x00000030	0x00000e17	auipc x28,0	29:	auipc t3, 0x00000
	0x00000034	0xfdc30e3b	beq x6,x28,0xfffffff	31:	beq t1, t3, teste
	0x00000038	0x00200313	addi x6,x0,2	33:	addi t1, zero, 2
	0x0000003c	0xfc7312e3	bne x6,x7,0xffffffc4	35:	bne t1, t2, teste
	0x00000040	0x004000ef	jal x1,0x00000004	37:	jal teste2
	0x00000044	0x00000367	jalr x6,x0,0	41:	jalr t1, zero, 0

Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0xfffffff
t2	7	0xffffffe
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000001
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000020

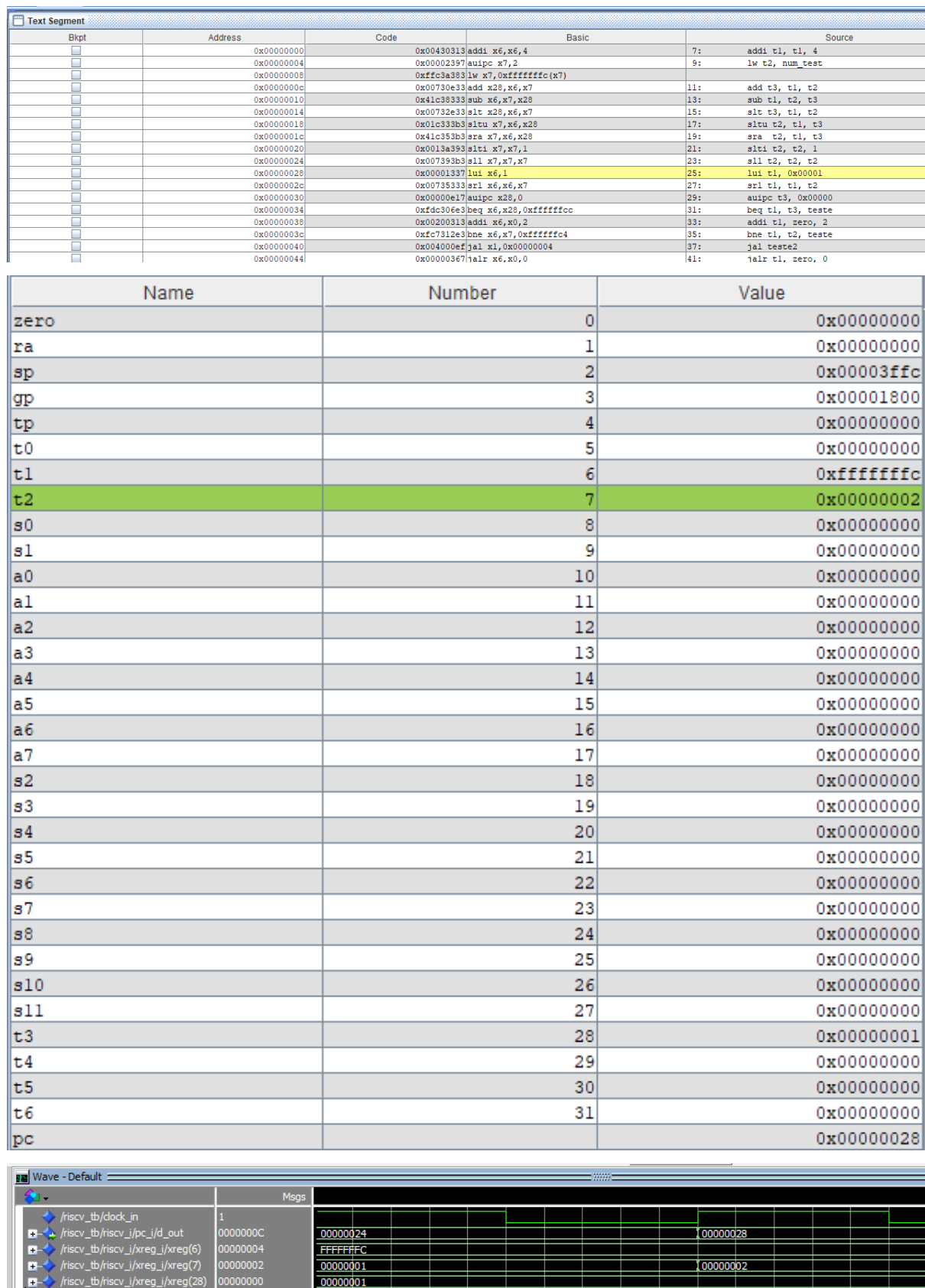
Wave - Default		Msgs
<div> <div>/riscv_tb/clock_in</div> <div>/riscv_tb/riscv_i/pc_i/d_out</div> <div>/riscv_tb/riscv_i/xreg_i/xreg(6)</div> <div>/riscv_tb/riscv_i/xreg_i/xreg(7)</div> <div>/riscv_tb/riscv_i/xreg_i/xreg(28)</div> </div>	1	
	0000000C	0000001C
	00000004	FFFFFFFC
	00000002	00000000
	00000000	00000001

Text Segment					
Bkpt	Address	Code	Basic	Source	
<input type="checkbox"/>	0x00000000	0x00430313 addi x6,x6,4		7:	addi t1, t1, 4
<input type="checkbox"/>	0x00000004	0x00002397 auipc x7,2		9:	lw t2, num_test
<input type="checkbox"/>	0x00000008	0xffc3a383 lw x7,0xfffffff(x7)			
<input type="checkbox"/>	0x0000000c	0x00730e33 add x28,x6,x7		11:	add t3, t1, t2
<input type="checkbox"/>	0x00000010	0x41c38333 sub x6,x7,x28		13:	sub t1, t2, t3
<input type="checkbox"/>	0x00000014	0x00732e33 slt x28,x6,x7		15:	slt t3, t1, t2
<input type="checkbox"/>	0x00000018	0x01c33b3b situ x7,x6,x28		17:	situ t2, t1, t3
<input type="checkbox"/>	0x0000001c	0x41c35b3b sra x7,x6,x28		19:	sra t2, t1, t3
<input type="checkbox"/>	0x00000020	0x0013a393 slli x7,x7,1		21:	slli t2, t2, 1
<input type="checkbox"/>	0x00000024	0x00739b3b sll x7,x7,x7		23:	sll t2, t2, t2
<input type="checkbox"/>	0x00000028	0x00001337 lui x6,1		25:	lui t1, 0x00001
<input type="checkbox"/>	0x0000002c	0x00735333 srl x6,x6,x7		27:	srl t1, t1, t2
<input type="checkbox"/>	0x00000030	0x00000e17 auipc x28,0		29:	auipc t3, 0x00000
<input type="checkbox"/>	0x00000034	0xfdc30e3b beq x6,x28,0xfffffffcc		31:	beq t1, t3, teste
<input type="checkbox"/>	0x00000038	0x00200313 addi x6,x0,2		33:	addi t1, zero, 2
<input type="checkbox"/>	0x0000003c	0xfc7312e3 bne x6,x7,0xfffffffcc4		35:	bne t1, t2, teste
<input type="checkbox"/>	0x00000040	0x004000ef jal x1,0x00000004		37:	jal teste2
<input type="checkbox"/>	0x00000044	0x00000367 jalr x6,x0,0		41:	jalr t1, zero, 0

Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0xffffffffc
t2	7	0x00000001
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000001
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000024

Wave - Default		Msgs
/riscv_tb/clock_in	1	
/riscv_tb/riscv_i/pc_i/d_out	0000000C	00000020
/riscv_tb/riscv_i/xreg_i/xreg(6)	00000004	FFFFFFFFC
/riscv_tb/riscv_i/xreg_i/xreg(7)	00000002	FFFFFFFE
/riscv_tb/riscv_i/xreg_i/xreg(28)	00000000	00000001

Figura 3.9: execução da instrução sll t2, t2, t2; estado dos registradores; formas de ondas obtidas.



**Figura 3.10:** execução da instrução lui t1, x00000; estado dos registradores; formas de ondas obtidas.



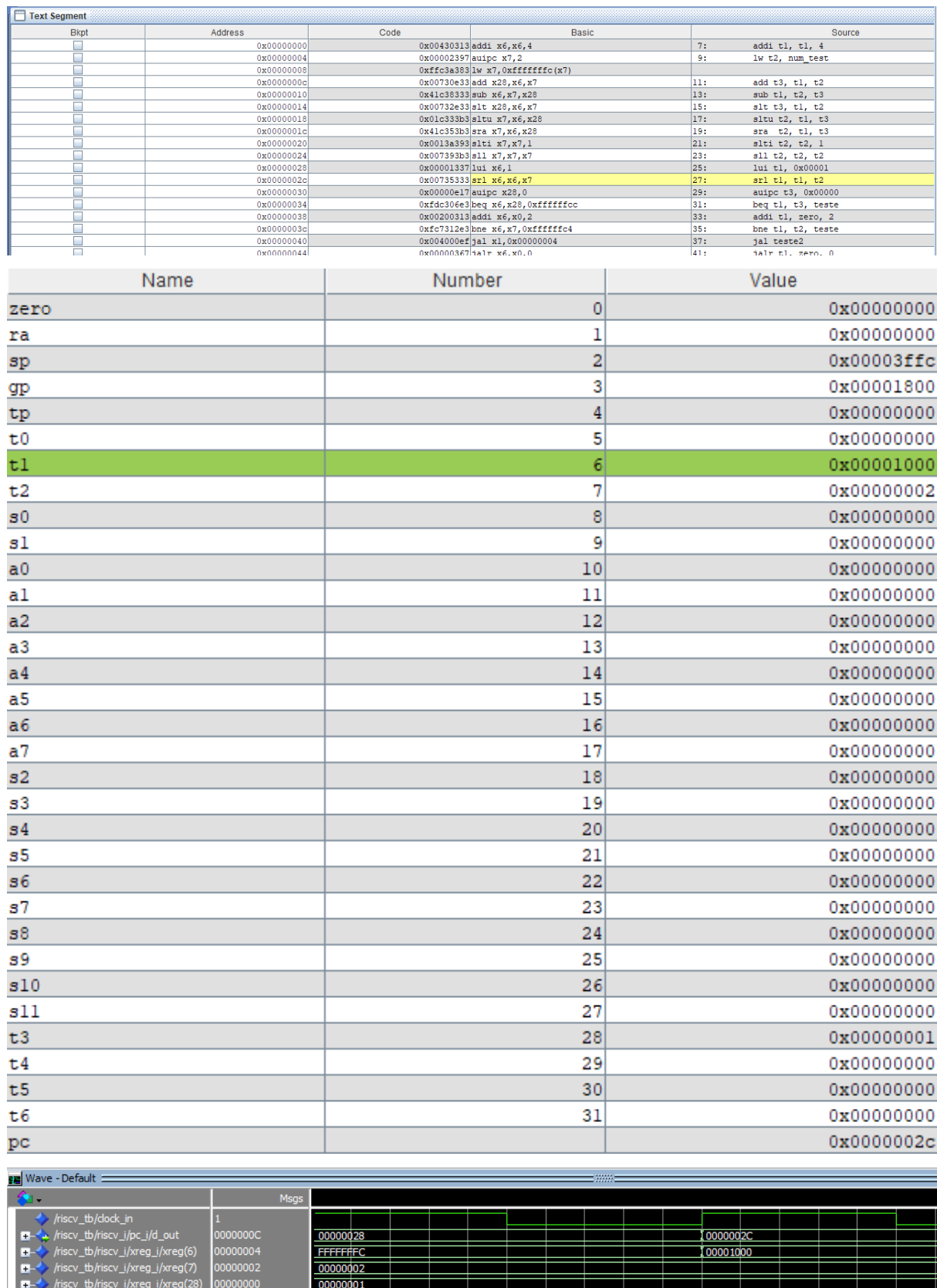
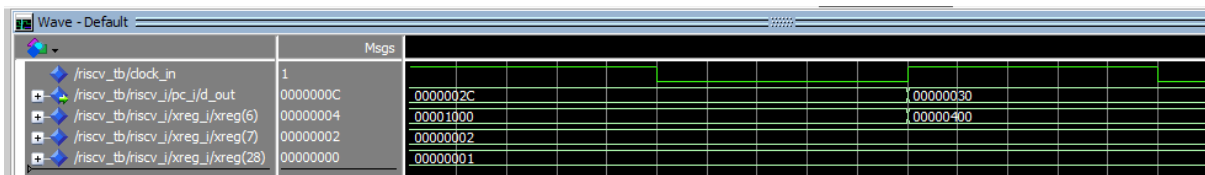


Figura 3.11: execução da instrução srl t1, t1, t2; estado dos registradores; formas de ondas obtidas.

Text Segment					
Bkpt	Address	Code	Basic	Source	
<input type="checkbox"/>	0x00000000	0x00430313	addi x6,x6,4	7:	addi t1, t1, 4
<input type="checkbox"/>	0x00000004	0x00002397	auipc x7,2	9:	lw t2, num_test
<input type="checkbox"/>	0x00000008	0xffc3a383	lw x7,0xfffffff(x7)		
<input type="checkbox"/>	0x0000000c	0x00730e33	add x28,x6,x7	11:	add t3, t1, t2
<input type="checkbox"/>	0x00000010	0x41c38333	sub x6,x7,x28	13:	sub t1, t2, t3
<input type="checkbox"/>	0x00000014	0x00732e33	slt x28,x6,x7	15:	slt t3, t1, t2
<input type="checkbox"/>	0x00000018	0x01c333b3	sltu x7,x6,x28	17:	sltu t2, t1, t3
<input type="checkbox"/>	0x0000001c	0x41c353b3	sra x7,x6,x28	19:	sra t2, t1, t3
<input type="checkbox"/>	0x00000020	0x0013a393	slti x7,x7,1	21:	slti t2, t2, 1
<input type="checkbox"/>	0x00000024	0x007393b3	sll x7,x7,x7	23:	sll t2, t2, t2
<input type="checkbox"/>	0x00000028	0x00001337	lui x6,1	25:	lui t1, 0x00001
<input type="checkbox"/>	0x0000002c	0x00735333	srl x6,x6,x7	27:	srl t1, t1, t2
<input type="checkbox"/>	0x00000030	0x00000e17	auipc x28,0	29:	auipc t3, 0x00000
<input type="checkbox"/>	0x00000034	0xfdc306e3	beq x6,x28,0xfffffffcc	31:	beq t1, t3, teste
<input type="checkbox"/>	0x00000038	0x00200313	addi x6,x0,2	33:	addi t1, zero, 2
<input type="checkbox"/>	0x0000003c	0xfc7312e3	bne x6,x7,0xfffffffcc4	35:	bne t1, t2, teste
<input type="checkbox"/>	0x00000040	0x004000ef	jal x1,0x00000004	37:	jal teste2
<input type="checkbox"/>	0x00000044	0x00000367	jair x6,x0,0	41:	jair t1, zero, 0

Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0x00000400
t2	7	0x00000002
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000001
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000030



**Figura 3.12:** execução da instrução `auipc t3, 0x00000`; estado dos registradores; formas de ondas obtidas.

Text Segment				
Bkpt	Address	Code	Basic	Source
	0x00000000	0x00403013	addi x6,x6,4	7: addi t1, t1, 4
	0x00000004	0x00002397	auipc x7,2	9: lw t2, num_test
	0x00000008	0xffff3a383	lw x7,0xfffffff0(x7)	
	0x0000000c	0x00730e33	add x28,x6,x7	11: add t3, t1, t2
	0x00000010	0x41c38333	sub x6,x7,x28	13: sub t1, t2, t3
	0x00000014	0x00732e33	slt x28,x6,x7	15: slt t3, t1, t2
	0x00000018	0x01c33b33	sltu x7,x6,x28	17: sltu t2, t1, t3
	0x0000001c	0x41c353b3	sra x7,x6,x28	19: sra t2, t1, t3
	0x00000020	0x0013a393	slli x7,x7,1	21: slli t2, t2, 1
	0x00000024	0x007393b3	slli x7,x7,x7	23: slli t2, t2, t2
	0x00000028	0x00001337	lui x6,1	25: lui t1, 0x00001
	0x0000002c	0x00735333	srl x6,x6,x7	27: srl t1, t1, t2
	0x00000030	0x00000e17	auipc x28,0	29: auipc t3, 0x00000
	0x00000034	0xfdc30ee3	beq x6,x28,0xfffffff0	31: beq t1, t3, teste
	0x00000038	0x00200313	addi x6,x0,2	33: addi t1, zero, 2
	0x0000003c	0xfc7312e3	bne x6,x7,0xfffffff0	35: bne t1, t2, teste
	0x00000040	0x004000ef	jai x1,0x00000004	37: jai teste2
	0x00000044	0x00000000		39: jai t1, zero, 0

Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0x00000400
t2	7	0x00000002
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000030
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000034

Wave - Default		Msgs
/riscv_tb/dock_in	1	
/riscv_tb/riscv_i/pc_i/d_out	0000000C	00000030
/riscv_tb/riscv_i/xreg_i/xreg(6)	00000004	00000400
/riscv_tb/riscv_i/xreg_i/xreg(7)	00000002	00000002
/riscv_tb/riscv_i/xreg_i/xreg(28)	00000000	00000001
		00000030

**Figura 3.13:** execução da instrução beq t1, t3, teste; estado dos registradores; formas de ondas obtidas.

Text Segment					
Bkpt	Address	Code	Basic	Source	
<input type="checkbox"/>	0x00000000	0x00430313	addi x6,x6,4	7:	addi t1, t1, 4
<input type="checkbox"/>	0x00000004	0x00002397	auipc x7,2	9:	lw t2, num_test
<input type="checkbox"/>	0x00000008	0xffc3a383	lw x7,0xfffffff(x7)		
<input type="checkbox"/>	0x0000000c	0x00730e33	add x28,x6,x7	11:	add t3, t1, t2
<input type="checkbox"/>	0x00000010	0x41c38333	sub x6,x7,x28	13:	sub t1, t2, t3
<input type="checkbox"/>	0x00000014	0x00732e33	slt x28,x6,x7	15:	slt t3, t1, t2
<input type="checkbox"/>	0x00000018	0x01c33b3b	sltu x7,x6,x28	17:	sltu t2, t1, t3
<input type="checkbox"/>	0x0000001c	0x41c353b3	sra x7,x6,x28	19:	sra t2, t1, t3
<input type="checkbox"/>	0x00000020	0x0013a393	slti x7,x7,1	21:	slti t2, t2, 1
<input type="checkbox"/>	0x00000024	0x007393b3	sll x7,x7,1	23:	sll t2, t2, t2
<input type="checkbox"/>	0x00000028	0x00001337	lui x6,1	25:	lui t1, 0x00001
<input type="checkbox"/>	0x0000002c	0x00735333	srl x6,x6,x7	27:	srl t1, t1, t2
<input type="checkbox"/>	0x00000030	0x00000e17	auipc x28,0	29:	auipc t3, 0x00000
<input type="checkbox"/>	0x00000034	0xfdc30e3	beq x6,x28,0xfffffff	31:	beq t1, t3, teste
<input type="checkbox"/>	0x00000038	0x00200313	addi x6,x0,2	33:	addi t1, zero, 2
<input type="checkbox"/>	0x0000003c	0xfc7312e3	bne x6,x7,0xfffffff4	35:	bne t1, t2, teste
<input type="checkbox"/>	0x00000040	0x004000ef	jal x1,0x00000004	37:	jal teste2
<input type="checkbox"/>	0x00000044	0x00000367	jair x6,x0,0	41:	jair t1, zero, 0

Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0x00000400
t2	7	0x00000002
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000030
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000038

Wave - Default		Msgs
/riscv_tb/dock_in	1	
/riscv_tb/riscv_i/pc_i/d_out	0000000C	00000034
/riscv_tb/riscv_i/xreg_i/xreg(6)	00000004	00000400
/riscv_tb/riscv_i/xreg_i/xreg(7)	00000002	00000002
/riscv_tb/riscv_i/xreg_i/xreg(28)	00000000	00000030

Figura 3.13: execução de outra instrução addi; estado dos registradores; formas de ondas obtidas.

Text Segment					
Bkpt	Address	Code	Basic	Source	
<input type="checkbox"/>	0x00000000	0x00430313 addi x6,x6,4		7:	addi t1, t1, 4
<input type="checkbox"/>	0x00000004	0x00002397 auipc x7,2		9:	lw t2, num_test
<input type="checkbox"/>	0x00000008	0xffc3a383 lw x7,0xfffffff(x7)			
<input type="checkbox"/>	0x0000000c	0x00730e33 add x28,x6,x7		11:	add t3, t1, t2
<input type="checkbox"/>	0x00000010	0x41c38333 sub x6,x7,x28		13:	sub t1, t2, t3
<input type="checkbox"/>	0x00000014	0x00732e33 slt x28,x6,x7		15:	slt t3, t1, t2
<input type="checkbox"/>	0x00000018	0x01c333b3 sltu x7,x6,x28		17:	sltu t2, t1, t3
<input type="checkbox"/>	0x0000001c	0x41c353b3 sra x7,x6,x28		19:	sra t2, t1, t3
<input type="checkbox"/>	0x00000020	0x0013a393 slti x7,x7,1		21:	slti t2, t2, 1
<input type="checkbox"/>	0x00000024	0x007393b3 sll x7,x7,x7		23:	sll t2, t2, t2
<input type="checkbox"/>	0x00000028	0x00001337 lui x6,1		25:	lui t1, 0x00001
<input type="checkbox"/>	0x0000002c	0x00735333 srl x6,x6,x7		27:	srl t1, t1, t2
<input type="checkbox"/>	0x00000030	0x00000e17 auipc x28,0		29:	auipc t3, 0x00000
<input type="checkbox"/>	0x00000034	0xfdc306e3 beq x6,x28,0xfffffffcc		31:	beq t1, t3, teste
<input type="checkbox"/>	0x00000038	0x00200313 addi x6,x0,2		33:	addi t1, zero, 2
<input type="checkbox"/>	0x0000003c	0xfc7312e3 bne x6,x7,0xfffffff4		35:	bne t1, t2, teste
<input type="checkbox"/>	0x00000040	0x004000ef jal x1,0x00000004		37:	jal teste2
<input type="checkbox"/>	0x00000044	0x00000367 jalr x6,x0,0		41:	jalr t1, zero, 0

Registers	Floating Point	Control and Status	
Name		Number	Value
zero		0	0x00000000
ra		1	0x00000000
sp		2	0x00003ffc
gp		3	0x00001800
tp		4	0x00000000
t0		5	0x00000000
t1		6	0x00000002
t2		7	0x00000002
s0		8	0x00000000
s1		9	0x00000000
a0		10	0x00000000
a1		11	0x00000000
a2		12	0x00000000
a3		13	0x00000000
a4		14	0x00000000
a5		15	0x00000000
a6		16	0x00000000
a7		17	0x00000000
s2		18	0x00000000
s3		19	0x00000000
s4		20	0x00000000
s5		21	0x00000000
s6		22	0x00000000
s7		23	0x00000000
s8		24	0x00000000
s9		25	0x00000000
s10		26	0x00000000
s11		27	0x00000000
t3		28	0x00000030
t4		29	0x00000000
t5		30	0x00000000
t6		31	0x00000000
pc			0x0000003c

Wave - Default			Msgs													
			1													
/riscv_tb/dock_in																
/riscv_tb/riscv_i/pc_i/d_out			0000000C													
/riscv_tb/riscv_i/xreg_i/xreg(6)			00000004													
/riscv_tb/riscv_i/xreg_i/xreg(7)			00000002													
/riscv_tb/riscv_i/xreg_i/xreg(28)			00000000													
				00000038										0000003C		
				00000400										00000002		
				00000002												
				00000030												

**Figura 3.14:** execução da instrução bne t1, t2, teste; estado dos registradores; formas de ondas obtidas.

Text Segment					
Bkpt	Address	Code	Basic	Source	
<input type="checkbox"/>	0x00000000	0x00430313	addi x6,x6,4	7:	addi t1, t1, 4
<input type="checkbox"/>	0x00000004	0x00002397	auipc x7,2	9:	lw t2, num_test
<input type="checkbox"/>	0x00000008	0xffc3a383	lw x7,0xfffffff(x7)		
<input type="checkbox"/>	0x0000000c	0x00730e33	add x28,x6,x7	11:	add t3, t1, t2
<input type="checkbox"/>	0x00000010	0x41c38333	sub x6,x7,x28	13:	sub t1, t2, t3
<input type="checkbox"/>	0x00000014	0x00732e33	slt x28,x6,x7	15:	slt t3, t1, t2
<input type="checkbox"/>	0x00000018	0x01c333b3	sltu x7,x6,x28	17:	sltu t2, t1, t3
<input type="checkbox"/>	0x0000001c	0x41c353b3	sra x7,x6,x28	19:	sra t2, t1, t3
<input type="checkbox"/>	0x00000020	0x0013a393	slti x7,x7,1	21:	slti t2, t2, 1
<input type="checkbox"/>	0x00000024	0x007393b3	sll x7,x7	23:	sll t2, t2, t2
<input type="checkbox"/>	0x00000028	0x00001337	lui x6,1	25:	lui t1, 0x00001
<input type="checkbox"/>	0x0000002c	0x00735333	srl x6,x6,x7	27:	srl t1, t1, t2
<input type="checkbox"/>	0x00000030	0x00000e17	auipc x28,0	29:	auipc t3, 0x00000
<input type="checkbox"/>	0x00000034	0xfdc30e3	beq x6,x28,0xfffffff	31:	beq t1, t3, teste
<input type="checkbox"/>	0x00000038	0x00200313	addi x6,x0,2	33:	addi t1, zero, 2
<input type="checkbox"/>	0x0000003c	0xfc7312e3	bne x6,x7,0xfffffff4	35:	bne t1, t2, teste
<input type="checkbox"/>	0x00000040	0x004000ef	jal x1,0x00000004	37:	jal teste2
<input type="checkbox"/>	0x00000044	0x00000367	jalr x6,x0,0	41:	jalr t1, zero, 0

Registers	Floating Point	Control and Status
Name	Number	Value
zero	0	0x00000000
ra	1	0x00000000
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0x00000002
t2	7	0x00000002
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000030
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000040

Wave - Default			Msgs	
/riscv_tb/dock_in	1	0000000C	0000003C	00000040
/riscv_tb/riscv_i/pc_i/d_out	00000004	00000002	00000002	00000030
/riscv_tb/riscv_i/xreg_i/xreg(6)	00000002	00000000		
/riscv_tb/riscv_i/xreg_i/xreg(7)	00000000			
/riscv_tb/riscv_i/xreg_i/xreg(28)				

**Figura 3.15:** execução da instrução jal zero, teste2; estado dos registradores; formas de ondas obtidas.

Text Segment					
Bkpt	Address	Code	Basic	Source	
<input type="checkbox"/>	0x00000000	0x00430313	addi x6,x6,4	7:	addi t1, t1, 4
<input type="checkbox"/>	0x00000004	0x00002397	auipc x7,2	9:	lw t2, num_test
<input type="checkbox"/>	0x00000008	0xffc3a383	lw x7,0xfffffff0(x7)		
<input type="checkbox"/>	0x0000000c	0x00730e33	add x28,x6,x7	11:	add t3, t1, t2
<input type="checkbox"/>	0x00000010	0x41c38333	sub x6,x7,x28	13:	sub t1, t2, t3
<input type="checkbox"/>	0x00000014	0x00732e33	slt x28,x6,x7	15:	slt t3, t1, t2
<input type="checkbox"/>	0x00000018	0x01c333b3	sltu x7,x6,x28	17:	sltu t2, t1, t3
<input type="checkbox"/>	0x0000001c	0x41c353b3	sra x7,x6,x28	19:	sra t2, t1, t3
<input type="checkbox"/>	0x00000020	0x0013a393	slti x7,x7,1	21:	slti t2, t2, 1
<input type="checkbox"/>	0x00000024	0x007393b3	sll x7,x7,x7	23:	sll t2, t2, t2
<input type="checkbox"/>	0x00000028	0x00001337	lui x6,1	25:	lui t1, 0x00001
<input type="checkbox"/>	0x0000002c	0x00735333	srl x6,x6,x7	27:	srl t1, t1, t2
<input type="checkbox"/>	0x00000030	0x00000e17	auipc x28,0	29:	auipc t3, 0x00000
<input type="checkbox"/>	0x00000034	0xfdc30e33	beq x6,x28,0xfffffff0	31:	beq t1, t3, teste
<input type="checkbox"/>	0x00000038	0x00200313	addi x6,x0,2	33:	addi t1, zero, 2
<input type="checkbox"/>	0x0000003c	0xfc7312e3	bne x6,x7,0xfffffff4	35:	bne t1, t2, teste
<input type="checkbox"/>	0x00000040	0x004000ef	jal x1,0x00000004	37:	jal teste2
<input type="checkbox"/>	0x00000044	0x00000367	jalr x6,x0,0	41:	jalr t1, zero, 0

Registers	Floating Point	Control and Status
Name	Number	Value
zero	0	0x00000000
ra	1	0x00000044
sp	2	0x00003ffc
gp	3	0x00001800
tp	4	0x00000000
t0	5	0x00000000
t1	6	0x00000002
t2	7	0x00000002
s0	8	0x00000000
s1	9	0x00000000
a0	10	0x00000000
a1	11	0x00000000
a2	12	0x00000000
a3	13	0x00000000
a4	14	0x00000000
a5	15	0x00000000
a6	16	0x00000000
a7	17	0x00000000
s2	18	0x00000000
s3	19	0x00000000
s4	20	0x00000000
s5	21	0x00000000
s6	22	0x00000000
s7	23	0x00000000
s8	24	0x00000000
s9	25	0x00000000
s10	26	0x00000000
s11	27	0x00000000
t3	28	0x00000030
t4	29	0x00000000
t5	30	0x00000000
t6	31	0x00000000
pc		0x00000044

Wave - Default									
		Msgs							
/riscv_tb/clock_in		1							
+	/riscv_tb/riscv_i/pc_i/d_out	0000000C	00000040					00000044	
+	/riscv_tb/riscv_i/xreg_i/xreg(6)	00000004	00000002						
+	/riscv_tb/riscv_i/xreg_i/xreg(7)	00000002	00000002						
+	/riscv_tb/riscv_i/xreg_i/xreg(28)	00000000	00000030						

**Figura 3.16:** execução da instrução `jalr t1, zero, 0`; estado dos registradores; formas de ondas obtidas.