IARISHI KATARI

🤳 9891299486 💌 emarishikataria2000@gmail.com 🛗 linkedin.com/in/emarishi-kataria-18185a23a

Education

Indira Gandhi Delhi Technical University For Women

M. Tech in VLSI Design - 7.285

Aug. 2021-July.2023 New Delhi, Delhi

Delhi Technical Campus (GGSIPU), G. Noida

B. Tech in Electrical and Electronics -8.19

Aug. 2017-July.2021

Experience/Internship

3ST Technologies Pvt Ltd

Aug 2023 - Present(1.5 years)

Design Verification Trainee

South Delhi, Delhi

Noida, UP

- Design Verification Trainee in 3ST worked on Verilog, SV, UVM, Digital electronics and STA
- Also, exposure to various protocols like UART, FIFO, AMBA APB

NIELIT.Noida Aug 2024 - Oct 2024

RTL to GDS Intern Hybrid

- Exposure to RTL to GDS-II qflow
- Worked on Various opensource tools like iverilog, openSTA, Yosys
- Hands on experience to open source tools, Basic Linux commands

Projects

AMBA APB | Verilog Sept 2024

- AMBA advanced microcontroller bus architecture APB Advanced Peripheral bus,
- The simulation results show that the data read from a particular memory location is same as the data written to the given memory location.

FIFO | Verilog, SVAug 2024

- Read and write operation use different clock frequencies
- FIFO synchronize data flow between two systems working on different clocks.

UART(Universal Asynchronous Receiver Transmitter) | Verilog, 3ST

Sept 2023

- Asynchronous data transfer protocol. (Implemented using Verilog)
- Various baud rate for synchronization

Washing Machine Controller | M. Tech

2023

washing machine controller using verilog various parameters using FSM Start Stop Rinse, Wash

Technical Skills

Languages: Verilog, System Verilog, UVM, C++(OOPS), Linux(basic commands)

Tools: Questasim, EDA playground, Ubuntu, Synopsys VCS, Yosys, Iverilog, Xilinx Vivado,

Technologies/Frameworks: Linux

Publication

International Conference Analysis of optical and electronic properties of MoS2 and WSe2 using first principle WREC,NIT Jalandhar