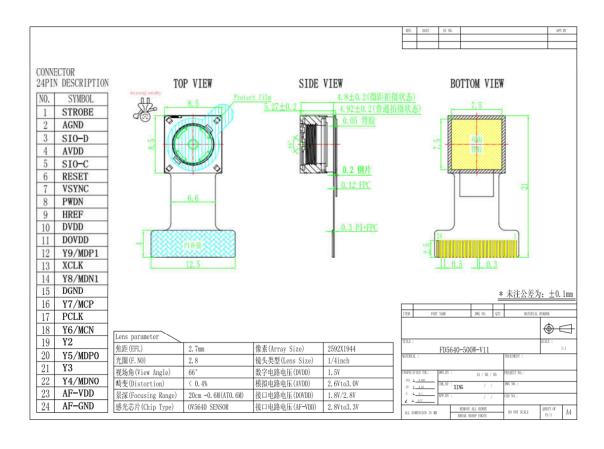
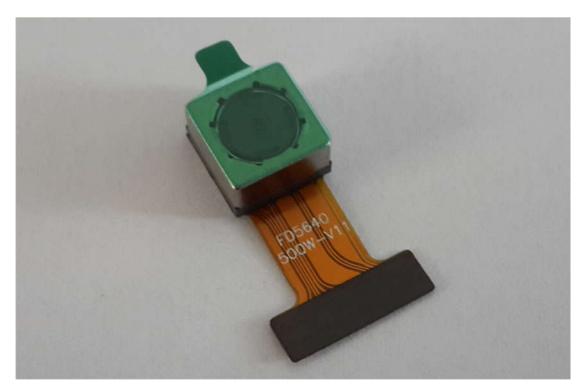
OV5640 模组结构图



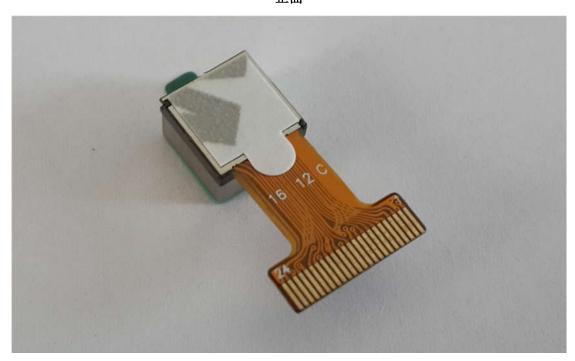
0V5640 模组引脚说明

Name	Туре	Description	Name	Туре	Description
STROBE	I/O	Strobe output	XCLK1	Input	System clock input
AGND	Ground	Ground for analog circuit	Y6	I/O	Video port output bit[6] Default: Input Note: There is no internal pull-up/pull-down resistor.
SIO_D	1/0	SCCB serial interface data I/O	DGND	Groun d	Ground for digital video port
AVDD	Power	Power for analog circuit	Y5	I/O	Video port output bit[5] Default: Input Note: There is no internal pull-up/pull-down resistor.
SIO_C	Input	SCCB serial interface clock input Note: There is no internal pull-up/pull-down resistor.	PCLK	I/O	Pixel clock output Default: Input Note: There is no internal pull-up/pull-down resistor.
RESET	Functio n (Default = 0)	Clears all registers and resets them to heir default values. Active low, internal pull-down resistor.	Y4	I/O	Video port output bit[4] Default: Input Note: There is no internal pull-up/pull-down resistor.
VSYNC	1/0	Vertical synchronization output Default: Input Note: There is no internal pull-up/pull-down resistor.	Y0	1/0	Video port output bit[0] Default: Input Note: There is no internal pull-up/pull-down resistor.
PWDN	Input	Power-down mode enable, active high Note: There is an internal pull-down resistor.	Y3	1/0	Video port output bit[3] Default: Input Note: There is no internal pull-up/pull-down resistor.
HREF	1/0	Horizontal reference output Default: Input Note: There is no internal pull-up/pull-down resistor.	Y1	I/O	Video port output bit[1] Default: Input Note: There is no internal pull-up/pull-down resistor.
DVDD	Power	Sensor digital power (Core)	Y2	1/0	Video port output bit[2] Default: Input Note: There is no internal pull-up/pull-down resistor.
DOVDD	Power	Power for digital video port	AF-VDD	-	Automatic zoom power
Y7	I/Ot	Video port output bit[7] Default: Input Note: There is no internal pull-up/pull-down resistor.	AF-GND	٠.	Automatic zoom power ground

OV5640 模组实物图



正面



背面(24PIN,引脚间距为 0.5MM)