CMOS VLSI Design

A Circuits and Systems Perspective

Fourth Edition

CMOS VLSI Design

A Circuits and Systems Perspective

Fourth Edition

Neil H. E. Weste

Macquarie University and The University of Adelaide

David Money Harris

Harvey Mudd College

Addison-Wesley

Boston Columbus Indianapolis New York San Francisco Upper Saddle River Amsterdam Cape Town Dubai London Madrid Milan Munich Paris Montreal Toronto Delhi Mexico City Sao Paulo Sydney Hong Kong Seoul Singapore Taipei Tokyo Editor in Chief: Michael Hirsch Acquisitions Editor: Matt Goldstein Editorial Assistant: Chelsea Bell Managing Editor: Jeffrey Holcomb

Senior Production Project Manager: Marilyn Lloyd

Media Producer: Katelyn Boller Director of Marketing: Margaret Waples Marketing Coordinator: Kathryn Ferranti Senior Manufacturing Buyer: Carol Melville Senior Media Buyer: Ginny Michaud

Text Designer: Susan Raymond
Art Director, Cover: Linda Knowles

Cover Designer: Joyce Cosentino Wells/J Wells Design

Cover Image: Cover photograph courtesy of Nick Knupffer—Intel Corporation.

Copyright © 2009 Intel Corporation. All rights reserved.

Full Service Vendor: Gillian Hall/The Aardvark Group Publishing Service

Copyeditor: Kathleen Cantwell, C4 Technologies

Proofreader: Holly McLean-Aldis

Indexer: Jack Lewis

Printer/Binder: Edwards Brothers

Cover Printer: Lehigh-Phoenix Color/Hagerstown

Credits and acknowledgments borrowed from other sources and reproduced with permission in this textbook appear on appropriate page within text or on page 838.

The interior of this book was set in Adobe Caslon and Trade Gothic.

Copyright © 2011, 2005, 1993, 1985 Pearson Education, Inc., publishing as Addison-Wesley. All rights reserved. Manufactured in the United States of America. This publication is protected by Copyright, and permission should be obtained from the publisher prior to any prohibited reproduction, storage in a retrieval system, or transmission in any form or by any means, electronic, mechanical, photocopying, recording, or likewise. To obtain permission(s) to use material from this work, please submit a written request to Pearson Education, Inc., Permissions Department, 501 Boylston Street, Suite 900, Boston, Massachusetts 02116.

Many of the designations by manufacturers and sellers to distinguish their products are claimed as trademarks. Where those designations appear in this book, and the publisher was aware of a trademark claim, the designations have been printed in initial caps or all caps.

Cataloging-in-Publication Data is on file with the Library of Congress.

Addison-Wesley is an imprint of



10 9 8 7 6 5 4 3 2 1—EB—14 13 12 11 10 ISBN 10: 0-321-54774-8 ISBN 13: 978-0-321-54774-3

To Avril, Melissa, Tamara, Nicky, Jocelyn, Makayla, Emily, Danika, Dan and Simon N. W.

To Jennifer, Samuel, and Abraham D. M. H.

Contents

Preface xxv

Cha	pter 1	Introduction
1.1	A Brief	History
1.2	Preview	
1.3	MOS Tr	ansistors
1.4	CMOS I	Logic9
	1.4.1	The Inverter 9
	1.4.2	The NAND Gate 9
	1.4.3	CMOS Logic Gates 9
	1.4.4	The NOR Gate 11
	1.4.5	Compound Gates 11
	1.4.6	Pass Transistors and Transmission Gates 12
	1.4.7	Tristates 14
	1.4.8	Multiplexers 15
	1.4.9	Sequential Circuits 16
1.5	CMOS I	Fabrication and Layout
	1.5.1	Inverter Cross-Section 19
	1.5.2	Fabrication Process 20
	1.5.3	Layout Design Rules 24
	1.5.4	Gate Layouts 27
	1.5.5	Stick Diagrams 28
1.6	Design	Partitioning
	1.6.1	Design Abstractions 30
	1.6.2	Structured Design 31
	1.6.3	Behavioral, Structural, and Physical Domains 31
1.7	Exampl	e: A Simple MIPS Microprocessor
	1.7.1	MIPS Architecture 33
	1.7.2	Multicycle MIPS Microarchitectures 34
1.8	Logic D	esign
	1.8.1	Top-Level Interfaces 38
	1.8.2	Block Diagrams 38
	1.8.3	Hierarchy 40
	1.8.4	Hardware Description Languages 40
1.9	Circuit	Design

1.10	Physical Design
	1.10.3 Pitch Matching 501.10.4 Slice Plans 501.10.5 Arrays 51
	1.10.6 Area Estimation 51
	Design Verification
	Pabrication, Packaging, and Testing
	nmary and a Look Ahead 55
Exer	rcises 57
Cha	apter 2 MOS Transistor Theory
2.1	Introduction
2.2	Long-Channel I-V Characteristics
2.3	C-V Characteristics
	2.3.1 Simple MOS Capacitance Models 68
	2.3.2 Detailed MOS Gate Capacitance Model 70
	2.3.3 Detailed MOS Diffusion Capacitance Model 72
2.4	Nonideal I-V Effects
	2.4.1 Mobility Degradation and Velocity Saturation 752.4.2 Channel Length Modulation 78
	2.4.3 Threshold Voltage Effects 79
	2.4.4 Leakage 80
	2.4.5 Temperature Dependence 852.4.6 Geometry Dependence 86
	2.4.7 Summary 86
2.5	DC Transfer Characteristics
	2.5.1 Static CMOS Inverter DC Characteristics 88
	2.5.2 Beta Ratio Effects 90
	2.5.3 Noise Margin 912.5.4 Pass Transistor DC Characteristics 92
2.6	Pitfalls and Fallacies
Sum	nmary 94
	rcises 95
_,.01	
Cha	apter 3 CMOS Processing Technology
3.1	Introduction
3.2	CMOS Technologies
	3.2.1 Wafer Formation 100
	3.2.2 Photolithography 101

	3.2.3 3.2.4 3.2.5	Well and Channel Formation 103 Silicon Dioxide (SiO ₂) 105 Isolation 106
	3.2.6 3.2.7 3.2.8 3.2.9 3.2.10	Gate Oxide 107 Gate and Source/Drain Formations 108 Contacts and Metallization 110 Passivation 112
3.3	3.3.1 3.3.2 3.3.3 3.3.4	Design Rules
3.4	3.4.1 3.4.2 3.4.3 3.4.4	Process Enhancements
3.5	Technol 3.5.1 3.5.2	Design Rule Checking (DRC) 131 Circuit Extraction 132
3.6	Manufa 3.6.1 3.6.2 3.6.3 3.6.4 3.6.5	Antenna Rules 133 Layer Density Rules 134 Resolution Enhancement Rules 134 Metal Slotting Rules 135 Yield Enhancement Guidelines 135
3.7 3.8		and Fallacies
Sumr Exerc	mary 13 sises 13	
Cha	pter 4	Delay
4.1	Introdu 4.1.1 4.1.2	Ction
4.2 4.3	RC Dela 4.3.1 4.3.2 4.3.3 4.3.4	nt Response
	4.3.5	Elmore Delay 150

	4.3.6 4.3.7	Layout Dependence of Capacitance 153 Determining Effective Resistance 154
4.4	Linear	Delay Model
	4.4.1	Logical Effort 156
	4.4.2	Parasitic Delay 156
	4.4.3	Delay in a Logic Gate 158
	4.4.4	Drive 159
	4.4.5 4.4.6	Extracting Logical Effort from Datasheets 159 Limitations to the Linear Delay Model 160
4 5		•
4.5		Effort of Paths
	4.5.1 4.5.2	Delay in Multistage Logic Networks 163 Choosing the Best Number of Stages 166
	4.5.3	Example 168
	4.5.4	Summary and Observations 169
	4.5.5	Limitations of Logical Effort 171
	4.5.6	Iterative Solutions for Sizing 171
4.6	Timing	Analysis Delay Models
	4.6.1	Slope-Based Linear Model 173
	4.6.2	Nonlinear Delay Model 174
	4.6.3	Current Source Model 174
4.7		and Fallacies
4.8	Historia	cal Perspective
Sumi	mary 1	76
Exerc	cises 1'	76
Cha	pter 5	Power
5.1	Introdu	ction
5.1	5.1.1	Definitions 182
	5.1.2	Examples 182
	5.1.3	Sources of Power Dissipation 184
5.2	Dvnami	c Power
	5.2.1	Activity Factor 186
	5.2.2	Capacitance 188
	5.2.3	Voltage 190
	5.2.4	Frequency 192
	5.2.5	Short-Circuit Current 193
	5.2.6	Resonant Circuits 193
5.3		Power
	5.3.1	Static Power Sources 194
	5.3.2 5.3.3	Power Gating 197 Multiple Threshold Voltages and Oxide Thicknesses 199
	0.010	1.13.14pt 1110011016 Totalgeo and Onide Internetioned 177

	5.3.4 5.3.5	Variable Threshold Voltages 199 Input Vector Control 200
5.4	Energ	gy-Delay Optimization
	5.4.1	Minimum Energy 200
	5.4.2	Minimum Energy-Delay Product 203
	5.4.3	Minimum Energy Under a Delay Constraint 203
5.5		Power Architectures
	5.5.1 5.5.2	Microarchitecture 204 Porallelism and Binelining 204
	5.5.3	
5.6		Is and Fallacies
		rical Perspective
Sumn		209
Exerci		209
Exerci	ises	209
Chai	ntor	6 Interconnect
Ulla		6 Interconnect
6.1	Introd	duction
	6.1.1	Wire Geometry 211
	6.1.2	Example: Intel Metal Stacks 212
6.2		connect Modeling
	6.2.1 6.2.2	
	6.2.3	
	6.2.4	
	6.2.5	Temperature Dependence 220
6.3	Interd	connect Impact
	6.3.1	Delay 220
	6.3.2	27
	6.3.3 6.3.4	
	6.3.5	An Aside on Effective Resistance and Elmore Delay 227
6.4	Interd	connect Engineering
	6.4.1	Width, Spacing, and Layer 229
	6.4.2	Repeaters 230
	6.4.3 6.4.4	Crosstalk Control 232 Low-Swing Signaling 234
	6.4.5	Regenerators 236
6.5	Logic	al Effort with Wires
6.6		Is and Fallacies
Sumn		238
Exerci		238

Cha	pter 7	Robustness
7.1	Introdu	uction
7.2	Variabi 7.2.1 7.2.2 7.2.3 7.2.4	Supply Voltage 2 Temperature 242 Process Variation Design Corners
7.3	7.3.1 7.3.2 7.3.3 7.3.4 7.3.5 7.3.6	Reliability Termino Oxide Wearout 2 Interconnect Wear Soft Errors 251 Overvoltage Failur Latchup 253
7.4		Transistor Scaling Interconnect Scalin International Tech Impacts on Design
7.5	7.5.1 7.5.2	Properties of Rand Variation Sources
7.6	7.5.3 Variation 7.6.1 7.6.2	Variation Impacts on-Tolerant Design Adaptive Control Fault Tolerance
7.7		and Fallacies
7.8	Histori	cal Perspective
	cises 2	.84 .84
	•	Circuit Simu
8.1 8.2		uction
5.1	8.2.1 8.2.2 8.2.3 8.2.4 8.2.5 8.2.6	Sources and Passiv Transistor DC An Inverter Transient Subcircuits and M Optimization 29

8.3	Device	Models
	8.3.1	Level 1 Models 299
	8.3.2	Level 2 and 3 Models 300
	8.3.3	BSIM Models 300
	8.3.4 8.3.5	Diffusion Capacitance Models 300
8.4		Design Corners 302 Characterization
0.4	8.4.1	I-V Characteristics 303
	8.4.2	Threshold Voltage 306
	8.4.3	Gate Capacitance 308
	8.4.4	Parasitic Capacitance 308
	8.4.5	Effective Resistance 310
	8.4.6	Comparison of Processes 311
	8.4.7	Process and Environmental Sensitivity 313
8.5		Characterization
	8.5.1 8.5.2	Path Simulations 313
	8.5.3	DC Transfer Characteristics 315 Logical Effort 315
	8.5.4	Power and Energy 318
	8.5.5	Simulating Mismatches 319
	8.5.6	Monte Carlo Simulation 319
8.6	Interco	nnect Simulation
8.7	Pitfalls	and Fallacies
Sumi	mary 3	24
Exerc	cises 3	24
\circ		
Cha	pter 9	Combinational Circuit Design
9.1	Introdu	ction
9.2	Circuit	Families
	9.2.1	Static CMOS 329
	9.2.2	Ratioed Circuits 334
	9.2.3 9.2.4	Cascode Voltage Switch Logic 339 Dynamic Circuits 339
	9.2.5	Pass-Transistor Circuits 349
9.3		Pitfalls
3.3	9.3.1	Threshold Drops 355
	9.3.2	Ratio Failures 355
	9.3.3	Leakage 356
	9.3.4	Charge Sharing 356
	9.3.5	Power Supply Noise 356
	9.3.6	Hot Spots 357

			Minority Carrier Injection 357 Back-Gate Coupling 358 Diffusion Input Noise Sensitivity 358 Process Sensitivity 358 Example: Domino Noise Budgets 359
WEB BIHANCED	9.4	More Ci	rcuit Families
	9.5	Silicon-	On-Insulator Circuit Design
		9.5.1 9.5.2 9.5.3 9.5.4 9.5.5	Floating Body Voltage 361 SOI Advantages 362 SOI Disadvantages 362 Implications for Circuit Styles 363 Summary 364
	9.6	9.6.1 9.6.2	eshold Circuit Design
	9.7	Pitfalls	and Fallacies
	9.8	Historic	cal Perspective
	Sumr	mary 30	59
		•	O Sequential Circuit Design
	10.2	10.2.1 10.2.2 10.2.3 10.2.4	Cing Static Circuits
	10.3	10.3.1 10.3.2 10.3.3 10.3.4 10.3.5 10.3.6 10.3.7 10.3.8 10.3.9 10.3.10	Design of Latches and Flip-Flops
	ENHANCED	10.3.11	True Single-Phase-Clock (TSPC) Latches and Flip-Flops 402
	10.4	Static S 10.4.1 10.4.2	Sequencing Element Methodology

		 10.4.3 State Retention Registers 408 10.4.4 Level-Converter Flip-Flops 408 10.4.5 Design Margin and Adaptive Sequential Elements 409
	ENHANCED	10.4.6 Two-Phase Timing Types 411
ENHANCED	10.5	Sequencing Dynamic Circuits
	10.6	Synchronizers
		10.6.1 Metastability 412
		10.6.2 A Simple Synchronizer 41510.6.3 Communicating Between Asynchronous Clock Domains 416
		10.6.4 Common Synchronizer Mistakes 417
		10.6.5 Arbiters 419
	10.7	10.6.6 Degrees of Synchrony 419 Wave Pipelining
		Pitfalls and Fallacies
ENHANCED		Case Study: Pentium 4 and Itanium 2 Sequencing Methodologies 423
ENHANCED		
	Sumr	nary 423 ises 425
	Exerc	1585 423
	Cha	pter 11 Datapath Subsystems
	11.1	Introduction
	11.2	Addition/Subtraction
		11.2.1 Single-Bit Addition 430
		11.2.2 Carry-Propagate Addition 434 11.2.3 Subtraction 458
		11.2.4 Multiple-Input Addition 458
		11.2.5 Flagged Prefix Adders 459
	11.3	One/Zero Detectors
	11.4	Comparators
		11.4.1 Magnitude Comparator 46211.4.2 Equality Comparator 462
		11.4.3 $K = A + B$ Comparator 463
	11.5	Counters
		11.5.1 Binary Counters 464
		11.5.2 Fast Binary Counters 465
		11.5.3 Ring and Johnson Counters 46611.5.4 Linear-Feedback Shift Registers 466
	116	Boolean Logical Operations
		Coding
	,	11.7.1 Parity 468
		11.7.2 Error-Correcting Codes 468
		11.7.3 Gray Codes 470
		11.7.4 XOR/XNOR Circuit Forms 471

11.8	Shifters	5
	11.8.1	Funnel Shifter 473
		Barrel Shifter 475
	11.8.3	Alternative Shift Functions 476
11.9		cation
		Unsigned Array Multiplication 478
	11.9.2	Two's Complement Array Multiplication 479 Booth Encoding 480
	11.9.3 11 9 4	Column Addition 485
		Final Addition 489
		Fused Multiply-Add 490
ENHANCED.	11.9.7	Serial Multiplication 490
	11.9.8	Summary 490
11.10	Parallel	-Prefix Computations
11.11	Pitfalls	and Fallacies
Sumr	mary 49	94
Exerc	ises 49	94
Cha	ntor 1	2 Array Subsystems
Ulla	•	2 Array Subsystems
12.1	Introdu	ction
12.2	SRAM	
		SRAM Cells 499
		Row Circuitry 506
		Column Circuitry 510 Multi-Ported SRAM and Register Files 514
		Large SRAMs 515
		Low-Power SRAMs 517
	12.2.7	Area, Delay, and Power of RAMs and Register Files 520
12.3	DRAM	522
	12.3.1	
		Column Circuitry 525
		Embedded DRAM 526
12.4		nly Memory
	12.4.1	Programmable ROMs 529 NAND ROMs 530
		Flash 531
12 5		Access Memories
12.5	12.5.1	Shift Registers 533
	12.5.1	Queues (FIFO, LIFO) 533
12.6		t-Addressable Memory
12.7		nmable Logic Arrays
	-0.511	

12.8.1 Redundancy 541 12.8.2 Error Correcting Codes (ECC) 543 12.8.3 Radiation Hardening 543 12.9 Historical Perspective
12.8.3 Radiation Hardening 543 12.9 Historical Perspective 544 Summary 545 Exercises 546 Chapter 13 Special-Purpose Subsystems 13.1 Introduction 549 13.2 Packaging and Cooling 549 13.2.1 Package Options 549 13.2.2 Chip-to-Package Connections 551 13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3 Power Distribution 555 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 Lid/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.4.1 Definitions 566 13.4.2 Clocks 566 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Generation 569 13.4.5 Local Clock Gaters 575
12.9 Historical Perspective 544 Summary 545 Exercises 546 Chapter 13 Special-Purpose Subsystems 13.1 Introduction 549 13.2 Packaging and Cooling 549 13.2.1 Package Options 549 13.2.2 Chip-to-Package Connections 551 13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3 Power Distribution 555 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.4.1 Definitions 566 13.4.2 Clocks 566 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Generation 571 13.4.5 Local Clock Gaters 575
Summary 545 Exercises 546 Chapter 13 Special-Purpose Subsystems 13.1 Introduction
Exercises 546 Chapter 13 Special-Purpose Subsystems 13.1 Introduction 549 13.2 Packaging and Cooling 549 13.2.1 Package Options 549 13.2.2 Chip-to-Package Connections 551 13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3 Power Distribution 555 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation
Chapter 13 Special-Purpose Subsystems 13.1 Introduction
13.1 Introduction 549 13.2 Packaging and Cooling 549 13.2.1 Package Options 549 13.2.2 Chip-to-Package Connections 551 13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3.1 On-Chip Power Distribution Network 556 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 566 13.4.1 Definitions 566 13.4.2 Clocks System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.1 Introduction 549 13.2 Packaging and Cooling 549 13.2.1 Package Options 549 13.2.2 Chip-to-Package Connections 551 13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3.1 On-Chip Power Distribution Network 556 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 566 13.4.1 Definitions 566 13.4.2 Clocks System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.1 Introduction 549 13.2 Packaging and Cooling 549 13.2.1 Package Options 549 13.2.2 Chip-to-Package Connections 551 13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3.1 On-Chip Power Distribution Network 556 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 566 13.4.1 Definitions 566 13.4.2 Clocks System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.2 Packaging and Cooling 549 13.2.1 Package Options 549 13.2.2 Chip-to-Package Connections 551 13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3 Power Distribution 555 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.2.1 Package Options 549 13.2.2 Chip-to-Package Connections 551 13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3 Power Distribution 555 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.2.2 Chip-to-Package Connections 551 13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3 Power Distribution 555 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.2.3 Package Parasitics 552 13.2.4 Heat Dissipation 552 13.2.5 Temperature Sensors 553 13.3 Power Distribution 555 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.2.5 Temperature Sensors 553 13.3 Power Distribution 555 13.3.1 On-Chip Power Distribution Network 556 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 559 13.3.5 Power Network Modeling 560 560 13.3.6 Power Supply Filtering 564 564 13.3.8 Substrate Noise 565 565 13.3.9 Energy Scavenging 565 566 13.4.1 Definitions 566 566 13.4.2 Clock System Architecture 568 568 13.4.3 Global Clock Generation 569 571 13.4.5 Local Clock Gaters 575 575
13.3 Power Distribution 555 13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.3.1 On-Chip Power Distribution Network 556 13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.3.2 IR Drops 557 13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.3.3 L di/dt Noise 558 13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.3.4 On-Chip Bypass Capacitance 559 13.3.5 Power Network Modeling 560 13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.3.6 Power Supply Filtering 564 13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4 Clocks 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.3.7 Charge Pumps 564 13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4 Clocks
13.3.8 Substrate Noise 565 13.3.9 Energy Scavenging 565 13.4 Clocks 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.4 Clocks
 13.4.1 Definitions 566 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
 13.4.2 Clock System Architecture 568 13.4.3 Global Clock Generation 569 13.4.4 Global Clock Distribution 571 13.4.5 Local Clock Gaters 575
13.4.3 Global Clock Generation 56913.4.4 Global Clock Distribution 57113.4.5 Local Clock Gaters 575
13.4.4 Global Clock Distribution 57113.4.5 Local Clock Gaters 575
13.4.5 Local Clock Gaters 575
13.4.6 Clock Skew Budgets 577
13.4.7 Adaptive Deskewing 579
13.5 PLLs and DLLs
13.5.1 PLLs 580 13.5.2 DLLs 587
13.5.3 Pitfalls 589
13.6 1/0
13.6.1 Basic I/O Pad Circuits 591
13.6.2 Electrostatic Discharge Protection 593
13.6.3 Example: MOSIS I/O Pads 59413.6.4 Mixed-Voltage I/O 596

13.7	High-Speed Links 597
	13.7.1 High-Speed I/O Channels 597
	13.7.2 Channel Noise and Interference 600
	13.7.3 High-Speed Transmitters and Receivers 601
	13.7.4 Synchronous Data Transmission 606
	13.7.5 Clock Recovery in Source-Synchronous Systems 606
	13.7.6 Clock Recovery in Mesochronous Systems 608
	13.7.7 Clock Recovery in Pleisochronous Systems 610
13.8	Random Circuits
10.0	13.8.1 True Random Number Generators 610
	13.8.2 Chip Identification 611
	•
13.9	Pitfalls and Fallacies
Sumr	mary 613
Exerc	cises 614
Cha	pter 14 Design Methodology and Tools
	Introduction
14.2	Structured Design Strategies
	14.2.1 A Software Radio—A System Example 618
	14.2.2 Hierarchy 620
	14.2.3 Regularity 623
	14.2.4 Modularity 625
	14.2.5 Locality 626
	14.2.6 Summary 627
14.3	Design Methods
	14.3.1 Microprocessor/DSP 627
	14.3.2 Programmable Logic 628
	14.3.3 Gate Array and Sea of Gates Design 631
	14.3.4 Cell-Based Design 632
	14.3.5 Full Custom Design 634
	14.3.6 Platform-Based Design—System on a Chip 635
	14.3.7 Summary 636
14.4	Design Flows
	14.4.1 Behavioral Synthesis Design Flow (ASIC Design Flow) 637
	14.4.2 Automated Layout Generation 641
	14.4.3 Mixed-Signal or Custom-Design Flow 645
14.5	Design Economics
14.0	14.5.1 Non-Recurring Engineering Costs (NREs) 647
	14.5.2 Recurring Costs 649
	14.5.3 Fixed Costs 650
	14.5.4 Schedule 651
	14.5.5 Personpower 653
	14.5.6 Project Management 653
	14.5.7 Design Reuse 654
	Design rease 05 i

	14.6	Data Sheets and Documentation
		 14.6.3 Description of Operation 655 14.6.4 DC Specifications 655 14.6.5 AC Specifications 656
		14.6.6 Package Diagram 65614.6.7 Principles of Operation Manual 65614.6.8 User Manual 656
WEB	14.7	CMOS Physical Design Styles
	14.8	Pitfalls and Fallacies
		stor 15 Tosting Dobugging and Varification
		pter 15 Testing, Debugging, and Verification
	15.1	Introduction
		15.1.3 Manufacturing Tests 664
	15.2	Testers, Test Fixtures, and Test Programs
		15.2.1 Testers and Test Fixtures 666
		15.2.2 Test Programs 668 15.2.3 Handlers 669
	15.3	Logic Verification Principles
		15.3.1 Test Vectors 670
		15.3.2 Testbenches and Harnesses 671
		15.3.3 Regression Testing 67115.3.4 Version Control 672
		15.3.5 Bug Tracking 673
	15.4	Silicon Debug Principles
	15.5	Manufacturing Test Principles
		15.5.1 Fault Models 677
		15.5.2 Observability 679
		15.5.3 Controllability 679 15.5.4 Repeatability 679
		15.5.5 Survivability 679
		15.5.6 Fault Coverage 680
		15.5.7 Automatic Test Pattern Generation (ATPG) 68015.5.8 Delay Fault Testing 680
	15.6	Design for Testability
		15.6.1 <i>Ad Hoc</i> Testing 681
		15.6.2 Scan Design 682
		15.6.3 Built-In Self-Test (BIST) 684 15.6.4 IDDQ Testing 687
		15.6.5 Design for Manufacturability 687
		•

ENHANCED	15.7 Boundary Scan					
	15.8 Testing in a University Environment					
	15.9 Pitfalls and Fallacies					
	Summary 697					
	Exerc	ises 69	97			
	aga	endix	A Hardware Description Languages			
	A.1		ction	699		
		A.1.1	Modules 700	0,,,		
		A.1.2	Simulation and Synthesis 701			
	A.2	Combin	national Logic	702		
		A.2.1	Bitwise Operators 702			
		A.2.2	Comments and White Space 703			
		A.2.3 A.2.4	Reduction Operators 703 Conditional Assignment 704			
		A.2.5	Internal Variables 706			
		A.2.6	Precedence and Other Operators 708			
		A.2.7 A.2.8				
			Bit Swizzling 711			
			Delays 712			
	A.3	Structu	ral Modeling	713		
	A.4 Sequential Logic		itial Logic	717		
		A.4.1	Registers 717			
		A.4.2	Resettable Registers 718			
		A.4.3 A.4.4	Enabled Registers 719 Multiple Registers 720			
		A.4.5	Latches 721			
		A.4.6	Counters 722			
		A.4.7	Shift Registers 724			
	A.5		national Logic with Always / Process Statements	724		
		A.5.1 A.5.2	Case Statements 726 If Statements 729			
		A.5.2	SystemVerilog Casez 731			
		A.5.4	Blocking and Nonblocking Assignments 731			
	A.6	Finite S	State Machines	735		
		A.6.1	FSM Example 735			
		A.6.2	State Enumeration 736			
	A 7	A.6.3	FSM with Inputs 738	740		
	A.7	TVDE 10	iosyncracies	740		

8.A	Parame	eterized Modules	. 742
A.9	Memor	٠	. 745
	A.9.2	RAM 745 Multiported Register Files 747 ROM 748	
A.10	Testber	nches	. 749
A.11	System	Verilog Netlists	. 754
A.12	Examp	e: MIPS Processor	. 755
	A.12.2	Testbench 756 SystemVerilog 757 VHDL 766	
Exerc	ises 7	76	

References 785

Index 817

Credits 838

Preface

In the two-and-a-half decades since the first edition of this book was published, CMOS technology has claimed the preeminent position in modern electrical system design. It has enabled the widespread use of wireless communication, the Internet, and personal computers. No other human invention has seen such rapid growth for such a sustained period. The transistor counts and clock frequencies of state-of-the-art chips have grown by orders of magnitude.

	1st Edition	2nd Edition	3rd Edition	4th Edition
Year	1985	1993	2004	2010
Transistor Counts	$10^5 - 10^6$	$10^6 - 10^7$	$10^8 - 10^9$	$10^9 - 10^{10}$
Clock Frequencies	10^{7}	108	109	10^{9}
Worldwide Market	\$25B	\$60B	\$170B	\$250B

This edition has been heavily revised to reflect the rapid changes in integrated circuit design over the past six years. While the basic principles are largely the same, power consumption and variability have become primary factors for chip design. The book has been reorganized to emphasize the key factors: delay, power, interconnect, and robustness. Other chapters have been reordered to reflect the order in which we teach the material.

How to Use This Book

This book intentionally covers more breadth and depth than any course would cover in a semester. It is accessible for a first undergraduate course in VLSI, yet detailed enough for advanced graduate courses and is useful as a reference to the practicing engineer. You are encouraged to pick and choose topics according to your interest. Chapter 1 previews the entire field, while subsequent chapters elaborate on specific topics. Sections are marked with the "Optional" icon (shown here in the margin) if they are not needed to understand subsequent sections. You may skip them on a first reading and return when they are relevant to you.

We have endeavored to include figures whenever possible ("a picture is worth a thousand words") to trigger your thinking. As you encounter examples throughout the text, we urge you to think about them before reading the solutions. We have also provided extensive references for those who need to delve deeper into topics introduced in this text. We



have emphasized the best practices that are used in industry and warned of pitfalls and fallacies. Our judgments about the merits of circuits may become incorrect as technology and applications change, but we believe it is the responsibility of a writer to attempt to call out the most relevant information.

Supplements

Numerous supplements are available on the Companion Web site for the book, www.cmosvlsi.com. Supplements to help students with the course include:

- A lab manual with laboratory exercises involving the design of an 8-bit microprocessor covered in Chapter 1.
- A collection of links to VLSI resources including open-source CAD tools and process parameters.
- A student solutions manual that includes answers to odd-numbered problems.
- Certain sections of the book moved online to shorten the page count. These sections are indicated by the "Web Enhanced" icon (shown here in the margin).

Supplements to help instructors with the course include:

- A sample syllabus.
- Lecture slides for an introductory VLSI course.
- An instructor's manual with solutions.

These materials have been prepared exclusively for professors using the book in a course. Please send email to computing@aw.com for information on how to access them.

Acknowledgments

We are indebted to many people for their reviews, suggestions, and technical discussions. These people include: Bharadwaj "Birdy" Amrutur, Mark Anders, Adnan Aziz, Jacob Baker, Kaustav Banerjee, Steve Bibyk, David Blaauw, Erik Brunvand, Neil Burgess, Wayne Burleson, Robert Drost, Jo Ebergen, Sarah Harris, Jacob Herbold, Ron Ho, David Hopkins, Mark Horowitz, Steven Hsu, Tanay Karnik, Omid Kaveh, Matthew Keeter, Ben Keller, Ali Keshavarzi, Brucek Khailany, Jaeha Kim, Volkan Kursun, Simon Knowles, Ram Krishnamurthy, Austin Lee, Ana Sonia Leon, Shih-Lien Lu, Sanu Mathew, Aleksandar Milenkovic, Sam Naffziger, Braden Phillips, Stefan Rusu, Justin Schauer, James Stine, Jason Stinson, Aaron Stratton, Ivan Sutherland, Jim Tschanz, Alice Wang, Gu-Yeon Wei, and Peiyi Zhao. We apologize in advance to anyone we overlooked.

MOSIS and IBM kindly provided permission to use nanometer SPICE models for many examples. Nathaniel Pinckney spent a summer revising the laboratory exercises and updating simulations. Jaeha Kim contributed new sections on phase-locked loops and high-speed I/O for Chapter 13. David would like to thank Bharadwaj Amrutur of the Indian Institute of Science and Braden Phillips of the University of Adelaide for hosting him during two productive summers of writing.



Addison-Wesley has done an admirable job with the grueling editorial and production process. We would particularly like to thank our editor, Matt Goldstein, and our compositor, Gillian Hall.

Sally Harris has been editing family books since David was an infant on her lap. She read the page proofs with amazing attention to detail and unearthed hundreds of errors.

This book would not have existed without the support of our families. David would particularly like to thank his wife Jennifer and sons Abraham and Samuel for enduring two summers of absence while writing, and to our extended family for their tremendous assistance.

We have become painfully aware of the ease with which mistakes creep into a book. Scores of 3rd edition readers have reported bugs that are now corrected. Despite our best efforts at validation, we are confident that we have introduced a similar number of new errors. Please check the errata sheet at www.cmosvlsi.com/errata.pdf to see if the bug has already been reported. Send your reports to bugs@cmosvlsi.com.

N. W. D. M. H. January 2010