Simulink Design Verifier Report

EB_12B

YUZEHONG

Simulink Design Verifier Report: EB_12B

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Chapter 1. Summary

Analysis Information.

Model:	EB_12B
Mode:	Test generation
Model Representation:	Built on 28-Aug-2021 14:18:56
Test generation target:	Model
Status:	Completed normally
PreProcessing Time:	9s
Analysis Time:	79s

Objectives Status.

Number of Objectives:	**6**
Objectives Satisfied:	5
Objectives Unsatisfiable:	1

Chapter 2. Analysis Information

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Model Information

File:	EB_12B
Version:	1.83
Time Stamp:	Fri Mar 22 01:03:25 2019
Author:	elliocm

Analysis Options

Mode:	TestGeneration
Rebuild Model Representation:	IfChangeIsDetected
Test generation target:	Model
Test Suite Optimization:	Auto
Maximum Testcase Steps:	10000time steps
Test Conditions:	UseLocalSettings
Test Objectives:	UseLocalSettings
Model Coverage Objectives:	ConditionDecision
Include Relational Boundary Objectives:	off
Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on
Save Data:	on
Save Harness:	off
Save Report:	off

Chapter 3. Test Objectives Status

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Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
1	Condition	EB/ridge/Relational Operator	RelationalOperator: input1 <= input2 **true**	78	2 [5]
2	Condition	EB/ridge/Relational Operator	RelationalOperator: input1 <= input2 **false**	5	1 [5]
4	Decision	EB/ridge/Switch1	trigger >= threshold **true (output is from 1st input port)**	5	1 [5]
5	Decision	EB/ridge/Switch	logical trigger input **false (output is from 3rd input port)**	5	1 [5]
6	Decision	EB/ridge/Switch	logical trigger input **true (output is from 1st input port)**	78	2 [5]

Objectives Unsatisfiable

Simulink Design Verifier found that there does not exist any test case exercising these test objectives. This often indicates the presence of dead logic in the model. Other possible reasons can be inactive blocks in the model due to parameter configuration or test constraints such as given using Test Condition blocks.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
3	Decision	EB/ridge/Switch1	trigger >= threshold **false (output is from 3rd input port)**	42	n/a

Chapter 4. Model Items

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This section presents, for each object in the model defining coverage objectives, the list of objectives and their individual status at the end of the analysis. It should match the coverage report obtained from running the generated test suite on the model, either from the harness model or by using the sldvruntest command.

EB/ridge/Relational Operator

#:	Type	Description	Status	Test Case
1	Condition	RelationalOperator: input1 <= input2 true	Satisfied	2 [5]
2	Condition	RelationalOperator: input1 <= input2 false	Satisfied	1 [5]

EB/ridge/Switch1

#:	Type	Description	Status	Test Case
3	Decision	trigger >= threshold false (output is from 3rd input port)	Unsatisfiable	n/a
4	Decision	trigger >= threshold true (output is from 1st input port)	Satisfied	1 [5]

EB/ridge/Switch

#:	Type	Description	Status	Test Case
5	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [5]
6	Decision	logical trigger input true (output is from 1st input port)	Satisfied	2 [5]

Chapter 5. Test Cases

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This section contains detailed information about each generated test case.

Test Case 1

Summary.

Length:	0 second (1 sample period)
Objectives Satisfied:	3

Objectives.

Step	Time	Model Item	Objectives
1	0	EB/ridge/Relational Operator EB/ridge/Switch EB/ridge/Switch1	RelationalOperator: input1 <= input2 false logical trigger input false (output is from 3rd input port) trigger >= threshold true (output is from 1st input port)

Generated Input Data.

Time	0
Step	1
B	[5.9566 1.9184 -5.4067 9.8142 -3.321 5.9365 -6.4012 2.414 -3.4756 2.6094 1.6229 -4.7853 1.162 -6.7752 -5.4024]

Test Case 2

Summary.

Length:	0 second (1 sample period)
Objectives Satisfied:	2

Objectives.

Step	Time	Model Item	Objectives
1	0	EB/ridge/Relational Operator EB/ridge/Switch	RelationalOperator: input1 <= input2 true

Step	Time	Model Item	Objectives
			logical trigger input true (output is from 1st input port)

Generated Input Data.

Time	**0**
Step	**1**
B	[0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0]