# Simulink Design Verifier Report

## bscfsm

### YUZEHONG

# Simulink Design Verifier Report: bscfsm

YUZEHONG

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# Chapter 1. Summary

**Analysis Information.**

| | |
|---|---|
| Model: | bscfsm |
| Mode: | Test generation |
| Model Representation: | Built on 28-Aug-2021 13:56:23 |
| Test generation target: | Model |
| Status: | Completed normally |
| PreProcessing Time: | 44s |
| Analysis Time: | 40s |

**Objectives Status.**

| | |
|---|---|
| **Number of Objectives:** | **80** |
| Objectives Satisfied: | 75 |
| Objectives Unsatisfiable: | 5 |

# Chapter 2. Analysis Information

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# Model Information

| | |
|---|---|
| File: | bscfsm |
| Version: | 1.102 |
| Time Stamp: | Sun Apr 08 01:43:19 2018 |
| Author: | elliocm |

# Analysis Options

| | |
|---|---|
| Mode: | TestGeneration |
| Rebuild Model Representation: | IfChangeIsDetected |
| Test generation target: | Model |
| Test Suite Optimization: | Auto |
| Maximum Testcase Steps: | 10000time steps |
| Test Conditions: | UseLocalSettings |
| Test Objectives: | UseLocalSettings |
| Model Coverage Objectives: | ConditionDecision |
| Include Relational Boundary Objectives: | off |
| Maximum Analysis Time: | 300s |
| Block Replacement: | off |
| Parameters Analysis: | off |
| Include expected output values: | off |
| Randomize data that do not affect the outcome: | off |
| Additional analysis to reduce instances of rational approximation: | on |
| Save Data: | on |
| Save Harness: | off |
| Save Report: | off |

# Chapter 3. Test Objectives Status

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# Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

| # | Type | Model Item | Description | Analysis Time (sec) | Test Case |
|---|---|---|---|---|---|
| 1 | Decision | FiniteStateMachine/Manager/Actions/If | input 1 "if" condition **true** | 21 | 1 [19] |
| 2 | Decision | FiniteStateMachine/Manager/Actions/If | input 1 "if" condition **false** | 21 | 1 [19] |
| 3 | Decision | FiniteStateMachine/Manager/Actions/If | input 2 "elseif" condition **true** | 21 | 1 [19] |
| 4 | Decision | FiniteStateMachine/Manager/Actions/If | input 2 "elseif" condition **false** | 21 | 1 [19] |
| 5 | Decision | FiniteStateMachine/Manager/Actions/If | input 3 "elseif" condition **true** | 21 | 1 [19] |
| 6 | Decision | FiniteStateMachine/Manager/Actions/If | input 3 "elseif" condition **false** | 21 | 1 [19] |
| 7 | Decision | FiniteStateMachine/Manager/Actions/If | input 4 "elseif" condition **true** | 21 | 1 [19] |
| 9 | Decision | FiniteStateMachine/Manager/Actions/Transition/Switch2 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 10 | Decision | FiniteStateMachine/Manager/Actions/Transition/Switch2 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 11 | Decision | FiniteStateMachine/Manager/Actions/Nominal/Switch2 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 12 | Decision | FiniteStateMachine/Manager/Actions/Nominal/Switch2 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 13 | Condition | FiniteStateMachine/Manager/Actions/Transition/Logical Operator12 | Logic: input port 1 **true** | 21 | 1 [19] |
| 14 | Condition | FiniteStateMachine/Manager/Actions/Transition/Logical Operator12 | Logic: input port 1 **false** | 21 | 1 [19] |

| # | Type | Model Item | Description | Analysis Time (sec) | Test Case |
|---|---|---|---|---|---|
| 15 | Condition | FiniteStateMachine/Manager/Actions/Transition/Logical Operator12 | Logic: input port 2 **true** | 21 | 1 [19] |
| 16 | Condition | FiniteStateMachine/Manager/Actions/Transition/Logical Operator12 | Logic: input port 2 **false** | 39 | 5 [23] |
| 17 | Condition | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator1 | Logic: input port 1 **true** | 21 | 1 [19] |
| 18 | Condition | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator1 | Logic: input port 1 **false** | 21 | 1 [19] |
| 19 | Condition | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator1 | Logic: input port 2 **true** | 21 | 1 [19] |
| 21 | Condition | FiniteStateMachine/Manager/Actions/Nominal/Logical Operator12 | Logic: input port 1 **true** | 21 | 1 [19] |
| 22 | Condition | FiniteStateMachine/Manager/Actions/Nominal/Logical Operator12 | Logic: input port 1 **false** | 37 | 4 [23] |
| 23 | Decision | FiniteStateMachine/Manager/Actions/Transition/Switch1 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 24 | Decision | FiniteStateMachine/Manager/Actions/Transition/Switch1 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 25 | Decision | FiniteStateMachine/Manager/Actions/Standby/Switch2 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 26 | Decision | FiniteStateMachine/Manager/Actions/Standby/Switch2 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 27 | Decision | FiniteStateMachine/Manager/Actions/Maneuver/Switch2 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 28 | Decision | FiniteStateMachine/Manager/Actions/Maneuver/Switch2 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 29 | Decision | FiniteStateMachine/Manager/Actions/Nominal/Switch1 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 30 | Decision | FiniteStateMachine/Manager/Actions/Nominal/Switch1 | logical trigger input **true (output is from 1st input port)** | 37 | 4 [23] |

| # | Type | Model Item | Description | Analysis Time (sec) | Test Case |
|---|---|---|---|---|---|
| 31 | Condition | FiniteStateMachine/Manager/Actions/Standby/Logical Operator12 | Logic: input port 1 **true** | 21 | 1 [19] |
| 32 | Condition | FiniteStateMachine/Manager/Actions/Standby/Logical Operator12 | Logic: input port 1 **false** | 21 | 1 [19] |
| 33 | Condition | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator12 | Logic: input port 1 **true** | 21 | 1 [19] |
| 34 | Condition | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator12 | Logic: input port 1 **false** | 21 | 1 [19] |
| 35 | Condition | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator12 | Logic: input port 2 **true** | 21 | 1 [19] |
| 37 | Decision | FiniteStateMachine/Manager/Actions/Standby/Switch1 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 38 | Decision | FiniteStateMachine/Manager/Actions/Standby/Switch1 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 39 | Decision | FiniteStateMachine/Manager/Actions/Maneuver/Switch1 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 40 | Decision | FiniteStateMachine/Manager/Actions/Maneuver/Switch1 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 41 | Decision | FiniteStateMachine/Manager/Output/If | input 1 "if" condition **true** | 21 | 1 [19] |
| 42 | Decision | FiniteStateMachine/Manager/Output/If | input 1 "if" condition **false** | 21 | 1 [19] |
| 43 | Decision | FiniteStateMachine/Manager/Output/If | input 2 "elseif" condition **true** | 21 | 1 [19] |
| 44 | Decision | FiniteStateMachine/Manager/Output/If | input 2 "elseif" condition **false** | 21 | 1 [19] |
| 45 | Decision | FiniteStateMachine/Manager/Output/If | input 3 "elseif" condition **true** | 21 | 1 [19] |
| 46 | Decision | FiniteStateMachine/Manager/Output/If | input 3 "elseif" condition **false** | 21 | 1 [19] |
| 47 | Decision | FiniteStateMachine/Manager/Output/If | input 4 "elseif" condition **true** | 21 | 1 [19] |
| 49 | Decision | FiniteStateMachine/Sen/Actions/If | input 1 "if" condition **true** | 21 | 1 [19] |

| # | Type | Model Item | Description | Analysis Time (sec) | Test Case |
|---|---|---|---|---|---|
| 50 | Decision | FiniteStateMachine/Sen/Actions/If | input 1 "if" condition **false** | 21 | 1 [19] |
| 51 | Decision | FiniteStateMachine/Sen/Actions/If | input 2 "elseif" condition **true** | 21 | 1 [19] |
| 52 | Decision | FiniteStateMachine/Sen/Actions/If | input 2 "elseif" condition **false** | 21 | 1 [19] |
| 53 | Decision | FiniteStateMachine/Sen/Actions/If | input 3 "elseif" condition **true** | 21 | 1 [19] |
| 55 | Decision | FiniteStateMachine/Sen/Actions/Nominal/Switch2 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 56 | Decision | FiniteStateMachine/Sen/Actions/Nominal/Switch2 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 57 | Condition | FiniteStateMachine/Sen/Actions/Transition/Logical Operator12 | Logic: input port 1 **true** | 21 | 1 [19] |
| 58 | Condition | FiniteStateMachine/Sen/Actions/Transition/Logical Operator12 | Logic: input port 1 **false** | 21 | 1 [19] |
| 59 | Condition | FiniteStateMachine/Sen/Actions/Transition/Logical Operator12 | Logic: input port 2 **true** | 21 | 1 [19] |
| 60 | Condition | FiniteStateMachine/Sen/Actions/Transition/Logical Operator12 | Logic: input port 2 **false** | 21 | 1 [19] |
| 61 | Condition | FiniteStateMachine/Sen/Actions/Nominal/Logical Operator12 | Logic: input port 1 **true** | 21 | 1 [19] |
| 62 | Condition | FiniteStateMachine/Sen/Actions/Nominal/Logical Operator12 | Logic: input port 1 **false** | 21 | 1 [19] |
| 63 | Condition | FiniteStateMachine/Sen/Actions/Fault/Logical Operator2 | Logic: input port 1 **true** | 29 | 2 [22] |
| 64 | Condition | FiniteStateMachine/Sen/Actions/Fault/Logical Operator2 | Logic: input port 1 **false** | 21 | 1 [19] |
| 65 | Decision | FiniteStateMachine/Sen/Actions/Transition/Switch1 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 66 | Decision | FiniteStateMachine/Sen/Actions/Transition/Switch1 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |

| # | Type | Model Item | Description | Analysis Time (sec) | Test Case |
|---|---|---|---|---|---|
| 67 | Decision | FiniteStateMachine/Sen/Actions/Nominal/Switch1 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 68 | Decision | FiniteStateMachine/Sen/Actions/Nominal/Switch1 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 69 | Condition | FiniteStateMachine/Sen/Actions/Fault/Logical Operator3 | Logic: input port 1 **true** | 21 | 1 [19] |
| 70 | Condition | FiniteStateMachine/Sen/Actions/Fault/Logical Operator3 | Logic: input port 1 **false** | 21 | 1 [19] |
| 71 | Condition | FiniteStateMachine/Sen/Actions/Fault/Logical Operator12 | Logic: input port 1 **true** | 21 | 1 [19] |
| 72 | Condition | FiniteStateMachine/Sen/Actions/Fault/Logical Operator12 | Logic: input port 1 **false** | 29 | 2 [22] |
| 73 | Condition | FiniteStateMachine/Sen/Actions/Fault/Logical Operator12 | Logic: input port 2 **true** | 29 | 2 [22] |
| 74 | Condition | FiniteStateMachine/Sen/Actions/Fault/Logical Operator12 | Logic: input port 2 **false** | 35 | 3 [22] |
| 75 | Decision | FiniteStateMachine/Sen/Actions/Fault/Switch1 | logical trigger input **false (output is from 3rd input port)** | 35 | 3 [22] |
| 76 | Decision | FiniteStateMachine/Sen/Actions/Fault/Switch1 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |
| 77 | Condition | FiniteStateMachine/Sen/Output/Relational Operator5 | RelationalOperator: input1 == input2 **true** | 21 | 1 [19] |
| 78 | Condition | FiniteStateMachine/Sen/Output/Relational Operator5 | RelationalOperator: input1 == input2 **false** | 21 | 1 [19] |
| 79 | Decision | FiniteStateMachine/Sen/Output/Switch2 | logical trigger input **false (output is from 3rd input port)** | 21 | 1 [19] |
| 80 | Decision | FiniteStateMachine/Sen/Output/Switch2 | logical trigger input **true (output is from 1st input port)** | 21 | 1 [19] |

# Objectives Unsatisfiable

Simulink Design Verifier found that there does not exist any test case exercising these test objectives. This often indicates the presence of dead logic in the model. Other possible reasons can be inactive blocks in the model due to parameter configuration or test constraints such as given using Test Condition blocks.

| # | Type | Model Item | Description | Analysis Time (sec) | Test Case |
|---|---|---|---|---|---|
| 8 | Decision | FiniteStateMachine/Manager/Actions/If | input 4 "elseif" condition **false** | 29 | n/a |
| 20 | Condition | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator1 | Logic: input port 2 **false** | 33 | n/a |
| 36 | Condition | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator12 | Logic: input port 2 **false** | 33 | n/a |
| 48 | Decision | FiniteStateMachine/Manager/Output/If | input 4 "elseif" condition **false** | 29 | n/a |
| 54 | Decision | FiniteStateMachine/Sen/Actions/If | input 3 "elseif" condition **false** | 29 | n/a |

# Chapter 4. Model Items

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This section presents, for each object in the model defining coverage objectives, the list of objectives and their individual status at the end of the analysis. It should match the coverage report obtained from running the generated test suite on the model, either from the harness model or by using the sldvruntest command.

# FiniteStateMachine/Manager/Actions/If

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 1 | Decision | input 1 "if" condition true | Satisfied | 1 [19] |
| 2 | Decision | input 1 "if" condition false | Satisfied | 1 [19] |
| 3 | Decision | input 2 "elseif" condition true | Satisfied | 1 [19] |
| 4 | Decision | input 2 "elseif" condition false | Satisfied | 1 [19] |

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 5 | Decision | input 3 "elseif" condition true | Satisfied | 1 [19] |
| 6 | Decision | input 3 "elseif" condition false | Satisfied | 1 [19] |
| 7 | Decision | input 4 "elseif" condition true | Satisfied | 1 [19] |
| 8 | Decision | input 4 "elseif" condition false | Unsatisfiable | n/a |

# FiniteStateMachine/Manager/Actions/Transition/Switch2

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 9 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 10 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Manager/Actions/Nominal/Switch2

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 11 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 12 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Manager/Actions/Transition/Logical Operator12

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 13 | Condition | Logic: input port 1 true | Satisfied | 1 [19] |
| 14 | Condition | Logic: input port 1 false | Satisfied | 1 [19] |

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 15 | Condition | Logic: input port 2 true | Satisfied | 1 [19] |
| 16 | Condition | Logic: input port 2 false | Satisfied | 5 [23] |

# FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator1

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 17 | Condition | Logic: input port 1 true | Satisfied | 1 [19] |
| 18 | Condition | Logic: input port 1 false | Satisfied | 1 [19] |
| 19 | Condition | Logic: input port 2 true | Satisfied | 1 [19] |
| 20 | Condition | Logic: input port 2 false | Unsatisfiable | n/a |

# FiniteStateMachine/Manager/Actions/Nominal/Logical Operator12

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 21 | Condition | Logic: input port 1 true | Satisfied | 1 [19] |
| 22 | Condition | Logic: input port 1 false | Satisfied | 4 [23] |

# FiniteStateMachine/Manager/Actions/Transition/Switch1

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 23 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 24 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Manager/Actions/Stand-by/Switch2

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 25 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 26 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Manager/Actions/Maneuver/Switch2

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 27 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 28 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Manager/Actions/Nominal/Switch1

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 29 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 30 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 4 [23] |

# FiniteStateMachine/Manager/Actions/Stand-by/Logical Operator12

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 31 | Condition | Logic: input port 1 true | Satisfied | 1 [19] |

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 32 | Condition | Logic: input port 1 false | Satisfied | 1 [19] |

# FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator12

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 33 | Condition | Logic: input port 1 true | Satisfied | 1 [19] |
| 34 | Condition | Logic: input port 1 false | Satisfied | 1 [19] |
| 35 | Condition | Logic: input port 2 true | Satisfied | 1 [19] |
| 36 | Condition | Logic: input port 2 false | Unsatisfiable | n/a |

# FiniteStateMachine/Manager/Actions/Standby/Switch1

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 37 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 38 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Manager/Actions/Maneuver/Switch1

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 39 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 40 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Manager/Output/If

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 41 | Decision | input 1 "if" condition true | Satisfied | 1 [19] |
| 42 | Decision | input 1 "if" condition false | Satisfied | 1 [19] |
| 43 | Decision | input 2 "elseif" condition true | Satisfied | 1 [19] |
| 44 | Decision | input 2 "elseif" condition false | Satisfied | 1 [19] |
| 45 | Decision | input 3 "elseif" condition true | Satisfied | 1 [19] |
| 46 | Decision | input 3 "elseif" condition false | Satisfied | 1 [19] |
| 47 | Decision | input 4 "elseif" condition true | Satisfied | 1 [19] |
| 48 | Decision | input 4 "elseif" condition false | Unsatisfiable | n/a |

# FiniteStateMachine/Sen/Actions/If

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 49 | Decision | input 1 "if" condition true | Satisfied | 1 [19] |
| 50 | Decision | input 1 "if" condition false | Satisfied | 1 [19] |
| 51 | Decision | input 2 "elseif" condition true | Satisfied | 1 [19] |
| 52 | Decision | input 2 "elseif" condition false | Satisfied | 1 [19] |
| 53 | Decision | input 3 "elseif" condition true | Satisfied | 1 [19] |
| 54 | Decision | input 3 "elseif" condition false | Unsatisfiable | n/a |

# FiniteStateMachine/Sen/Actions/Nominal/Switch2

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 55 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 56 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Sen/Actions/Transition/Logical Operator12

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 57 | Condition | Logic: input port 1 true | Satisfied | 1 [19] |
| 58 | Condition | Logic: input port 1 false | Satisfied | 1 [19] |
| 59 | Condition | Logic: input port 2 true | Satisfied | 1 [19] |
| 60 | Condition | Logic: input port 2 false | Satisfied | 1 [19] |

# FiniteStateMachine/Sen/Actions/Nominal/Logical Operator12

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 61 | Condition | Logic: input port 1 true | Satisfied | 1 [19] |
| 62 | Condition | Logic: input port 1 false | Satisfied | 1 [19] |

# FiniteStateMachine/Sen/Actions/Fault/Logical Operator2

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 63 | Condition | Logic: input port 1 true | Satisfied | 2 [22] |

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 64 | Condition | Logic: input port 1 false | Satisfied | 1 [19] |

# FiniteStateMachine/Sen/Actions/Transition/Switch1

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 65 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 66 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Sen/Actions/Nominal/Switch1

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 67 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |
| 68 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Sen/Actions/Fault/Logical Operator3

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 69 | Condition | Logic: input port 1 true | Satisfied | 1 [19] |
| 70 | Condition | Logic: input port 1 false | Satisfied | 1 [19] |

# FiniteStateMachine/Sen/Actions/Fault/Logical Operator12

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 71 | Condition | Logic: input port 1 true | Satisfied | 1 [19] |
| 72 | Condition | Logic: input port 1 false | Satisfied | 2 [22] |
| 73 | Condition | Logic: input port 2 true | Satisfied | 2 [22] |
| 74 | Condition | Logic: input port 2 false | Satisfied | 3 [22] |

# FiniteStateMachine/Sen/Actions/Fault/Switch1

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 75 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 3 [22] |
| 76 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# FiniteStateMachine/Sen/Output/Relational Operator5

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 77 | Condition | RelationalOperator: input1 == input2 true | Satisfied | 1 [19] |
| 78 | Condition | RelationalOperator: input1 == input2 false | Satisfied | 1 [19] |

# FiniteStateMachine/Sen/Output/Switch2

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 79 | Decision | logical trigger input false (output is from 3rd input port) | Satisfied | 1 [19] |

| #: | Type | Description | Status | Test Case |
|---|---|---|---|---|
| 80 | Decision | logical trigger input true (output is from 1st input port) | Satisfied | 1 [19] |

# Chapter 5. Test Cases

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This section contains detailed information about each generated test case.

# Test Case 1

**Summary.**

| | |
|---|---|
| Length: | 3 seconds (16 sample periods) |
| Objectives Satisfied: | 67 |

**Objectives.**

| Step | Time | Model Item | Objectives |
|---|---|---|---|
| 1 | 0 | FiniteStateMachine/Manager/Output/If<br>FiniteStateMachine/Manager/Output/If<br>FiniteStateMachine/Manager/Output/If<br>FiniteStateMachine/Sen/Actions/If<br>FiniteStateMachine/Manager/Output/If<br>FiniteStateMachine/Sen/Actions/Nominal/Switch2<br>FiniteStateMachine/Manager/Actions/If<br>FiniteStateMachine/Manager/Actions/Transition/Switch2<br>FiniteStateMachine/Sen/Output/Relational Operator5<br>FiniteStateMachine/Sen/Output/Switch2 | input 2 "elseif" condition false<br>input 3 "elseif" condition false<br>input 1 "if" condition false<br>input 1 "if" condition true<br>input 4 "elseif" condition true<br>logical trigger input true (output is from 1st input port)<br>input 1 "if" condition true<br>logical trigger input true (output is from 1st input port)<br>RelationalOperator: input1 == input2 true<br>logical trigger input true (output is from 1st input port) |
| 2 | 0.2 | FiniteStateMachine/Manager/Actions/If<br>FiniteStateMachine/Manager/Actions/If<br>FiniteStateMachine/Manager/Actions/Standby/Switch2<br>FiniteStateMachine/Manager/Actions/If<br>FiniteStateMachine/Sen/Actions/If<br>FiniteStateMachine/Sen/Actions/If<br>FiniteStateMachine/Manager/Output/If<br>FiniteStateMachine/Sen/Actions/Fault/Logical Operator3<br>FiniteStateMachine/Sen/Actions/If<br>FiniteStateMachine/Sen/Actions/Fault/Logical Operator12 | input 3 "elseif" condition false<br>input 2 "elseif" condition false<br>logical trigger input true (output is from 1st input port)<br>input 4 "elseif" condition true<br>input 1 "if" condition false<br>input 2 "elseif" condition false<br>input 3 "elseif" condition true<br>Logic: input port 1 true<br>input 3 "elseif" condition true<br>Logic: input port 1 true<br>Logic: input port 1 false<br>input 1 "if" condition false |

| Step | Time | Model Item | Objectives |
|---|---|---|---|
| | | FiniteStateMachine/Sen/Actions/Fault/Logical Operator2<br>FiniteStateMachine/Manager/Actions/If<br>FiniteStateMachine/Sen/Actions/Fault/Switch1<br>FiniteStateMachine/Sen/Output/Relational Operator5<br>FiniteStateMachine/Sen/Output/Switch2 | logical trigger input true (output is from 1st input port)<br>RelationalOperator: input1 == input2 false<br>logical trigger input false (output is from 3rd input port) |
| 3 | 0.4 | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator1<br>FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator1<br>FiniteStateMachine/Manager/Actions/If<br>FiniteStateMachine/Manager/Actions/Maneuver/Switch2<br>FiniteStateMachine/Sen/Actions/If<br>FiniteStateMachine/Sen/Actions/Transition/Logical Operator12<br>FiniteStateMachine/Sen/Actions/Transition/Switch1 | Logic: input port 1 true<br>Logic: input port 2 true<br>input 3 "elseif" condition true<br>logical trigger input true (output is from 1st input port)<br>input 2 "elseif" condition true<br>Logic: input port 1 false<br>logical trigger input false (output is from 3rd input port) |
| 4 | 0.6 | FiniteStateMachine/Manager/Actions/Standby/Switch2<br>FiniteStateMachine/Manager/Actions/Standby/Switch1<br>FiniteStateMachine/Manager/Output/If<br>FiniteStateMachine/Manager/Actions/Standby/Logical Operator12<br>FiniteStateMachine/Sen/Actions/Transition/Logical Operator12<br>FiniteStateMachine/Sen/Actions/Transition/Logical Operator12 | logical trigger input false (output is from 3rd input port)<br>logical trigger input true (output is from 1st input port)<br>input 1 "if" condition true<br>Logic: input port 1 false<br>Logic: input port 1 true<br>Logic: input port 2 false |
| 5 | 0.8 | FiniteStateMachine/Manager/Actions/Transition/Switch1<br>FiniteStateMachine/Manager/Actions/Transition/Logical Operator12<br>FiniteStateMachine/Manager/Actions/Transition/Switch2 | logical trigger input false (output is from 3rd input port)<br>Logic: input port 1 false<br>logical trigger input false (output is from 3rd input port) |
| 6 | 1 | FiniteStateMachine/Manager/Actions/Transition/Logical Operator12<br>FiniteStateMachine/Manager/Actions/Transition/Logical Operator12<br>FiniteStateMachine/Manager/Actions/Transition/Switch1<br>FiniteStateMachine/Manager/Output/If<br>FiniteStateMachine/Sen/Actions/Transition/Logical Operator12<br>FiniteStateMachine/Sen/Actions/Transition/Switch1 | Logic: input port 2 true<br>Logic: input port 1 true<br>logical trigger input true (output is from 1st input port)<br>input 2 "elseif" condition true<br>Logic: input port 2 true<br>logical trigger input true (output is from 1st input port) |

| Step | Time | Model Item | Objectives |
|---|---|---|---|
| 7 | 1.2 | FiniteStateMachine/Manager/Actions/Nominal/Logical Operator12<br>FiniteStateMachine/Manager/Actions/If<br>FiniteStateMachine/Manager/Actions/Nominal/Switch1<br>FiniteStateMachine/Manager/Actions/Nominal/Switch2<br>FiniteStateMachine/Sen/Actions/Nominal/Switch2<br>FiniteStateMachine/Sen/Actions/Nominal/Logical Operator12<br>FiniteStateMachine/Sen/Actions/Nominal/Switch1 | Logic: input port 1 true<br>input 2 "elseif" condition true<br>logical trigger input false (output is from 3rd input port)<br>logical trigger input false (output is from 3rd input port)<br>logical trigger input false (output is from 3rd input port)<br>Logic: input port 1 true<br>logical trigger input false (output is from 3rd input port) |
| 8 | 1.4 | FiniteStateMachine/Manager/Actions/Nominal/Switch2<br>FiniteStateMachine/Sen/Actions/Nominal/Switch1<br>FiniteStateMachine/Sen/Actions/Nominal/Logical Operator12 | logical trigger input true (output is from 1st input port)<br>logical trigger input true (output is from 1st input port)<br>Logic: input port 1 false |
| 9 | 1.6 | FiniteStateMachine/Manager/Actions/Standby/Logical Operator12<br>FiniteStateMachine/Manager/Actions/Standby/Switch1 | Logic: input port 1 true<br>logical trigger input false (output is from 3rd input port) |
| 12 | 2.2 | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator1<br>FiniteStateMachine/Manager/Actions/Maneuver/Switch2<br>FiniteStateMachine/Manager/Actions/Maneuver/Switch1<br>FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator12 | Logic: input port 1 false<br>logical trigger input false (output is from 3rd input port)<br>logical trigger input false (output is from 3rd input port)<br>Logic: input port 1 false |
| 13 | 2.4 | FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator12<br>FiniteStateMachine/Manager/Actions/Maneuver/Logical Operator12<br>FiniteStateMachine/Manager/Actions/Maneuver/Switch1 | Logic: input port 2 true<br>Logic: input port 1 true<br>logical trigger input true (output is from 1st input port) |
| 16 | 3 | FiniteStateMachine/Sen/Actions/Fault/Logical Operator3 | Logic: input port 1 false |

**Generated Input Data.**

| **Time** | **0-0.4** | **0.6-0.8** | **1-1.2** | **1.4-1.8** | **2** | **2.2** | **2.4-2.6** | **2.8** | **3** |
|---|---|---|---|---|---|---|---|---|---|
| **Step** | **1-3** | **4-5** | **6-7** | **8-10** | **11** | **12** | **13-14** | **15** | **16** |
| standby | 5.9566 | 0 | 0 | -1 | -3.321 | 0 | 0 | -3.4756 | 0 |
| apfail | 1.9184 | 0 | 0 | 0 | 5.9365 | 0 | 0 | 2.6094 | -1 |

| **Time** | **0-0.4** | **0.6-0.8** | **1-1.2** | **1.4-1.8** | **2** | **2.2** | **2.4-2.6** | **2.8** | **3** |
|---|---|---|---|---|---|---|---|---|---|
| **Step** | **1-3** | **4-5** | **6-7** | **8-10** | **11** | **12** | **13-14** | **15** | **16** |
| suppor-ted | -5.4067 | 0 | -1 | 0 | -6.4012 | 0 | -1 | 1.6229 | 0 |
| limits | 9.8142 | 0 | 0 | 0 | 2.414 | 0 | 0 | -4.7853 | 0 |

# Test Case 2

**Summary.**

| | |
|---|---|
| Length: | 0.2 second (2 sample periods) |
| Objectives Satisfied: | 3 |

**Objectives.**

| **St-ep** | **Ti-me** | **Model Item** | **Objectives** |
|---|---|---|---|
| 2 | 0.2 | FiniteStateMachine/Sen/Actions/Faul-t/Logical Operator12<br>FiniteStateMachine/Sen/Actions/Faul-t/Logical Operator2<br>FiniteStateMachine/Sen/Actions/Faul-t/Logical Operator12 | Logic: input port 1 false<br>Logic: input port 1 true<br>Logic: input port 2 true |

**Generated Input Data.**

| **Time** | **0** | **0.2** |
|---|---|---|
| **Step** | **1** | **2** |
| standby | 1 | 0 |
| apfail | 0 | 0 |
| supported | 0 | -1 |
| limits | 1 | 0 |

# Test Case 3

**Summary.**

| | |
|---|---|
| Length: | 0.2 second (2 sample periods) |
| Objectives Satisfied: | 2 |

**Objectives.**

| **St-ep** | **Ti-me** | **Model Item** | **Objectives** |
|---|---|---|---|
| 2 | 0.2 | FiniteStateMachine/Sen/Actions/Faul-t/Logical Operator12 | Logic: input port 2 false |

| Step | Time | Model Item | Objectives |
|---|---|---|---|
| | | FiniteStateMachine/Sen/Actions/Fault/Switch1 | logical trigger input false (output is from 3rd input port) |

**Generated Input Data.**

| Time | 0 | 0.2 |
|---|---|---|
| **Step** | **1** | **2** |
| standby | 1 | 0 |
| apfail | 0 | 0 |
| supported | 0 | -1 |
| limits | 1 | 1 |

# Test Case 4

**Summary.**

| | |
|---|---|
| Length: | 0.2 second (2 sample periods) |
| Objectives Satisfied: | 2 |

**Objectives.**

| Step | Time | Model Item | Objectives |
|---|---|---|---|
| 2 | 0.2 | FiniteStateMachine/Manager/Actions/Nominal/Logical Operator12<br>FiniteStateMachine/Manager/Actions/Nominal/Switch1 | Logic: input port 1 false<br>logical trigger input true (output is from 1st input port) |

**Generated Input Data.**

| Time | 0 | 0.2 |
|---|---|---|
| **Step** | **1** | **2** |
| standby | 0 | 0 |
| apfail | 0 | - |
| supported | 1 | 0 |
| limits | 1 | - |

# Test Case 5

**Summary.**

| | |
|---|---|
| Length: | 0.2 second (2 sample periods) |
| Objectives Satisfied: | 1 |

**Objectives.**

| Step | Time | Model Item | Objectives |
|---|---|---|---|
| 2 | 0.2 | FiniteStateMachine/Manager/Actions/Transition/Logical Operator12 | Logic: input port 2 false |

**Generated Input Data.**

| **Time** | **0** | **0.2** |
|---|---|---|
| **Step** | **1** | **2** |
| standby | 0 | 0 |
| apfail | 0 | - |
| supported | 0 | -1 |
| limits | 1 | - |