Simulink Design Verifier Report

F:\Benchmark\sldv_output\regs_12B\regs_12B_replacement.slx

YUZEHONG

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Chapter 1. Summary

Analysis Information.

Model:	regs_12B
Replacement Model:	F:\Benchmark\sldv_output\regs_12B\regs_12B_replacement.s-lx
Mode:	Test generation
Model Representation:	Built on 28-Aug-2021 14:08:42
Test generation target:	Model
Status:	Exceeded time limit
PreProcessing Time:	11s
Analysis Time:	300s

Objectives Status.

Number of Objectives:	**28**
Objectives Satisfied:	18
Objectives Unsatisfiable:	8
Objectives Undecided:	2

Chapter 2. Analysis Information

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Model Information

File:	regs_12B
Version:	1.55
Time Stamp:	Wed Dec 05 21:38:09 2018
Author:	elliocm

Analysis Options

Mode:	TestGeneration
Rebuild Model Representation:	IfChangeIsDetected
Test generation target:	Model
Test Suite Optimization:	Auto
Maximum Testcase Steps:	10000time steps
Test Conditions:	UseLocalSettings
Test Objectives:	UseLocalSettings
Model Coverage Objectives:	ConditionDecision
Include Relational Boundary Objectives:	off
Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on
Save Data:	on
Save Harness:	off
Save Report:	off

Chapter 3. Test Objectives Status

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Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
2	Condition	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator	RelationalOperator: input1 < input2 **false**	5	1 [11]
3	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch1	logical trigger input **false (output is from 3rd input port)**	5	1 [11]
5	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch2	logical trigger input **false (output is from 3rd input port)**	5	1 [11]
8	Condition	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator	RelationalOperator: input1 < input2 **false**	5	1 [11]
9	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch1	logical trigger input **false (output is from 3rd input port)**	5	1 [11]
11	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch2	logical trigger input **false (output is from 3rd input port)**	5	1 [11]
13	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Switch	logical trigger input **false (output is from 3rd input port)**	5	1 [11]
15	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	logical trigger input **false (output is from 3rd input port)**	5	1 [11]

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
16	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	logical trigger input **true (output is from 1st input port)**	163	2 [12]
17	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input **false (output is from 3rd input port)**	5	1 [11]
18	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input **true (output is from 1st input port)**	163	3 [13]
19	Decision	Regulators/HeightRegulator/Saturation	input > lower limit **true**	5	1 [11]
20	Decision	Regulators/HeightRegulator/Saturation	input > lower limit **false**	5	1 [11]
21	Decision	Regulators/HeightRegulator/Saturation	input >= upper limit **true**	5	1 [11]
22	Decision	Regulators/HeightRegulator/Saturation	input >= upper limit **false**	5	1 [11]
23	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Switch	logical trigger input **false (output is from 3rd input port)**	5	1 [11]
25	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	logical trigger input **false (output is from 3rd input port)**	5	1 [11]
27	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input **false (output is from 3rd input port)**	5	1 [11]

Objectives Unsatisfiable

Simulink Design Verifier found that there does not exist any test case exercising these test objectives. This often indicates the presence of dead logic in the model. Other possible reasons can be inactive blocks in the model due to parameter configuration or test constraints such as given using Test Condition blocks.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
1	Condition	Regulators/HeightRegulator/Tustin Integrator (Limi-	RelationalOperator: input1 < input2 **true**	7	n/a

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
		ted, Resettable, States)/bounds/Relational Operator			
4	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch1	logical trigger input **true (output is from 1st input port)**	7	n/a
6	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch2	logical trigger input **true (output is from 1st input port)**	7	n/a
7	Condition	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator	RelationalOperator: input1 < input2 **true**	7	n/a
10	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch1	logical trigger input **true (output is from 1st input port)**	7	n/a
12	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch2	logical trigger input **true (output is from 1st input port)**	7	n/a
14	Decision	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Switch	logical trigger input **true (output is from 1st input port)**	7	n/a
24	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Switch	logical trigger input **true (output is from 1st input port)**	7	n/a

Objectives Undecided

Simulink Design Verifier was not able to process these objectives with the current options.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
26	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	logical trigger input **true (output is from 1st input port)**	-1	n/a
28	Decision	Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input **true (output is from 1st input port)**	-1	n/a

Chapter 4. Model Items

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This section presents, for each object in the model defining coverage objectives, the list of objectives and their individual status at the end of the analysis. It should match the coverage report obtained from running the generated test suite on the model, either from the harness model or by using the sldvruntest command.

Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator

#:	Type	Description	Status	Test Case
1	Condition	RelationalOperator: input1 < input2 true	Unsatisfiable	n/a
2	Condition	RelationalOperator: input1 < input2 false	Satisfied	1 [11]

Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch1

#:	Type	Description	Status	Test Case
3	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
4	Decision	logical trigger input true (output is from 1st input port)	Unsatisfiable	n/a

Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch2

#:	Type	Description	Status	Test Case
5	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
6	Decision	logical trigger input true (output is from 1st input port)	Unsatisfiable	n/a

Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator

#:	Type	Description	Status	Test Case
7	Condition	RelationalOperator: input1 < input2 true	Unsatisfiable	n/a
8	Condition	RelationalOperator: input1 < input2 false	Satisfied	1 [11]

Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch1

#:	Type	Description	Status	Test Case
9	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
10	Decision	logical trigger input true (output is from 1st input port)	Unsatisfiable	n/a

Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch2

#:	Type	Description	Status	Test Case
11	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
12	Decision	logical trigger input true (output is from 1st input port)	Unsatisfiable	n/a

Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Switch

#:	Type	Description	Status	Test Case
13	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
14	Decision	logical trigger input true (output is from 1st input port)	Unsatisfiable	n/a

Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2

#:	Type	Description	Status	Test Case
15	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
16	Decision	logical trigger input true (output is from 1st input port)	Satisfied	2 [12]

Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch

#:	Type	Description	Status	Test Case
17	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
18	Decision	logical trigger input true (output is from 1st input port)	Satisfied	3 [13]

Regulators/HeightRegulator/Saturation

#:	Type	Description	Status	Test Case
19	Decision	input > lower limit true	Satisfied	1 [11]
20	Decision	input > lower limit false	Satisfied	1 [11]
21	Decision	input >= upper limit true	Satisfied	1 [11]
22	Decision	input >= upper limit false	Satisfied	1 [11]

Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Switch

#:	Type	Description	Status	Test Case
23	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
24	Decision	logical trigger input true (output is from 1st input port)	Unsatisfiable	n/a

Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2

#:	Type	Description	Status	Test Case
25	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
26	Decision	logical trigger input true (output is from 1st input port)	Undecided	n/a

Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch

#:	Type	Description	Status	Test Case
27	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [11]
28	Decision	logical trigger input true (output is from 1st input port)	Undecided	n/a

Chapter 5. Test Cases

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This section contains detailed information about each generated test case. Some input signals are unused. Input data will not be reported for them.

Test Case 1

Summary.

Length:	0.02 second (3 sample periods)
Objectives Satisfied:	16

Objectives.

Step	Time	Model Item	Objectives
1	0	Regulators/HeightRegulator/Saturation	input >= upper limit false
		Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Switch	logical trigger input false (output is from 3rd input port)
		Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	logical trigger input false (output is from 3rd input port) input > lower limit false
		Regulators/HeightRegulator/Saturation	logical trigger input false (output is from 3rd input port)
		Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Switch	logical trigger input false (output is from 3rd input port)
		Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input false (output is from 3rd input port)
		Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input false (output is from 3rd input port)
		Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	RelationalOperator: input1 < input2 false logical trigger input false (output is from 3rd input port)
		Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch1	RelationalOperator: input1 < input2 false logical trigger input false (output is from 3rd input port)
		Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator	logical trigger input false (output is from 3rd input port)

Step	Time	Model Item	Objectives
		Regulators/HeightRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch2 Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch1 Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/bounds/Switch2	
2	0.01	Regulators/HeightRegulator/Saturation	input > lower limit true
3	0.02	Regulators/HeightRegulator/Saturation	input >= upper limit true

Generated Input Data.

Time	**0**	**0.01**	**0.02**
Step	**1**	**2**	**3**
beta_adc_deg	5.9566	0	0
vtas_adc_kts	1.9184	1	1
lcv_cmd_fcs_dps	-5.4067	0	0
mcv_cmd_fcs_dps	-3.321	1.4643	1.4643
ncv_cmd_fcs_dps	-6.4012	-7.5632	-7.5632
xcv_cmd_fcs_fps	2.414	0	0
hcv_cmd_fcs_fps	2.6094	0	1
lcv_fps_dps	1.6229	0	0
mcv_fcs_dps	-4.7853	0	0
ncv_fcs_dps	1.162	0	0
dcv_fcs_fps	-6.7752	0	0
zcv_fcs_fps	-5.4024	0	0
beta_dot	-4.0808	0	0

Test Case 2

Summary.

Length:	0 second (1 sample period)
Objectives Satisfied:	1

Objectives.

Step	Time	Model Item	Objectives
1	0	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	logical trigger input true (output is from 1st input port)

Generated Input Data.

Time	**0**
Step	**1**
beta_adc_deg	-
vtas_adc_kts	-
lcv_cmd_fcs_dps	-
mcv_cmd_fcs_dps	2000000
ncv_cmd_fcs_dps	-
xcv_cmd_fcs_fps	-
hcv_cmd_fcs_fps	-
lcv_fps_dps	-
mcv_fcs_dps	0
ncv_fcs_dps	-
dcv_fcs_fps	-
zcv_fcs_fps	-
beta_dot	-

Test Case 3

Summary.

Length:	0 second (1 sample period)
Objectives Satisfied:	1

Objectives.

Step	Time	Model Item	Objectives
1	0	Regulators/PitchRegulator/Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input true (output is from 1st input port)

Generated Input Data.

Time	**0**
Step	**1**
beta_adc_deg	-

Time	**0**
Step	**1**
vtas_adc_kts	-
lcv_cmd_fcs_dps	-
mcv_cmd_fcs_dps	-2000000
ncv_cmd_fcs_dps	-
xcv_cmd_fcs_fps	-
hcv_cmd_fcs_fps	-
lcv_fps_dps	-
mcv_fcs_dps	0
ncv_fcs_dps	-
dcv_fcs_fps	-
zcv_fcs_fps	-
beta_dot	-