Simulink Design Verifier Report

NLGuidance

YUZEHONG

Simulink Design Verifier Report: NLGuidance

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Publication date 27-Aug-2021 10:00:28

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Chapter 1. Summary

Analysis Information.

Model:	NLGuidance
Mode:	Test generation
Model Representation:	Cache from 27-Aug-2021 09:52:14
Test generation target:	Model
Status:	Stopped by user
PreProcessing Time:	4s
Analysis Time:	171s

Objectives Status.

Number of Objectives:	**18**
Objectives Satisfied:	7
Objectives Undecided Due to Nonlinearities:	1
Objectives Undecided Due to Division by Zero:	8
Objectives Unsatisfiable under Approximation:	2

Chapter 2. Analysis Information

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Model Information

File:	NLGuidance
Version:	1.72
Time Stamp:	Fri Mar 23 23:59:56 2018
Author:	elliocm

Analysis Options

Mode:	TestGeneration
Rebuild Model Representation:	IfChangeIsDetected
Test generation target:	Model
Test Suite Optimization:	Auto
Maximum Testcase Steps:	10000time steps
Test Conditions:	UseLocalSettings
Test Objectives:	UseLocalSettings
Model Coverage Objectives:	ConditionDecision
Include Relational Boundary Objectives:	off
Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on
Save Data:	on
Save Harness:	off
Save Report:	off

Approximations

Simulink Design Verifier performed the following approximations during analysis. These can impact the precision of the results generated by Simulink Design Verifier. Please see the product documentation for further details.

#	Type	Description
1	Rational approximation	The model includes floating-point arithmetic. Simulink Design Verifier approximates floating-point arithmetic with rational number arithmetic. Specifying minimum and maximum values that mimic environmental constraints on root-level Inport blocks may reduce instances of rational approximation.

Chapter 3. Test Objectives Status

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Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
2	Condition	NLGuidance/Relational Operator1	RelationalOperator: input1 <= input2 **false**	4	1 [9]
4	Condition	NLGuidance/Relational Operator	RelationalOperator: input1 <= input2 **false**	4	1 [9]
6	Condition	NLGuidance/Logical Operator	Logic: input port 1 **false**	4	1 [9]
8	Condition	NLGuidance/Logical Operator	Logic: input port 2 **false**	4	1 [9]
10	Decision	NLGuidance/If	input logical value **false**	4	1 [9]
12	Condition	NLGuidance/Outer/Relational Operator	RelationalOperator: input1 < input2 **false**	4	1 [9]
18	Decision	NLGuidance/Outer/If	input logical value **false**	4	1 [9]

Objectives Undecided Due to Nonlinearities

Simulink Design Verifier was not able to decide these objectives due to the presence of nonlinear arithmetic in the model.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
7	Condition	NLGuidance/Logical Operator	Logic: input port 2 **true**	10	n/a

Objectives Undecided Due to Division by Zero

Simulink Design Verifier was not able to decide these objectives due to division by zero errors in the model.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
1	Condition	NLGuidance/Relational Operator1	RelationalOperator: input1 <= input2 **true**	10	n/a
3	Condition	NLGuidance/Relational Operator	RelationalOperator: input1 <= input2 **true**	10	n/a
5	Condition	NLGuidance/Logical Operator	Logic: input port 1 **true**	10	n/a
9	Decision	NLGuidance/If	input logical value **true**	10	n/a
13	Condition	NLGuidance/Inner/Relational Operator1	RelationalOperator: input1 < input2 **true**	10	n/a
14	Condition	NLGuidance/Inner/Relational Operator1	RelationalOperator: input1 < input2 **false**	10	n/a
15	Decision	NLGuidance/Inner/If	input logical value **true**	10	n/a
16	Decision	NLGuidance/Inner/If	input logical value **false**	10	n/a

Objectives Unsatisfiable under Approximation

Simulink Design Verifier found that there does not exist any test case exercising these test objectives under the impact of approximations during analysis. This often indicates the presence of dead logic in the model. Other possible reasons can be inactive blocks in the model due to parameter configuration or test constraints such as given using Test Condition blocks. In rare cases, the approximations performed by Simulink Design Verifier can make objectives impossible to achieve.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
11	Condition	NLGuidance/Outer/Relational Operator	RelationalOperator: input1 < input2 **true**	10	n/a
17	Decision	NLGuidance/Outer/If	input logical value **true**	10	n/a

Chapter 4. Model Items

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This section presents, for each object in the model defining coverage objectives, the list of objectives and their individual status at the end of the analysis. It should match the coverage report obtained from running the generated test suite on the model, either from the harness model or by using the sldvruntest command.

NLGuidance/Relational Operator1

#:	Type	Description	Status	Test Case
1	Condition	RelationalOperator: input1 <= input2 true	Undecided due to division by zero	n/a
2	Condition	RelationalOperator: input1 <= input2 false	Satisfied	1 [9]

NLGuidance/Relational Operator

#:	Type	Description	Status	Test Case
3	Condition	RelationalOperator: input1 <= input2 true	Undecided due to division by zero	n/a
4	Condition	RelationalOperator: input1 <= input2 false	Satisfied	1 [9]

NLGuidance/Logical Operator

#:	Type	Description	Status	Test Case
5	Condition	Logic: input port 1 true	Undecided due to division by zero	n/a
6	Condition	Logic: input port 1 false	Satisfied	1 [9]
7	Condition	Logic: input port 2 true	Undecided due to nonlinearities	n/a
8	Condition	Logic: input port 2 false	Satisfied	1 [9]

NLGuidance/If

#:	Type	Description	Status	Test Case
9	Decision	input logical value true	Undecided due to division by zero	n/a
10	Decision	input logical value false	Satisfied	1 [9]

NLGuidance/Outer/Relational Operator

#:	Type	Description	Status	Test Case
11	Condition	RelationalOperator: input1 < input2 true	Unsatisfiable under approximation	n/a
12	Condition	RelationalOperator: input1 < input2 false	Satisfied	1 [9]

NLGuidance/Inner/Relational Operator1

#:	Type	Description	Status	Test Case
13	Condition	RelationalOperator: input1 < input2 true	Undecided due to division by zero	n/a
14	Condition	RelationalOperator: input1 < input2 false	Undecided due to division by zero	n/a

NLGuidance/Inner/If

#:	Type	Description	Status	Test Case
15	Decision	input logical value true	Undecided due to division by zero	n/a
16	Decision	input logical value false	Undecided due to division by zero	n/a

NLGuidance/Outer/If

#:	Type	Description	Status	Test Case
17	Decision	input logical value true	Unsatisfiable under approximation	n/a
18	Decision	input logical value false	Satisfied	1 [9]

Chapter 5. Test Cases

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This section contains detailed information about each generated test case. Some input signals are unused. Input data will not be reported for them.

Test Case 1

Summary.

Length:	0 second (1 sample period)
Objectives Satisfied:	7

Objectives.

Step	Time	Model Item	Objectives
1	0	NLGuidance/Relational Operator1 NLGuidance/Relational Operator NLGuidance/Logical Operator NLGuidance/If NLGuidance/Logical Operator NLGuidance/Outer/If NLGuidance/Outer/Relational Operator	RelationalOperator: input1 <= input2 false RelationalOperator: input1 <= input2 false Logic: input port 2 false input logical value false Logic: input port 1 false input logical value false RelationalOperator: input1 < input2 false

Generated Input Data.

Time	**0**
Step	**1**
Xtarg	[5.9566 1.9184 -5.4067]
Xv	[9.8142 -3.321 5.9365]
Vv	[-6.4012 2.414 -3.4756]
r	1.162