

Simulink Design Verifier Report

euler321_I2B_12B

YUZEHONG

Simulink Design Verifier Report: euler321_I2B_12B

YUZEHONG

Publication date 27-Aug-2021 10:31:30

Table of Contents

1. Summary	1
2. Analysis Information	2
Model Information	2
Analysis Options	2
Unsupported Blocks	3
3. Test Objectives Status	4
Objectives Satisfied	4
Objectives Undecided Due to Stubbing	5
Objectives Undecided Due to Nonlinearities	5
4. Model Items	7
Subsystem2/Relational Operator	7
Subsystem2/Relational Operator1	7
Subsystem2/Relational Operator2	8
Subsystem2/Relational Operator3	8
Subsystem2/Relational Operator4	8
Subsystem2/Relational Operator5	8
Subsystem2/Relational Operator6	9
Subsystem2/Relational Operator7	9
Subsystem2/Relational Operator8	9
Subsystem2/AND	10
5. Test Cases	12
Test Case 1	12

Chapter 1. Summary

Analysis Information.

Model:	euler321_I2B_12B
Mode:	Test generation
Model Representation:	Built on 27-Aug-2021 10:30:36
Test generation target:	Model
Status:	Stopped by user
PreProcessing Time:	9s
Analysis Time:	46s

Objectives Status.

Number of Objectives:	36
Objectives Satisfied:	18
Objectives Undecided Due to Stubbing:	1
Objectives Undecided Due to Nonlinearities:	17

Chapter 2. Analysis Information

Table of Contents

Model Information	2
Analysis Options	2
Unsupported Blocks	3

Model Information

File:	euler321_I2B_12B
Version:	1.44
Time Stamp:	Mon Nov 19 18:10:29 2018
Author:	elliocm

Analysis Options

Mode:	TestGeneration
Rebuild Model Representation:	IfChangeIsDetected
Test generation target:	Model
Test Suite Optimization:	Auto
Maximum Testcase Steps:	10000time steps
Test Conditions:	UseLocalSettings
Test Objectives:	UseLocalSettings
Model Coverage Objectives:	ConditionDecision
Include Relational Boundary Objectives:	off
Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on
Save Data:	on
Save Harness:	off
Save Report:	off

Unsupported Blocks

The following blocks are not supported by Simulink Design Verifier. They were abstracted during the analysis. This can lead Simulink Design Verifier to produce only partial results for parts of the model that depends on the output values of these blocks.

Block	Type
sincos	Trigonometry
sincos	Trigonometry
sincos	Trigonometry
sincos	Trigonometry
sincos	Trigonometry
sincos	Trigonometry
sincos	Trigonometry
sincos	Trigonometry
sincos	Trigonometry
Trigonometric Function2	Trigonometry
Trigonometric Function3	Trigonometry
Trigonometric Function4	Trigonometry
Trigonometric Function5	Trigonometry
Trigonometric Function6	Trigonometry
Trigonometric Function7	Trigonometry

Chapter 3. Test Objectives Status

Table of Contents

Objectives Satisfied	4
Objectives Undecided Due to Stubbing	5
Objectives Undecided Due to Nonlinearities	5

Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
1	Condition	Subsystem2/Relational Operator	RelationalOperator: input1 == input2 true	5	1 [12]
3	Condition	Subsystem2/Relational Operator1	RelationalOperator: input1 == input2 true	5	1 [12]
5	Condition	Subsystem2/Relational Operator2	RelationalOperator: input1 == input2 true	5	1 [12]
7	Condition	Subsystem2/Relational Operator3	RelationalOperator: input1 == input2 true	5	1 [12]
9	Condition	Subsystem2/Relational Operator4	RelationalOperator: input1 == input2 true	5	1 [12]
11	Condition	Subsystem2/Relational Operator5	RelationalOperator: input1 == input2 true	5	1 [12]
13	Condition	Subsystem2/Relational Operator6	RelationalOperator: input1 == input2 true	5	1 [12]
15	Condition	Subsystem2/Relational Operator7	RelationalOperator: input1 == input2 true	5	1 [12]
17	Condition	Subsystem2/Relational Operator8	RelationalOperator: input1 == input2 true	5	1 [12]
19	Condition	Subsystem2/AND	Logic: input port 1 true	5	1 [12]
21	Condition	Subsystem2/AND	Logic: input port 2 true	5	1 [12]
23	Condition	Subsystem2/AND	Logic: input port 3 true	5	1 [12]
25	Condition	Subsystem2/AND	Logic: input port 4 true	5	1 [12]
27	Condition	Subsystem2/AND	Logic: input port 5 true	5	1 [12]
29	Condition	Subsystem2/AND	Logic: input port 6 true	5	1 [12]

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
31	Condition	Subsystem2/AND	Logic: input port 7 true	5	1 [12]
33	Condition	Subsystem2/AND	Logic: input port 8 true	5	1 [12]
35	Condition	Subsystem2/AND	Logic: input port 9 true	5	1 [12]

Objectives Undecided Due to Stubbing

Simulink Design Verifier was not able to decide these objectives due to stubbing.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
14	Condition	Subsystem2/Relational Operator6	RelationalOperator: input1 == input2 false	34	n/a

Objectives Undecided Due to Nonlinearities

Simulink Design Verifier was not able to decide these objectives due to the presence of nonlinear arithmetic in the model.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
2	Condition	Subsystem2/Relational Operator	RelationalOperator: input1 == input2 false	34	n/a
4	Condition	Subsystem2/Relational Operator1	RelationalOperator: input1 == input2 false	34	n/a
6	Condition	Subsystem2/Relational Operator2	RelationalOperator: input1 == input2 false	34	n/a
8	Condition	Subsystem2/Relational Operator3	RelationalOperator: input1 == input2 false	34	n/a
10	Condition	Subsystem2/Relational Operator4	RelationalOperator: input1 == input2 false	34	n/a
12	Condition	Subsystem2/Relational Operator5	RelationalOperator: input1 == input2 false	34	n/a
16	Condition	Subsystem2/Relational Operator7	RelationalOperator: input1 == input2 false	34	n/a
18	Condition	Subsystem2/Relational Operator8	RelationalOperator: input1 == input2 false	34	n/a
20	Condition	Subsystem2/AND	Logic: input port 1 false	34	n/a

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
22	Condition	Subsystem2/AND	Logic: input port 2 false	34	n/a
24	Condition	Subsystem2/AND	Logic: input port 3 false	34	n/a
26	Condition	Subsystem2/AND	Logic: input port 4 false	35	n/a
28	Condition	Subsystem2/AND	Logic: input port 5 false	35	n/a
30	Condition	Subsystem2/AND	Logic: input port 6 false	35	n/a
32	Condition	Subsystem2/AND	Logic: input port 7 false	35	n/a
34	Condition	Subsystem2/AND	Logic: input port 8 false	35	n/a
36	Condition	Subsystem2/AND	Logic: input port 9 false	35	n/a

Chapter 4. Model Items

Table of Contents

Subsystem2/Relational Operator	7
Subsystem2/Relational Operator1	7
Subsystem2/Relational Operator2	8
Subsystem2/Relational Operator3	8
Subsystem2/Relational Operator4	8
Subsystem2/Relational Operator5	8
Subsystem2/Relational Operator6	9
Subsystem2/Relational Operator7	9
Subsystem2/Relational Operator8	9
Subsystem2/AND	10

This section presents, for each object in the model defining coverage objectives, the list of objectives and their individual status at the end of the analysis. It should match the coverage report obtained from running the generated test suite on the model, either from the harness model or by using the `sldvruntime` command.

Subsystem2/Relational Operator

#:	Type	Description	Status	Test Case
1	Condition	RelationalOperator: input1 == input2 true	Satisfied	1 [12]
2	Condition	RelationalOperator: input1 == input2 false	Undecided due to nonlinearities	n/a

Subsystem2/Relational Operator1

#:	Type	Description	Status	Test Case
3	Condition	RelationalOperator: input1 == input2 true	Satisfied	1 [12]
4	Condition	RelationalOperator: input1 == input2 false	Undecided due to nonlinearities	n/a

Subsystem2/Relational Operator2

#:	Type	Description	Status	Test Case
5	Condition	RelationalOperator: input1 == input2 true	Satisfied	1 [12]
6	Condition	RelationalOperator: input1 == input2 false	Undecided due to nonlinearities	n/a

Subsystem2/Relational Operator3

#:	Type	Description	Status	Test Case
7	Condition	RelationalOperator: input1 == input2 true	Satisfied	1 [12]
8	Condition	RelationalOperator: input1 == input2 false	Undecided due to nonlinearities	n/a

Subsystem2/Relational Operator4

#:	Type	Description	Status	Test Case
9	Condition	RelationalOperator: input1 == input2 true	Satisfied	1 [12]
10	Condition	RelationalOperator: input1 == input2 false	Undecided due to nonlinearities	n/a

Subsystem2/Relational Operator5

#:	Type	Description	Status	Test Case
11	Condition	RelationalOperator: input1 == input2 true	Satisfied	1 [12]

#:	Type	Description	Status	Test Case
12	Condition	RelationalOperator: input1 == input2 false	Undecided due to nonlinearities	n/a

Subsystem2/Relational Operator6

#:	Type	Description	Status	Test Case
13	Condition	RelationalOperator: input1 == input2 true	Satisfied	1 [12]
14	Condition	RelationalOperator: input1 == input2 false	Undecided due to stubbing	n/a

Subsystem2/Relational Operator7

#:	Type	Description	Status	Test Case
15	Condition	RelationalOperator: input1 == input2 true	Satisfied	1 [12]
16	Condition	RelationalOperator: input1 == input2 false	Undecided due to nonlinearities	n/a

Subsystem2/Relational Operator8

#:	Type	Description	Status	Test Case
17	Condition	RelationalOperator: input1 == input2 true	Satisfied	1 [12]
18	Condition	RelationalOperator: input1 == input2 false	Undecided due to nonlinearities	n/a

Subsystem2/AND

#:	Type	Description	Status	Test Case
19	Condition	Logic: input port 1 true	Satisfied	1 [12]
20	Condition	Logic: input port 1 false	Undecided due to nonlinearities	n/a
21	Condition	Logic: input port 2 true	Satisfied	1 [12]
22	Condition	Logic: input port 2 false	Undecided due to nonlinearities	n/a
23	Condition	Logic: input port 3 true	Satisfied	1 [12]
24	Condition	Logic: input port 3 false	Undecided due to nonlinearities	n/a
25	Condition	Logic: input port 4 true	Satisfied	1 [12]
26	Condition	Logic: input port 4 false	Undecided due to nonlinearities	n/a
27	Condition	Logic: input port 5 true	Satisfied	1 [12]
28	Condition	Logic: input port 5 false	Undecided due to nonlinearities	n/a
29	Condition	Logic: input port 6 true	Satisfied	1 [12]
30	Condition	Logic: input port 6 false	Undecided	n/a

#:	Type	Description	Status	Test Case
			due to nonlinearity	
31	Condition	Logic: input port 7 true	Satisfied	1 [12]
32	Condition	Logic: input port 7 false	Undecided due to nonlinearity	n/a
33	Condition	Logic: input port 8 true	Satisfied	1 [12]
34	Condition	Logic: input port 8 false	Undecided due to nonlinearity	n/a
35	Condition	Logic: input port 9 true	Satisfied	1 [12]
36	Condition	Logic: input port 9 false	Undecided due to nonlinearity	n/a

Chapter 5. Test Cases

Table of Contents

Test Case 1	12
-------------------	----

This section contains detailed information about each generated test case.

Test Case 1

Summary.

Length: 0 second (1 sample period)
Objectives Satisfied: 18

Objectives.

St- ep	Ti- me	Model Item	Objectives
1	0	Subsystem2/Relational Operator2 Subsystem2/Relational Operator4 Subsystem2/Relational Operator3 Subsystem2/Relational Operator5 Subsystem2/Relational Operator7 Subsystem2/Relational Operator1 Subsystem2/Relational Operator6 Subsystem2/Relational Operator8 Subsystem2/Relational Operator Subsystem2/AND Subsystem2/AND Subsystem2/AND Subsystem2/AND Subsystem2/AND Subsystem2/AND Subsystem2/AND Subsystem2/AND Subsystem2/AND Subsystem2/AND	RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true RelationalOperator: input1 == input2 true Logic: input port 9 true Logic: input port 2 true Logic: input port 5 true Logic: input port 1 true Logic: input port 3 true Logic: input port 4 true Logic: input port 6 true Logic: input port 7 true Logic: input port 8 true

Generated Input Data.

Test Cases

Time	0
Step	1
phi	5.9566
theta	1.9184
psi	-5.4067
Vi	[9.8142 -3.321 5.9365]
Inport	-6.4012