

Simulink Design Verifier Report

tustinintegrator

YUZEHONG

Simulink Design Verifier Report: tustinintegrator

YUZEHONG

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Chapter 1. Summary

Analysis Information.

Model:	tustinintegrator
Mode:	Test generation
Model Representation:	Built on 28-Aug-2021 14:02:51
Test generation target:	Model
Status:	Completed normally
PreProcessing Time:	10s
Analysis Time:	4s

Objectives Status.

Number of Objectives:	12
Objectives Satisfied:	12

Chapter 2. Analysis Information

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Model Information

File:	tustinintegrator
Version:	1.56
Time Stamp:	Thu Jun 07 01:30:15 2018
Author:	elliocm

Analysis Options

Mode:	TestGeneration
Rebuild Model Representation:	IfChangeIsDetected
Test generation target:	Model
Test Suite Optimization:	Auto
Maximum Testcase Steps:	500time steps
Test Conditions:	UseLocalSettings
Test Objectives:	UseLocalSettings
Model Coverage Objectives:	ConditionDecision
Include Relational Boundary Objectives:	off
Maximum Analysis Time:	5000s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on
Save Data:	on
Save Harness:	off
Save Report:	off

Chapter 3. Test Objectives Status

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Objectives Satisfied	3
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Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
1	Condition	Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator	RelationalOperator: input1 < input2 true	3	1 [8]
2	Condition	Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator	RelationalOperator: input1 < input2 false	3	1 [8]
3	Decision	Tustin Integrator (Limited, Resettable, States)/bounds/Switch1	logical trigger input false (output is from 3rd input port)	3	1 [8]
4	Decision	Tustin Integrator (Limited, Resettable, States)/bounds/Switch1	logical trigger input true (output is from 1st input port)	3	1 [8]
5	Decision	Tustin Integrator (Limited, Resettable, States)/Switch	logical trigger input false (output is from 3rd input port)	3	1 [8]
6	Decision	Tustin Integrator (Limited, Resettable, States)/Switch	logical trigger input true (output is from 1st input port)	3	1 [8]
7	Decision	Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	logical trigger input false (output is from 3rd input port)	3	1 [8]
8	Decision	Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	logical trigger input true (output is from 1st input port)	3	1 [8]
9	Decision	Tustin Integrator (Limited, Resettable, States)/bounds/Switch2	logical trigger input false (output is from 3rd input port)	3	1 [8]
10	Decision	Tustin Integrator (Limited, Resettable, States)/bounds/Switch2	logical trigger input true (output is from 1st input port)	3	1 [8]
11	Decision	Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input false (output is from 3rd input port)	3	1 [8]

Test Objectives Status

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
12	Decision	Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input true (output is from 1st input port)	3	1 [8]

Chapter 4. Model Items

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Tustin Integrator (Limited, Resettable, States)/bounds/Switch1	5
Tustin Integrator (Limited, Resettable, States)/Switch	6
Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	6
Tustin Integrator (Limited, Resettable, States)/bounds/Switch2	6
Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	6

This section presents, for each object in the model defining coverage objectives, the list of objectives and their individual status at the end of the analysis. It should match the coverage report obtained from running the generated test suite on the model, either from the harness model or by using the `sldvrntest` command.

Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator

#:	Type	Description	Status	Test Case
1	Condition	RelationalOperator: input1 < input2 true	Satisfied	1 [8]
2	Condition	RelationalOperator: input1 < input2 false	Satisfied	1 [8]

Tustin Integrator (Limited, Resettable, States)/bounds/Switch1

#:	Type	Description	Status	Test Case
3	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [8]
4	Decision	logical trigger input true (output is from 1st input port)	Satisfied	1 [8]

Tustin Integrator (Limited, Resettable, State-s)/Switch

#:	Type	Description	Status	Test Case
5	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [8]
6	Decision	logical trigger input true (output is from 1st input port)	Satisfied	1 [8]

Tustin Integrator (Limited, Resettable, State-s)/Saturation Dynamic/Switch2

#:	Type	Description	Status	Test Case
7	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [8]
8	Decision	logical trigger input true (output is from 1st input port)	Satisfied	1 [8]

Tustin Integrator (Limited, Resettable, State-s)/bounds/Switch2

#:	Type	Description	Status	Test Case
9	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [8]
10	Decision	logical trigger input true (output is from 1st input port)	Satisfied	1 [8]

Tustin Integrator (Limited, Resettable, State-s)/Saturation Dynamic/Switch

#:	Type	Description	Status	Test Case
11	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1 [8]

Model Items

#:	Type	Description	Status	Test Case
12	Decision	logical trigger input true (output is from 1st input port)	Satisfied	1 [8]

Chapter 5. Test Cases

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This section contains detailed information about each generated test case.

Test Case 1

Summary.

Length: 0.4 second (5 sample periods)

Objectives Satisfied: 12

Objectives.

St- ep	Ti- me	Model Item	Objectives
1	0	Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator Tustin Integrator (Limited, Resettable, States)/bounds/Switch1 Tustin Integrator (Limited, Resettable, States)/Switch Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2	RelationalOperator: input1 < input2 true logical trigger input true (output is from 1st input port) logical trigger input true (output is from 1st input port) logical trigger input true (output is from 1st input port)
2	0.1	Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch2 Tustin Integrator (Limited, Resettable, States)/bounds/Switch2 Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input false (output is from 3rd input port) logical trigger input true (output is from 1st input port) logical trigger input false (output is from 3rd input port)
3	0.2	Tustin Integrator (Limited, Resettable, States)/Saturation Dynamic/Switch	logical trigger input true (output is from 1st input port)
4	0.3	Tustin Integrator (Limited, Resettable, States)/Switch	logical trigger input false (output is from 3rd input port)
5	0.4	Tustin Integrator (Limited, Resettable, States)/bounds/Switch1 Tustin Integrator (Limited, Resettable, States)/bounds/Switch2 Tustin Integrator (Limited, Resettable, States)/bounds/Relational Operator	logical trigger input false (output is from 3rd input port) logical trigger input false (output is from 3rd input port) RelationalOperator: input1 < input2 false

Generated Input Data.

Time	0	0.1	0.2	0.3	0.4
Step	1	2	3	4	5
xin	5.9566	0	0	0	0

Test Cases

Time	0	0.1	0.2	0.3	0.4
Step	1	2	3	4	5
reset	1.9184	1	1	0	0
T	-5.4067	0	0	0	0
ic	9.8142	0	0	0	0
TL	-3.321	-1	1	-1	0
BL	5.9365	0	2	0	0