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[front page](#) » [Cortex M0/M3/M4/M7](#)» [Assembly-optimized high-speed DAP-Link \(CMSIS-DAP v2\) implemented](#)Page: **1**[Share link / view only the original poster](#)The original poster 2022-02-07 17:34:55 [Share comments](#) #

posystorage

member

Registration time: 2018-05-06
Posted: 162
Points: 553

This work is improved based on the work of @ljbfly, the boss of this site.

Please see the post for details: CH552 version CMSIS-DAP v2 https://whycan.com/t_3732.html

The basic big frame has not been changed, and the SWD timing is optimized using assembly. High-speed provides SWD timing for IO simulation, and also provides a taste of hardware SPI.

Completely rewrites the C+ assembly mix and optimizes the virtual serial port part, effectively reducing serial port packet loss and transmission interruption problems, and improving efficiency.

Only the driver-free bulk mode of the v2 version is used. It is not compatible with the V1 version of hid. It provides a virtual serial port that currently occupies space. The ROM has used more than 7k, the ram is basically exhausted, all the xram is cache, and there are not many bytes left in the iram.

Access to open source code, compiled firmware, and PCB projects:

https://github.com/posystorage/CH55x_HS_DAP-Link-v2

The optimization idea refers to the work of @metro boss, see:

[Reopening the old pit] CMSIS-DAP debugger on 8051 - TinyDAP development process record

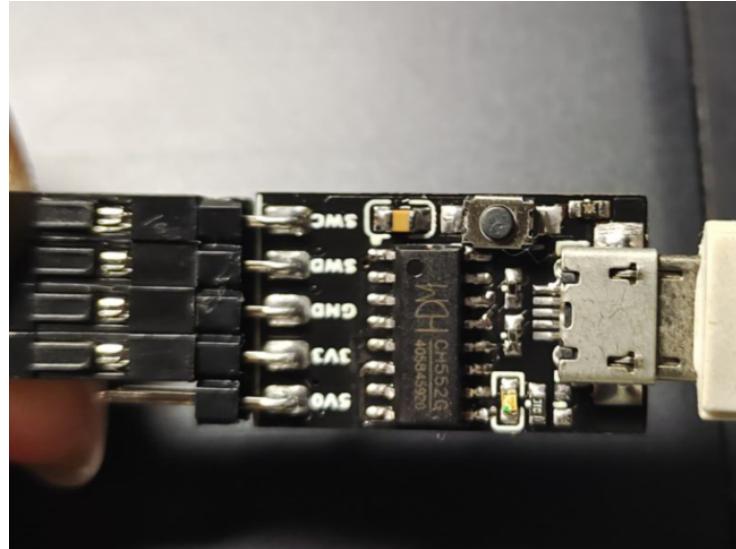
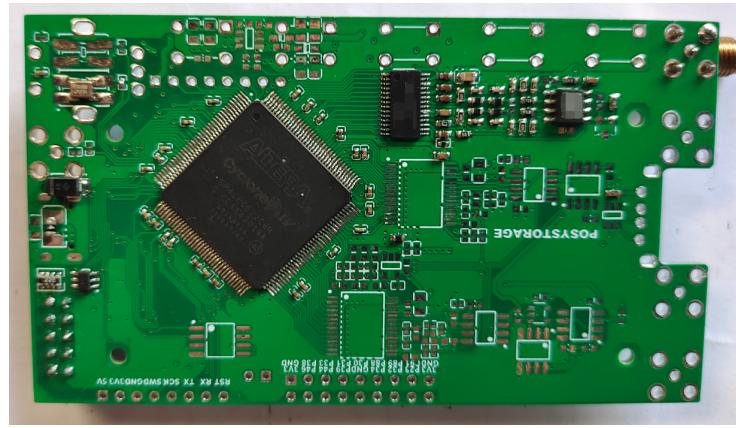
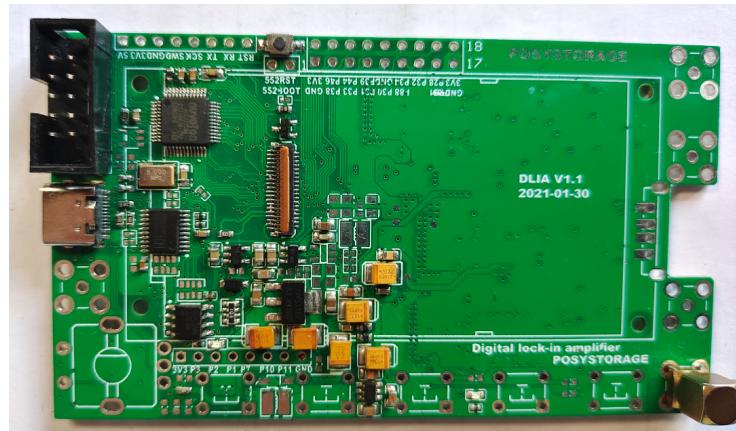
https://whycan.com/t_6114.html

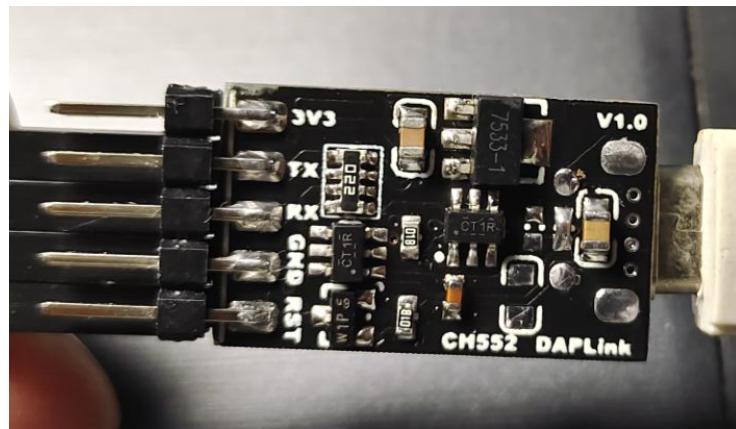
Show the CMSIS running on CH558 -DAP v2 debugger, download speed can reach 70KB/s (Flash) and 300KB/s (SRAM) https://whycan.com/t_3766.html

Compared with @metro boss, my goal is to achieve high-speed SWD optimization. I don't plan to dabble in JTAG\SWO\file drag and drop download\HID compatibility and other functions for the time being. The main application direction is to make an onboard debugger (such as using CH552E Realizing serial port + SWD), it is very convenient to debug the chip on the development board, reducing wiring.

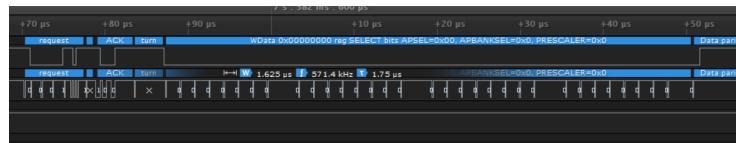
For example, this board for digging holes is used as a digital lock-in amplifier. The CH552 is responsible for communication + SWD debugging microcontroller + JTAG debugging FPGA, all integrated. Of course, when this hole will be filled is another matter. Back to the topic of hardware implementation, my board can choose 3.3V power supply or 5V. What I am considering is to choose 5V to run at 24M main frequency (32M is also stable and can run in the actual test), and then use two 1T45 to convert the IO level to 3.3V, which is

responsible for the process. SWDIO commutation, the board size is very small. If it is an onboard debugger, it is enough to run 16M with 3.3V power supply, which can save a lot of peripherals.





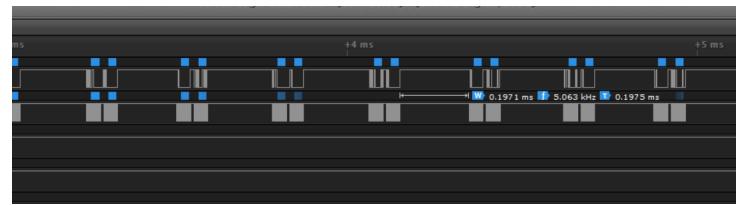
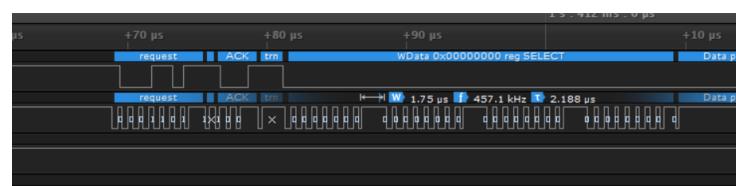
The code written by @ljbfly is implemented in full C. Due to compiler problems, the underlying part of SWD is frequently moving data. The timing effect seems to have a very high duty cycle, and SWD directly uses push-pull reading when inputting (let I was very confused at first). According to actual measurements, some microcontrollers may not have good compatibility if the SWD pin driver is not strong. So the entire SWD timing is created in an assembly file, all optimized with assembly. The 8051 mixed programming in C and assembly written on the Internet is also written in a mess, copied from each other, and pieced together here and there. It took me a long time to get this thing to work stably () Maybe it's because it's too bad. After optimization and calculation of soft IO simulation, 12 processor cycles can refresh an SWD clock, 16M clock speed at 3.3V, 1.66M, 5V IO simulation read timing under 24M main frequency clock 2M. 3.3V: IO simulation write timing under 3.3V: It seems that the duty cycle of the SWD interface is relatively large under 16M main frequency. After actual research, the interval time is two-fifths ch552 is processing, and three-fifths of it is because the upper computer is relatively slow. If the upper computer driver does not change, there is still a lot of room for optimization in the processing of DAP instructions by the lower computer (there is a lot of data transfer process from xram), but considering that my hair is limited, I won't do it for now.



```

3
4 SWC_PIN BIT 090H.0
5 SWD_PIN BIT 090H.1
6 SWD_PMOD_OC DATA 092H
7 SWD_PDIR_BU DATA 093H
8 P2 DATA 0A0H
9 ;Fn_MOD_OC Fn_DIR_BU
10 ; 0 0 Input
11 ; 0 1 FP_Output
12 ; 1 0 OC_Output
13 ; 1 1 OC_BU_Output
14
15 ?PR?SWD_Write_Byte?SW_DP_ASM SEGMENT CODE
16 ?PR?SWD_Write_Bits?SW_DP_ASM SEGMENT CODE
17 ?PR?SWD_IN_Sequence?SW_DP_ASM SEGMENT CODE
18 ?PR?SWD_Transfer?SW_DP_ASM SEGMENT CODE
19
20 EXTRN IDATA (data_phase)
21 EXTRN IDATA (idle_cycles)
22 ;EXTRN IDATA (turnaround)
23 PUBLIC __SWJ_Sequence
24 PUBLIC __SWD_IN_Sequence
25 PUBLIC __SWD_Transfer
26
27 ;ACC = data
28 ;R0 = Bits
29 RSEG ?PR?SWD_Write_Byte?SW_DP_ASM
30 SWD_Write_Byte:
31 MOV R0,#8
32 SWD_Write_Bits:
33 SETB SWC_PIN
34 RRC A
35 MOV SWD_PIN,C
36 CLR SWC_PIN
37 DJNZ R0,SWD_Write_Bits
38 SETB SWC_PIN
39 RET

```



Serial port optimization: The original serial port driver can only be said to have it, but there is basically no optimization. The CPU is waiting hard for serial port transmission, and packets are lost when the amount of data is large. After optimization, 256-byte xram is currently used to send large fifos through the serial port (the advantage of this is that 8 bits are enough for writing and writing pointers, and it is very simple to handle the full and empty fifos). The USB bandwidth for serial port reception is much higher than that of the serial port, so using a 64-byte cache is enough. When receiving serial port data, as long as there is a free USB endpoint, it will be thrown directly to the USB (basically 1-2 bytes will be sent once), and there is generally no pressure.

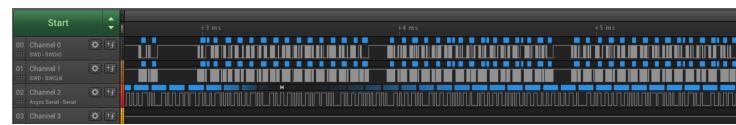
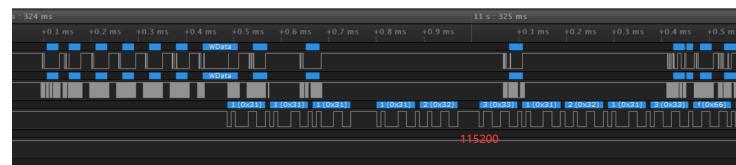
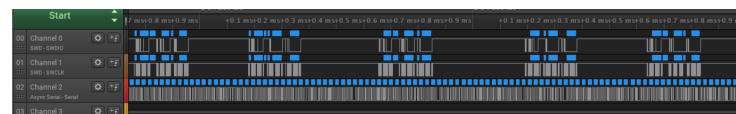
When sending serial port data larger than 256 bytes,

USB will send packets four times until the buffer is full.

When the USB packet is sent, the serial port interrupt will indeed be interrupted. In the future, the following interrupt nesting can be optimized to make the serial port priority higher.

However, the processing of fifo involves the possibility of two interrupts being accessed at the same time, and some hair needs to be lost.

You can see the status when swd and the serial port are working together. The baud rate is increased to 500000. If there is no USB interrupt that requires complicated processing, swd will not affect the serial port and the baud rate is reduced to 115200.



Hardware SPI optimization

uses hardware SPI to flush the fixed bytes of the SWD part. 8-bit command and 32-bit data can be directly switched to spi brush optimization. The proportion can reach $(8+32)/(8+5+32+1) \approx 87\%$. Since spi is used, the speed can be adjusted to 5V. Taking 24M clock speed as an example, the swd speed can be adjusted from 100KHz to 12MHz. Of course, only the spi brush part is adjusted, and the software part cannot be changed. 100K 1M is actually 6M. The 12M logic analyzer cannot capture it, but it can still communicate normally. I also played with the clock running at 32M clock speed and 16M clock speed, and there was no problem.

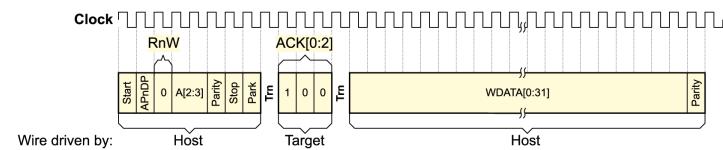


Figure B4-1 SWD successful write operation

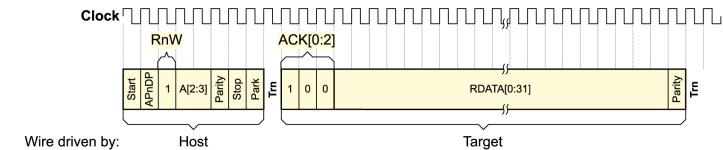
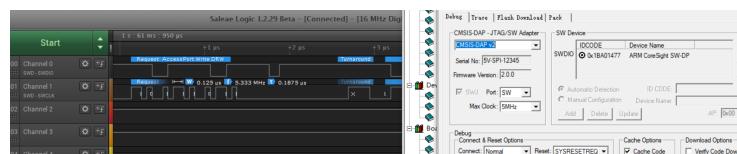
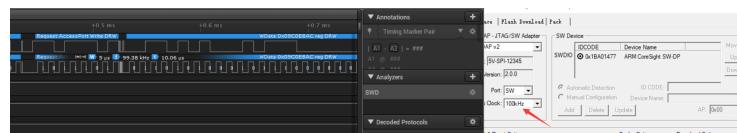


Figure B4-2 SWD successful read operation



The PCB project files and circuit diagrams are open sourced, and the code is open sourced for software simulation io. Because the spi hardware was refreshed, I found that the compatibility is not very good. I am a bit picky about the MCU, and sometimes errors are reported inexplicably, so I will go back and study it, so I won't do it now. Take it out to show your shame. Several compiled firmwares are provided for you to try. Welcome to find bugs and submit suggestions for improvements~
Commercial use is prohibited

Offline

2022-02-07 18:24:16

Share comments #1

mousebat04**member**

Registration time: 2020-04-26

Posts posted: 10

Points: 10

Boss is awesome! It simply benefits mankind. I hope it will become more useful in the future.

Also, I would like to ask, is the CH551 unable to install this firmware?

| | | |
|---|---|-----------------------------------|
| Offline | The original poster 2022-02-07 18:31:41 | Share comments #2 |
| posystorage member Registration time: 2018-05-06 Posted: 162 Points: 553 | mousebat04 said: Boss is awesome! It simply benefits mankind. I hope it will become more useful in the future. Also, I would like to ask, is the CH551 unable to install this firmware? I didn't set any restrictions. The size is only 8K and serial port 1 is not used. It should be no problem. | |
| Offline | 2022-02-07 19:20:38 | Share comments #3 |
| pla155 member Registration time: 2020-01-05 Posted: 3 Points: 3 | Big brother, learn from it for the benefit of mankind , please support me. | |
| Offline | 2022-02-07 19:32:01 | Share comments #4 |
| LingMao member Registration time: 2020-03-21 Posted: 1 Points: 1 | Another masterpiece from the boss, here comes Zi Ci. Using CH552E, the cost is lower and the size is smaller. | |
| Offline | 2022-02-07 22:13:43 | Share comments #5 |
| llinjupt member Registration time: 2020-12-21 Posts posted: 92 Points: 177 | Yes, CH552 is used as an onboard debugger at low cost. DAPLink's JTAG debugs FPGA? Does this need to be supported by the host computer, or should I implement a set of JTAG protocols for the FPGA in the debugger? | |
| Offline | The original poster 2022-02-08 01:47:20 | Share comments #6 |

posystorage**member**

Registration time: 2018-05-06
Posted: 162
Points: 553

Offline

Ilinjupt said:

Yes, CH552 is used as an onboard debugger at low cost. DAPLink's JTAG debugs FPGA? Does this need to be supported by the host computer, or should I implement a set of JTAG protocols for the FPGA in the debugger?

Just switch between using usbblaster+daplink. Use one button to switch.

2022-02-11 16:23:04 [Share comments #7](#)

Chin**member**

Registration time: 2020-10-19
Posts posted: 61
Points: 39

Offline

Oh my god, they are all bosses! How much does a set cost?

The original poster 2022-02-12 22:09:55 [Share comments #8](#)

posystorage**member**

Registration time: 2018-05-06
Posted: 162
Points: 553

Offline

Chin said:

Oh my god, they are all bosses! How much does a set cost?

No more than 10 yuan. This chip is very cheap (especially before the price increase)

2022-02-14 17:18:06 [Share comments #9](#)

Lexson**member**

Registration time: 2020-03-28
Posted: 1
Points: 6

[personal website](#)

Offline

The boss is too strong! I have a few pieces of CH554T that Lichuang bought many years ago. DS said that 554 only has more USB Host functions than 552/1. Is it possible to do this thing as well?

The original poster 2022-02-14 18:29:54 [#10](#)

[Share comments](#)

posystorage**member**

Registration time: 2018-05-06
 Posted: 162
 Points: 553

Offline

Lexsion said:

The boss is too strong! I have a few pieces of CH554T that Lichuang bought many years ago. DS said that 554 only has more USB Host functions than 552/1. Is it possible to do this thing as well?

You can use the same ones

2022-02-14 20:32:51

[Share comments](#) #11**echo****member**

Registration time: 2020-04-16
 Posts posted: 339
 Points: 343.5

Offline

The performance upper limit of CH552 is too low, and it is not cheap now.

2022-02-17 14:58:50

[Share comments](#) #12**taotieren****member**

Registration time: 2020-05-19
 Posts posted: 108
 Points: 148

Offline

Are there any plans to support rs-flash?

The original poster 2022-02-19 00:41:39

#13

[Share comments](#)**posystorage****member**

Registration time: 2018-05-06
 Posted: 162
 Points: 553

Offline

echo said:

The performance upper limit of CH552 is too low, and it is not cheap now.

The ch552e ssop10 package is still very fragrant. Install one on the development board to get the serial port + swd

The original poster 2022-02-22 00:46:54

#14

[Share comments](#)

posystorage**member**

Registration time: 2018-05-06

Posted: 162

Points: 553

Offline

taotieren said:

Are there any plans to support rs-flash?

What is this? I have never heard of it.

2022-02-22 15:29:33

Share comments #15**234336283****member**

Registration time: 2021-03-05

Posts posted: 8

Points: 8

Offline

Simple and practical, I don't know how fast the actual downloading experience is, especially when downloading large programs or H750 external Qflash

2022-02-22 21:03:33

Share comments #16**taotieren****member**

Registration time: 2020-05-19

Posts posted: 108

Points: 148

Offline

posystorage said:**taotieren said:**

Are there any plans to support rs-flash?

What is this? I have never heard of it.

<https://github.com/probe-rs/cargo-flash><https://github.com/probe-rs/probe-rs>

2022-02-22 22:18:28

Share comments #17

echo**member**

Registration time: 2020-04-16
Posts posted: 339
Points: 343.5

Offline

posystorage said:**echo said:**

The performance upper limit of CH552 is too low, and it is not cheap now.

The ch552e ssop10 package is still very fragrant. Install one on the development board to get the serial port + swd

My FPGA development board uses CH552T as the onboard USB-blaster, which can save an active crystal oscillator for the FPGA.

The original poster 2022-02-23 13:10:43

#18

[Share comments](#)**posystorage****member**

Registration time: 2018-05-06
Posted: 162
Points: 553

Offline

taotieren said:**posystorage said:****taotieren said:**

Are there any plans to support rs-flash?

What is this? I have never heard of it.

<https://github.com/probe-rs/cargo-flash>

<https://github.com/probe-rs/probe-rs>

I looked at it briefly, but I didn't quite understand it. Isn't this just a host computer software?

2022-03-01 14:57:36

[Share comments](#) #19**witty****member**

Location: Shenzhen
Registration time: 2022-03-01
Posted: 3
Points: 3

[personal website](#)

I plan to do it recently, otherwise I can only use ch549.

| | | |
|--|--|--|
| Offline | | |
| | 2022-03-02 09:54:50 | Share comments #20 |
| taotieren member Registration time: 2020-05-19 Posts posted: 108 Points: 148 Offline | @posystorage This is an open source schematic and PCB: https://github.com/probe-rs/hs-probe probe-rs uses rust to debug the firmware of embedded hardware, and cargo-flash is the host computer. | |
| | 2022-03-02 22:07:33 | Share comments #twenty one |
| bigbat member Registration time: 2022-01-30 Posts posted: 71 Points: 21 Offline | Is this CH552 a 51-core chip? | |
| | 2022-03-07 09:44:40 | Share comments #twenty two |
| kingsley_ch member Registration time: 2020-08-15 Posted: 2 Points: 2 Offline | Pay homage to the boss. I wanted to play with it before, but I always felt that 51 was weird. By the way, wch has recently released a lot of 144M MCUs with built-in USB high-speed PHY. Wouldn't it be much more fun to do this? .I asked Moxia on their website before about the high-speed and lowest configuration version, CH32V305, and they said it costs more than 8 yuan. I guess it can be cheaper in batches. <i>Recent editing records kingsley_ch (2022-03-07 09:53:31)</i> | |
| | 2022-03-07 11:33:23 | Share comments #twenty three |

gdddd**member**

Registration time: 2020-03-27

Posts posted: 30

Points: 30

Offline

posystorage said:**mousebat04 said:**

Boss is awesome! It simply benefits mankind. I hope it will become more useful in the future.

Also, I would like to ask, is the CH551 unable to install this firmware?

I didn't set any restrictions. The size is only 8K and serial port 1 is not used. It should be no problem.

The XRAM of CH551 is only 512B, so it cannot be used directly. I tried to change the absolute address and reduce the definition of XRAM, but it cannot be used after compilation. It mainly feels that there are some XRAM-related addresses in the program that are bound and I have not changed them.

Is it possible for posystorage to come up with a simplified version of the memory? Can it be adapted to the CH551?

2022-03-07 16:13:37

[Share comments](#) #twenty four**echo****member**

Registration time: 2020-04-16

Posts posted: 339

Points: 343.5

Offline

@gddddd

512kB XRAM is very frustrating, and CH551 has been discontinued

The original poster 2022-03-11 02:16:17

#25

[Share comments](#)**posystorage****member**

Registration time: 2018-05-06

Posted: 162

Points: 553

Offline

@gddddd

Maybe it's because some assembly codes are affected?
I'll look back when I have time

2022-03-15 00:07:31

[Share comments](#) #26

wh201906**member**

Registration time: 2021-12-09

Posts posted: 49

Points: 49

Offline

Excuse me, if you use SPI, do you need to use 2-wire half-duplex mode as the SWDIO port? Or use other methods to solve the two-way problem?

The original poster 2022-03-21 12:19:28

#27

[Share comments](#)**posystorage****member**

Registration time: 2018-05-06

Posted: 162

Points: 553

wh201906 said:

Excuse me, if you use SPI, do you need to use 2-wire half-duplex mode as the SWDIO port? Or use other methods to solve the two-way problem?

Using full-duplex SPI, two IOs are used together. There is a problem with the half-duplex SPI of ch552, and the speed is not the fastest.

Offline

2022-04-16 16:41:37

[Share comments](#) #28**Meski****member**

Registration time: 2022-04-16

Posted: 2

Points: 12

Offline

Sir, I tried to reproduce the pcb and found a contradiction. The readme suggested that P1.6 and P1.7 need to be connected in parallel, but in the schematic diagram, P1.6 and P1.5 pass through a 0 ohm resistor. Connected, I am very confused, is there something wrong with my understanding? I hope to get an answer, thank you.

The original poster 2022-04-17 01:25:14

#29

[Share comments](#)

posystorage**member**

Registration time: 2018-05-06
 Posted: 162
 Points: 553

Offline

Meski said:

Sir, I tried to reproduce the pcb and found a contradiction. The readme suggested that P1.6 and P1.7 need to be connected in parallel, but in the schematic diagram, P1.6 and P1.5 pass through a 0 ohm resistor. Connected, I am very confused, is there something wrong with my understanding? I hope to get an answer, thank you.

If the readme is written incorrectly, please refer to the schematic diagram.

2022-04-25 17:44:27

Share comments #30**JZH1996****member**

Registration time: 2019-09-25
 Posts posted: 9
 Points: 15

Offline

Boss, I burned the firmware you compiled. I can see a serial port and a CMSIS-DAP V2 device in the device manager, but it cannot be detected in Keil. I would like to ask whether I need to install a special driver or whether it depends on the Keil version. Request, my Keil is version 5.23

The original poster 2022-04-26 00:14:45

#31

Share comments**posystorage****member**

Registration time: 2018-05-06
 Posted: 162
 Points: 553

Offline

JZH1996 said:

Boss, I burned the firmware you compiled. I can see a serial port and a CMSIS-DAP V2 device in the device manager, but it cannot be detected in Keil. I would like to ask whether I need to install a special driver or whether it depends on the Keil version. Request, my Keil is version 5.23

The keil version is too old and cannot recognize the v2 version of daplink. Upgrade keil or replace the dll file in CMSIS_DAP.zip under Keil_mdk_c51\ARM\BIN.

2022-05-02 13:54:50

Share comments #32

Leng Yueyan**member**

Registration time: 2020-07-06

Posts posted: 39

Points: 46.5

Offline

Sir, I tried this compiled firmware. The serial port is unstable. It is powered by 3.3V and has a baud rate of 115200. The serial port receives very bad bit errors.

2022-05-02 21:57:29

[Share comments #33](#)**Meski****member**

Registration time: 2022-04-16

Posted: 2

Points: 12

Offline

Boss, I finished it, but encountered some small problems. I adopted the 5VIO solution, and then used SN74LVC1T45DCKR to convert it to 3.3VIO. The computer and Keil can recognize the Daplink device, but it shows SWD/JTAG Communication Failure and cannot be found. to the device ID, and then I suspected that the level conversion might not work. After confirming that my SWD interface supports 5V level input, I removed the level conversion and directly connected the wires to the pin headers of CLK and DIO. The ID was read out, but it failed. Cannot Load Flash Programming Algorithm is displayed. I tried changing the computer or reducing the download rate but it still failed to solve the problem. I would also like to thank you if you have the time to analyze the possible reasons. I would be very grateful.

2022-05-03 00:11:06

[Share comments #34](#)**health****member**

Registration time: 2021-02-23

Posts posted: 20

Points: 44.5

Offline

Leng Yueyan said:

Sir, I tried this compiled firmware. The serial port is unstable. It is powered by 3.3V and has a baud rate of 115200. The serial port receives very bad bit errors.

The 3.3V power supply cannot produce a baud rate of 115200bps.

The original poster 2022-05-03 03:55:36

#35

[Share comments](#)

posystorage**member**

Registration time: 2018-05-06
Posted: 162
Points: 553

Offline

Leng Yueyan said:

Sir, I tried this compiled firmware. The serial port is unstable. It is powered by 3.3V and has a baud rate of 115200. The serial port receives very bad bit errors.

The main frequency is only 16MHz under 3.3V, and the baud rate of Fsys / 16 / running 115200 has a very large deviation.

The baud rate should be 111111

The original poster 2022-05-03 03:56:27

#36

[Share comments](#)**posystorage****member**

Registration time: 2018-05-06
Posted: 162
Points: 553

Offline

@Meski

Cannot Load Flash Programming Algorithm This is a problem with your keil settings. It has nothing to do with daplink. This is because the download algorithm is not set.

2022-05-23 16:45:57

[Share comments](#) #37**jk****member**

Registration time: 2022-05-23
Posted: 2
Points: 2

Offline

Sir, I have also copied it. It is powered by 5V, serial port and download are OK, but debugging is not working. Is it a problem with my settings, or is the firmware not perfect with debug function?

2022-05-23 18:21:39

[Share comments](#) #38**jk****member**

Registration time: 2022-05-23
Posted: 2
Points: 2

Offline

Sir, I have discovered a new problem. It is normal to download small files. However, when downloading large files (such as 14K), a verification error will be prompted.

2022-05-27 10:15:18

[Share comments](#) #39

Vans000**member**

Registration time: 2022-01-04

Posts posted: 10

Points: 5

Offline

There should be no problem with burning after using it now, but the serial port feels not very stable and data loss is serious.

2022-06-16 17:37:05

[Share comments #40](#)**nick_zm****member**

Registration time: 2022-06-16

Posted: 2

Points: 2

Offline

Thanks for sharing the source code. I searched for it on Baidu and it took no effort to bring it up.

2022-06-26 16:12:54

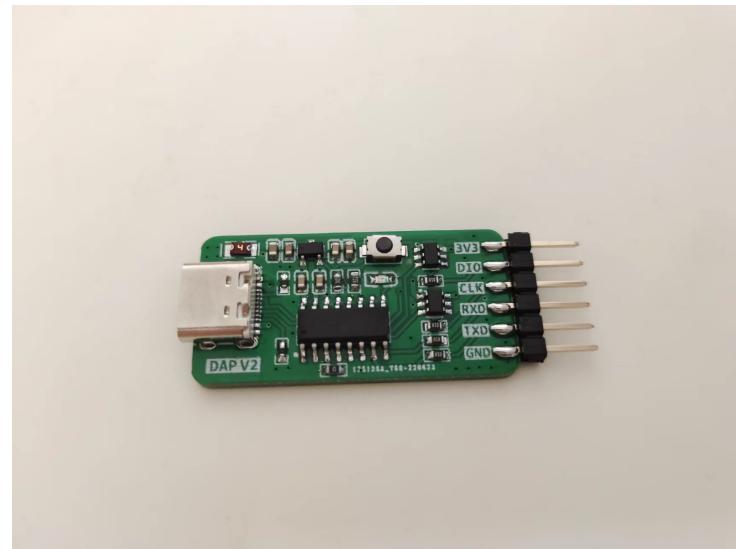
[Share comments #41](#)**jdsuchen****member**

Registration time: 2022-06-19

Posted: 2

Points: 2

Thanks for sharing. I made one. It is very fast. It takes 1 second to read STM32F030C8T6 with UnionPRG and 9 seconds with WCH-LINK.



Offline

2022-06-27 12:46:36

[Share comments #42](#)

Sea rocks create wind

member



Location: Shenzhen

Registration time: 2019-07-02

Posts posted: 457

Points: 576

[personal website](#)

Offline

Further optimization directions for CMSIS-DAP are:

- * Switch to a master control with larger RAM, higher frequency, and support HS USB;
- * Use pure hardware SPI to implement the SWD interface (for example: Nuvoton has MCU SPI that can send and receive Very byte-aligned data);
- * Implement smart writing: if the content of a sector or page on the chip is consistent with what is to be written, the writing of this area will be skipped.

2022-06-28 16:22:30

[Share comments #43](#)

jdsuchen

member

Registration time: 2022-06-19

Posted: 2

Points: 2

I tried STM32F407VET6 and had some problems.

Occasionally, I couldn't debug it even after connecting to it. WCH-LINK also had the same problem.

Info : Listening on port 6666 for tcl connections

Info : Listening on port 4444 for telnet connections

Info : Using CMSIS-DAPv2 interface with

VID:PID=0x0d28:0x0204, serial=5V0-IO-12345

Info : CMSIS-DAP: SWD Supported

Info : CMSIS-DAP: FW Version = 2.0.0

Info : CMSIS-DAP: Interface Initialised (SWD)

Info : SWCLK/TCK = 1 SWDIO/TMS = 1 TDI = 0 TDO = 0 nTRST = 0 nRESET = 1

Info : CMSIS- DAP: Interface ready

Info: clock speed 10000 kHz

Error: Error connecting DP: cannot read IDR

Offline

2022-06-28 21:23:19

[Share comments #44](#)

Shanghai Hangxin Mar...**member**

Registration time: 2022-06-23

Posts posted: 44

Points: 139

The DAP-Link made using Hangxin's ACH512 with HS

USB has been put on the whycan Taobao store

<https://item.taobao.com/item.htm?spm=a1z10.3-cs.w4002-24455499472.11.77c6526cEQ21jK&id=677891191502>

Original factory meeting Cooperate with whycan to supply DAP-Link at a long-term low price (within 30RMB)

Serial port 921600 baud rate, download 480KB firmware to ACM32FP4, speed comparison:
other 70+RMB daplink: 16s
ACH512-dap: 14.5sSWD downloads 63KB firmware to ACM32FP4, speed comparison:
other 70+RMB daplink-10M: 3.6s
ACH512-dap-10M: 5s*Recently edited record Shanghai Hangxin Market (2022-06-28 21:25:16)*

Offline

2022-07-18 22:59:30

Share comments #46**cuit4017****member**

Registration time: 2022-07-18

Posted: 1

Points: 1

jdsuchen said:Thanks for sharing, I made one, it is very fast. It takes 1 second to read STM32F030C8T6 with UnionPRG, and 9 seconds with WCH-LINK
https://whycan.com/files/members/9626/WeChat%20picture_20220626161156.jpg

Are you open source? I want to get a typec port.

Offline

2022-07-20 17:23:15

Share comments #47**Vans000****member**

Registration time: 2022-01-04

Posts posted: 10

Points: 5

Offline

You guys are very good. I am also using ljbfly's code and found out that it uses serial port 1. When I came back to build the board, I found that serial port 1 had too big an error when the power supply was 3.3V.

2022-08-02 20:08:37

Share comments #48

xiao_fang**member**

Registration time: 2022-08-02

Posted: 3

Points: 4

Offline

Thanks to the author for sharing the source code. I am learning USB these days and plan to transplant it to CH583. The next step is to use Bluetooth to make a wireless DAP.

The original poster 2022-08-11 00:51:05

#49

[Share comments](#)**posystorage****member**

Registration time: 2018-05-06

Posted: 162

Points: 553

Offline

xiao_fang said:

Thanks to the author for sharing the source code. I am learning USB these days and plan to transplant it to CH583. The next step is to use Bluetooth to make a wireless DAP.

Support you, SWD speed optimization recommends that you rewrite the official original SWD timing code

2022-08-28 11:13:06

[Share comments](#) #50

EListen**member**

Registration time: 2021-08-25

Posted: 3

Points: 33

I found a problem. In the poster's code, endpoint 1, endpoint 2, and endpoint 3 are allocated a buffer of 64*4, which is 256 bytes.

```
UINT8X Ep0Buffer[THIS_ENDP0_SIZE] _at_ 0x0000;
UINT8X Ep1Buffer0[THIS_ENDP0_SIZE] _at_ 0x0040;
UINT8X Ep1BufferI[THIS_ENDP0_SIZE] _at_ 0x0080;
//100,140,180,1C0
UINT8X Ep2Buffer0[4 * THIS_ENDP0_SIZE] _at_ 0x00C0;
//200,240,280,2C0
UINT8X Ep3BufferI[4 * THIS_ENDP0_SIZE] _at_ 0x0100;
```

◀ ▶

But when it comes to the actual configuration, all configurations are single buffer configurations.

```
UEP2_DMA = Ep2Buffer0;
UEP3_DMA = Ep3BufferI;
UEP2_3_MOD |= (bUEP3_TX_EN | bUEP2_RX_EN);
UEP2_3_MOD &= ~(bUEP2_BUF_MOD | bUEP3_BUF_MOD);
UEP2_CTRL = bUEP_AUTO_TOG | UEP_T_RES_NAK | UEP_T_RES_STALL;
UEP3_CTRL = bUEP_AUTO_TOG | UEP_T_RES_NAK | UEP_T_RES_STALL;
```

◀ ▶

If there is no correctness in the manual, adding the configuration of endpoint 1 can save 512 bytes of external ram according to the actual full single buffer configuration.

In addition, it seems that endpoint 4 is configured, but this is disabled during the actual endpoint initialization.
I'm still checking

Offline

The original poster 2022-08-28 17:22:33

#51

[Share comments](#)**posystorage****member**

Registration time: 2018-05-06

Posted: 162

Points: 553

Offline

@EListen

Endpoints 2 and 3 should be the serial port cache buff, using 256 bytes of space for fifo. You will find out if you look at the assembly part.

2022-08-28 18:08:18

[Share comments](#) #52

EListen**member**

Registration time: 2021-08-25

Posted: 3

Points: 33

posystorage said:

@EListen

Endpoints 2 and 3 should be the serial port cache buff, using 256 bytes of space for fifo. You will find out if you look at the assembly part.

If I understand correctly, you should have opened up a separate buffer and specified the segment address.
It is quite dangerous to mix USB buff and serial port buff.

```
UINT8X Ep0Buffer[THIS_ENDP0_SIZE] _at_ 0x0000;  
UINT8X Ep1Buffer0[THIS_ENDP0_SIZE] _at_ 0x0040;  
UINT8X Ep1BufferI[THIS_ENDP0_SIZE] _at_ 0x0080;  
  
//100,140,180,1C0  
UINT8X Ep2Buffer0[4 * THIS_ENDP0_SIZE] _at_ 0x0:  
//200,240,280,2C0  
UINT8X Ep3BufferI[4 * THIS_ENDP0_SIZE] _at_ 0x0:  
  
UINT8I UART_RX_Data_Buff[ENDP1_SIZE];  
UINT8X UART_TX_Data_Buff[256] _at_ 0x0300;
```



I plan to rewrite the daplink of ch552. I want to add it to the system of rtx51tiny. I'll take a closer look. If you look at it, you should be able to cut off a lot of buffers for usb.

Offline

The original poster 2022-08-29 11:40:33

#53

[Share comments](#)

posystorage

member

Registration time: 2018-05-06
Posted: 162
Points: 553

@EListen

I kind of forgot about it after a long time. I took a look and it turns out that the EP1 cache is a buffer used by the serial port, and each uses 64 bytes for sending and receiving.

Main_Usb.C

```
UINT8X Ep1Buffer0[THIS_ENDP0_SIZE] _at_ 0x0040;
UINT8X Ep1BufferI[THIS_ENDP0_SIZE] _at_ 0x0080;
```



There are two buffers under the serial port file. The internal one is the RX buffer, 64 bytes, and the external one is the TX buffer, 256 bytes.

Uart.c

```
UINT8I UART_RX_Data_Buff[ENDP1_SIZE];
UINT8X UART_TX_Data_Buff[256] _at_ 0x0300;
```

void UART_Get_USB_Data(UINT8 Nums) is responsible for moving Ep1Buffer0 to the sending fifo UART_TX_Data_Buff.

void memcpy_TXBUFF_USBBUFF(UINT8 data_len) is responsible for moving UART_RX_Data_Buff to Ep1BufferI.

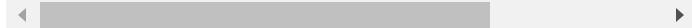
The buffers in this part of the serial port are not mixed.

EP2 is the PC that sends DAP data to CH552.

The cache here is used like this. When it is full, it will directly +64

Main_Usb.C

```
case UIS_TOKEN_OUT | 2: //endpoint 2# 端
    if (U_TOG_OK)           // 不同步的数据
    {
        Ep20i += 64;
        UEP2_DMA_L = Ep20i;
    }
    break;
```



The same is true for EP3, just change the cache, so you don't have to wait for the USB

```
Main_Usb.C
    if (Endp3Busy != 1 && Ep3Ii != Ep3Io)
    {
        Endp3Busy = 1;
        UEP3_T_LEN = Ep3Is[0];//Ep3Io>>6];
        UEP3_DMA_L = Ep3Io;

        UEP3_CTRL = UEP3_CTRL & ~MASK_UEP_T_
        Ep3Io += 64;
    }
```



Here is the use of FIFO cache

```
DAP.c
void DAP_Thread(void)
{
    UINT8I num;

    if (Ep20i != Ep20o)
    {
        PUINT8 req = &Ep2Buffer0[Ep20o];
        PUINT8 res = &Ep3BufferI[Ep3Ii];
        Ep20o += 64;
        .....
        Ep3Is[0]/*(Ep3Ii>>6)]*/ = num + 1;
        Ep3Ii += 64;
    }
}
```

Offline

2022-08-30 18:36:43

[Share comments #54](#)

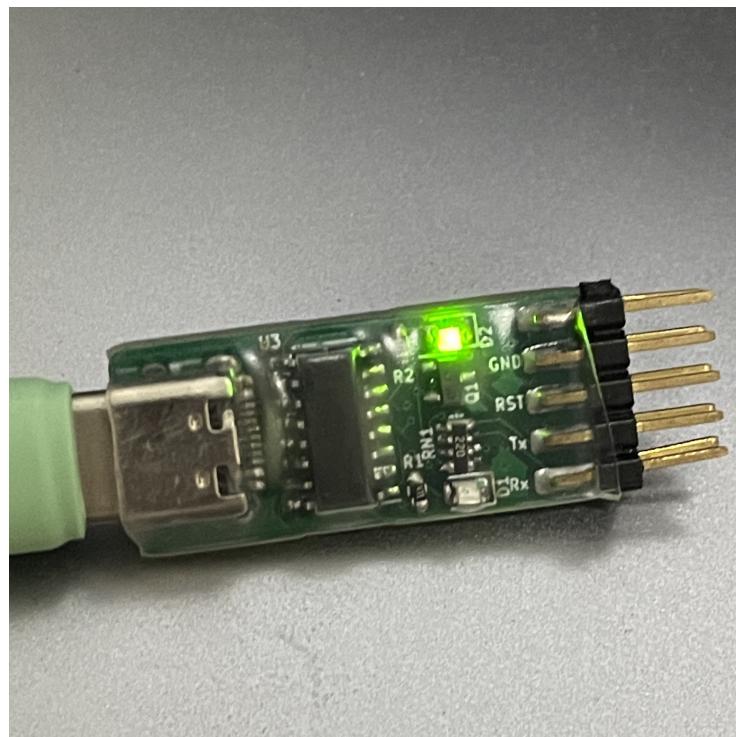
abgelehnt**member**

Registration time: 2022-05-01

Posts posted: 10

Points: 110

Thanks for sharing, I made a typec version 😊



Offline

2022-08-30 18:50:33

[Share comments](#) #55**EListen****member**

Registration time: 2021-08-25

Posted: 3

Points: 33

Offline

@posystorage

Sorry, I understand the buffer settings when calling DAP, but these buffer settings are a bit confusing. Also, does DAP really need to send and receive buffers of 256 bytes each? I currently plan to use the dual buffer mode supported by USB peripherals to try it out. It should be enough

2022-09-02 19:17:24

[Share comments](#) #56**abgelehnt****member**

Registration time: 2022-05-01

Posts posted: 10

Points: 110

Offline

I feel like there is no need for such a large buffer. The original poster probably wrote this for ease of compilation. The DPH is fixed directly. However, the XRAM is not used in vain, right hhh

The original poster 2022-09-04 04:11:42

#57

[Share comments](#)

posystorage

member

Registration time: 2018-05-06
Posted: 162
Points: 553

Offline

abgelehnt said:

I feel like there is no need for such a large buffer. The original poster probably wrote this for ease of compilation. The DPH is fixed directly. However, the XRAM is not used in vain, right hhh

Haha, you discovered that I was lazy in assembly. You are right, and this part of the code was used in other projects before. I just moved it over and was lazy.

2022-11-17 22:27:41

[Share comments #58](#)

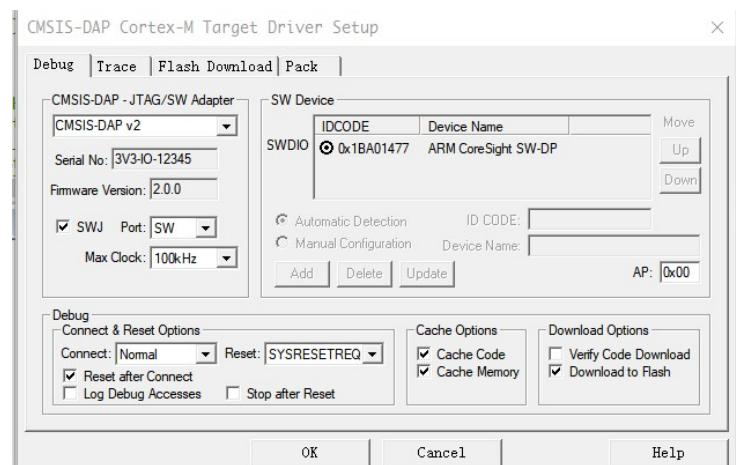
815794369

member

Registration time: 2020-02-16
Posts posted: 9
Points: 22.5

In actual testing, it is not very stable in a 3.3V environment. The download failed 9 times out of 10 times. After failure, the following error was reported. You need to disconnect and reconnect both ch552 and stm32 before downloading. Please help me take a look

```
Build started: Project: STM32F103C8TX_TEMPLET
*** Using Compiler 'V6.12', folder: 'C:\Keil_v5\ARM\ARMCLANG\Bin'
Build target 'STM32F103C8TX_TEMPLET'
"STM32F103C8TX_TEMPLET\STM32F103C8TX_TEMPLET.axf" - 0 Error(s), 0 Warning(s).
Build Time Elapsed: 00:00:00
Load "STM32F103C8TX_TEMPLET"\STM32F103C8TX_TEMPLET.axf"
RDDI-DAP Error
Error: Flash Download failed - Target DLL has been cancelled
Flash Load finished at 21:56:14
```



Offline

2022-11-17 22:57:26

[Share comments #59](#)

815794369

member

Registration time: 2020-02-16
Posts posted: 9
Points: 22.5

The actual test found that it is enough to connect the 3.3V of the target board and the power supply of ch552. The specific reason is very confusing

| | | |
|---|--|---------------------------------------|
| Offline | The original poster 2022-11-18 01:58:22 | #60 Share comments |
| posystorage member Registration time: 2018-05-06 Posted: 162 Points: 553 Offline | @815794369 Such little information is not enough to analyze the problem. This can only be easily seen by capturing the swd+usb packet. By the way, have you tested whether it can work stably under 5V? | |
| | 2022-11-22 19:22:27 | Share comments #61 |
| 815794369 member Registration time: 2020-02-16 Posts posted: 9 Points: 22.5 Offline | I didn't test 5V and I didn't draw 1T45 on my board. | |
| | 2022-11-22 19:25:30 | Share comments #62 |
| 815794369 member Registration time: 2020-02-16 Posts posted: 9 Points: 22.5 Offline | After seeing this post (https://whycan.com/t_6042.html), a big boss said, "In addition, nerdralph reported that CH552 cannot be used when connected to HK32F with Dupont cable. The reason is that the ringing is too large and the clock is wrong. CH552 cannot control the slew rate, so a 50-150Ohm resistor should be connected in the middle of the SWD for matching to eliminate ringing." I connected a 100R resistor in series to the swd. In actual testing, I found that the download failure rate was much smaller, but it could not be debugged. "Cannot access target Shutting down debug session" will be reported. | |
| | The original poster 2022-11-22 20:22:58 | #63 Share comments |
| posystorage member Registration time: 2018-05-06 Posted: 162 Points: 553 | @815794369 I think the ringing is mainly caused by bad Dupont wires and imperfect grounding shielding. It is recommended not to tear the Dupont wires. | |

| | | |
|--|---|---------------------------------------|
| Offline | | |
| | 2023-06-02 16:57:38 | Share comments #64 |
| foticing member Registration time: 2023-06-02 Posted: 1 Points: 1 Offline | What is the situation when CH552 cannot download STM32? | |
| | The original poster 2023-06-02 17:09:30 | #65 Share comments |
| posystorage member Registration time: 2018-05-06 Posted: 162 Points: 553 Offline | foticing said: What is the situation when CH552 cannot download STM32? It's OK for me to test here. Why don't you see if it works at low speed? | |
| | 2023-06-25 23:17:15 | Share comments #66 |
| andyxu member Registration time: 2023-06-25 Posted: 1 Points: 1 Offline | @posystorage When the original poster connected the downloader alone and did not connect to 32, when checking the downloader status in Keil, did the RDDI-DAP Error appear in the debugger settings? | |
| | The original poster 2023-07-03 12:28:39 | #67 Share comments |
| posystorage member Registration time: 2018-05-06 Posted: 162 Points: 553 Offline | andyxu said: @posystorage When the original poster connected the downloader alone and did not connect to 32, when checking the downloader status in Keil, did the RDDI-DAP Error appear in the debugger settings? Send a screenshot to see. Can it be used when connecting to stm32? | |

| | | |
|---|--|---|
| | 2024-01-03 23:02:38 | Share comments #70 |
| flex-A member  Registration time: 2019-08-27 Posts posted: 48 Points: 153.5 Offline | Boss, if the resources of ch551/552 are enough, can you also use a chip like cy7c68013/cbm9002 to get a downloader? | |
| | The original poster 2024-01-04 02:13:26 | #71 Share comments |
| posystorage member Registration time: 2018-05-06 Posted: 162 Points: 553 Offline | flex-A says: Boss, if the resources of ch551/552 are enough, can you also use a chip like cy7c68013/cbm9002 to get a downloader? I guess it's ok? | |
| | 2024-01-04 08:52:17 | Share comments #72 |
| mcujishu member Registration time: 2024-01-03 Posts posted: 4 Points: 4 Offline | Where are the source code examples of CH552? | |
| | 2024-01-18 11:46:48 | Share comments #73 |
| Mox_Q member Registration time: 2023-09-05 Posted: 1 Points: 1 Offline | Can you please add a debugging function? :D | |
| | 2024-01-19 11:05:05 | Share comments #74 |

zydl123**member**

Registration time: 2022-10-22

Posted: 3

Points: 3

Offline

I have also made several kinds of ch552, DAPLink's JTAG debugging FPGA? No

Page: 1

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