

Design of Digital Systems Laboratory

Assignment Lab 1

Brian Ryner

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: Brian Ryner

SYNOPSIS

LAB1 MAPS INPUT SWITCHES TO OUTPUT LEDs USING 4 DIFFERENT DESIGN TECHNIQUES. THIS GIVES A DEMONSTRABLE VIEW OF HOW THE SAME DESIGN CAN BE IMPLEMENTED USING DIFFERENT METHODS WHETHER IT BE BEHAVIORAL, DATAFLOW, OR LUT PRIMITIVES. USING A TOP LEVEL COMPARATOR, THE INPUT SWITCHES ARE TIED TO THE INPUT OF EACH DIFFERENT DESIGN TECHNIQUE AND IF THEY ALL MATCH, SHOULD RESULT IN A POSITIVE LED OUTPUT.

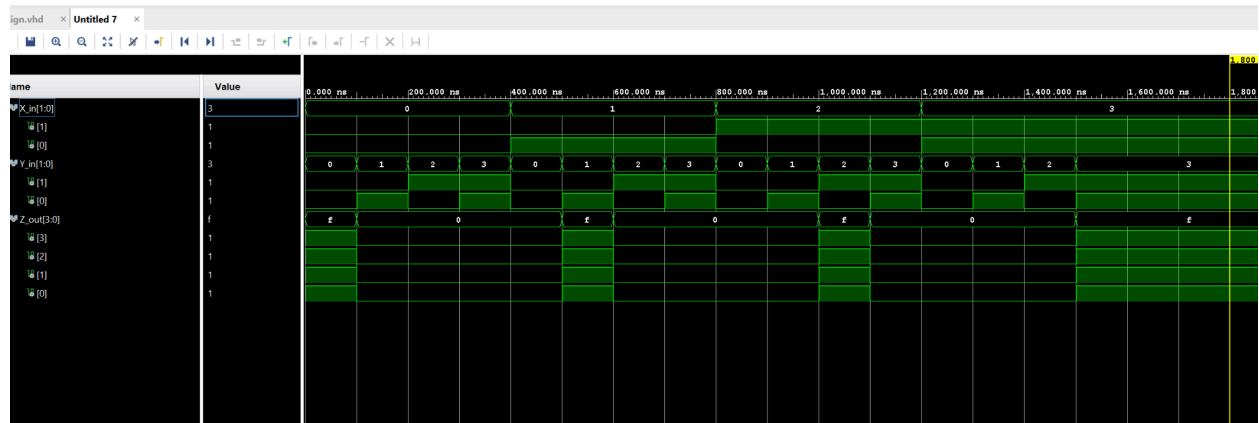
INITIALLY, WE ARE TASKED WITH FINDING THE CORRECT VALUES FOR THE INIT TABLE CORRESPONDING TO THE LUT IMPLEMENTATION. RENAMING THE INPUTS AND DESIGNING FOR A 2 BIT, 2 INPUT LUX, WHERE Z_OUT IS $X = Y$, GIVES THE FOLLOWING RESULT.

Table 1: INIT Table

X ⁰	X	Y ¹	Y	Z ²	Z _{out}	INIT
0	0	0	0	0	0	0000 = 0
0	0	0	1	0	0	
0	0	1	0	0	0	
0	0	1	1	0	0	
0	1	0	0	0	0	0000 = 0
0	1	0	1	0	0	
0	1	1	0	0	0	
0	1	1	1	0	0	
1	0	0	0	0	0	0000 = 0
1	0	0	1	0	0	
1	0	1	0	0	0	
1	0	1	1	0	0	
1	1	0	0	0	0	1000 = 8
1	1	0	1	0	0	
1	1	1	0	0	0	
1	1	1	1	1	1	

x8421

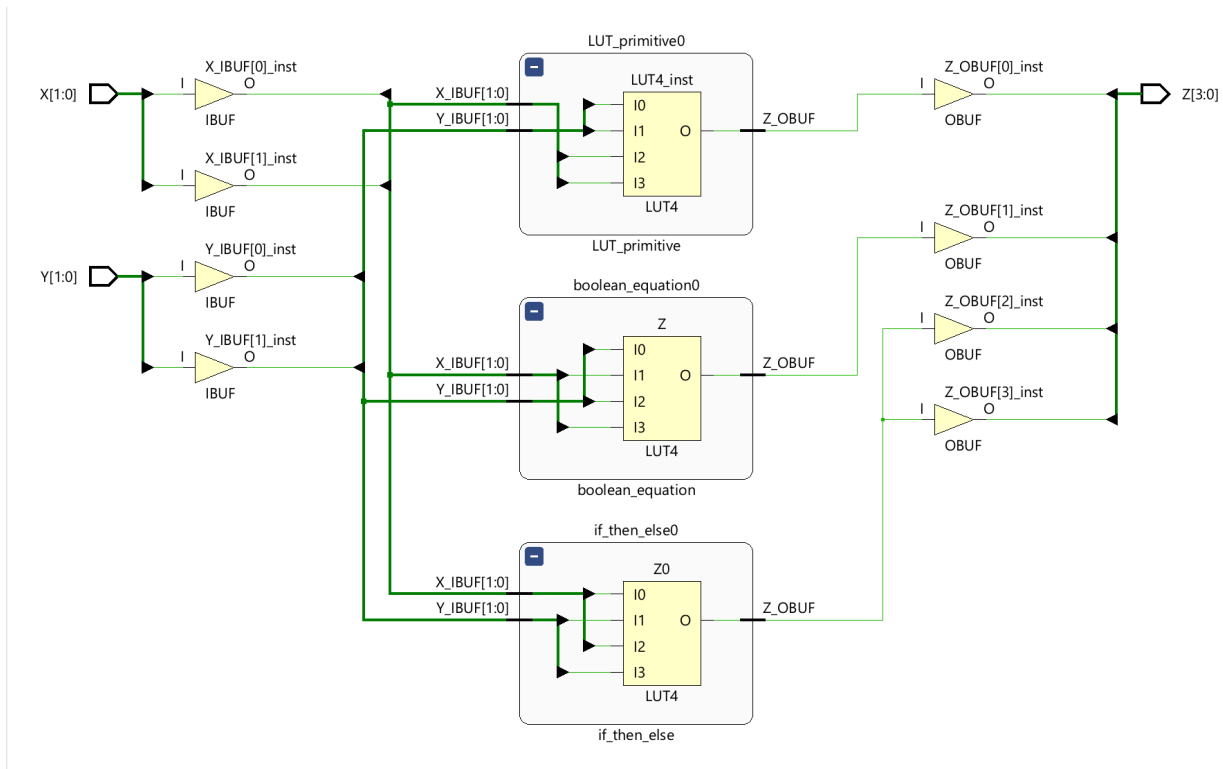
WAVEFORM



DEMONSTRATED IN THE WAVEFORM DIAGRAM ABOVE, WE SEE THE CLOCK CYCLE BEING EVERY 10 nS. OUR SIM IS SUCH THAT THE INPUT VALUES FOR EACH OF THE 4 BITS CHANGE AT A DIFFERENT RATE WITH THE LOWEST BIT VALUE CHANGING EVERY 100 nS AND THE HIGHEST BIT VALUE CHANGING EVERY 800mS. THIS GIVES A TOTAL CYCLE TIME OF 1600nS.

ON THE Z BUS, WE SEE THAT Z IS HIGH WHEN BOTH x0 AND y0 ARE THE SAME AND x1 AND y1 ARE THE SAME. THIS GIVES US THE CORRECT OUTPUT FOR A 2 INPUT, 2 BIT COMPARATOR.

IMPLEMENTATION



VIDEO DEMONSTRATION

[Lab1](#)

FILENAMES

DESIGN.VHD = DESIGN

SIM.VHD= SIMULATION

BLACKBOARD_REV D.XDC = **BLACKBOARD** CONSTRAINT FILE

NEXYS-4-DDR-MASTER.XDC = **NEXYS** CONSTRAINT FILE

LAB1_REPORT.DOCX

(RUNNING AS A REMOTE STUDENT ON A DIFFERENT XILINX BOARD SO A DIFFERENT CONSTRAINT FILE IS NECESSARY FOR MY IMPLEMENTATIONS. I WILL BE PROVIDING THAT AS WELL AS THE COMPATIBLE NEXYS CONSTRAINT FILE IF VERIFICATION IS NECESSARY ON YOUR END.)

FINDINGS AND OBSERVATIONS

A COUPLE TYPOS IN MY CODE HAD THROWN OFF MY IMPLEMENTED DESIGN FOR A FEW DAYS. FINALLY AFTER REVIEWING THE SIMULATED RESULTS, I WAS ABLE TO MAKE SENSE OF IT AND SEE WHICH BIT ON THE Z BUS WAS NOT GENERATING THE CORRECT RESPONSE. THIS MADE IT EASIER TO REVIEW THE HDL CODE AND MAKE THE NECESSARY ALTERATIONS. BELOW ARE SNIPPETS FROM SAID RUNS. THE FIRST SCREENSHOT SHOWS Z0 GOING HIGH 4 TIMES OVER THE 1600NS CYCLE, HOWEVER THE 2 MIDDLE BITS ARE INCORRECT. THIS LEAD ME TO REVIEWING THE LUT CODE AND SWITCHING THE TWO INPUTS ON THAT LUT TO CORRECT IT.

