**Design of Digital Systems Laboratory**

**Assignment Lab 0**

Brian Ryner

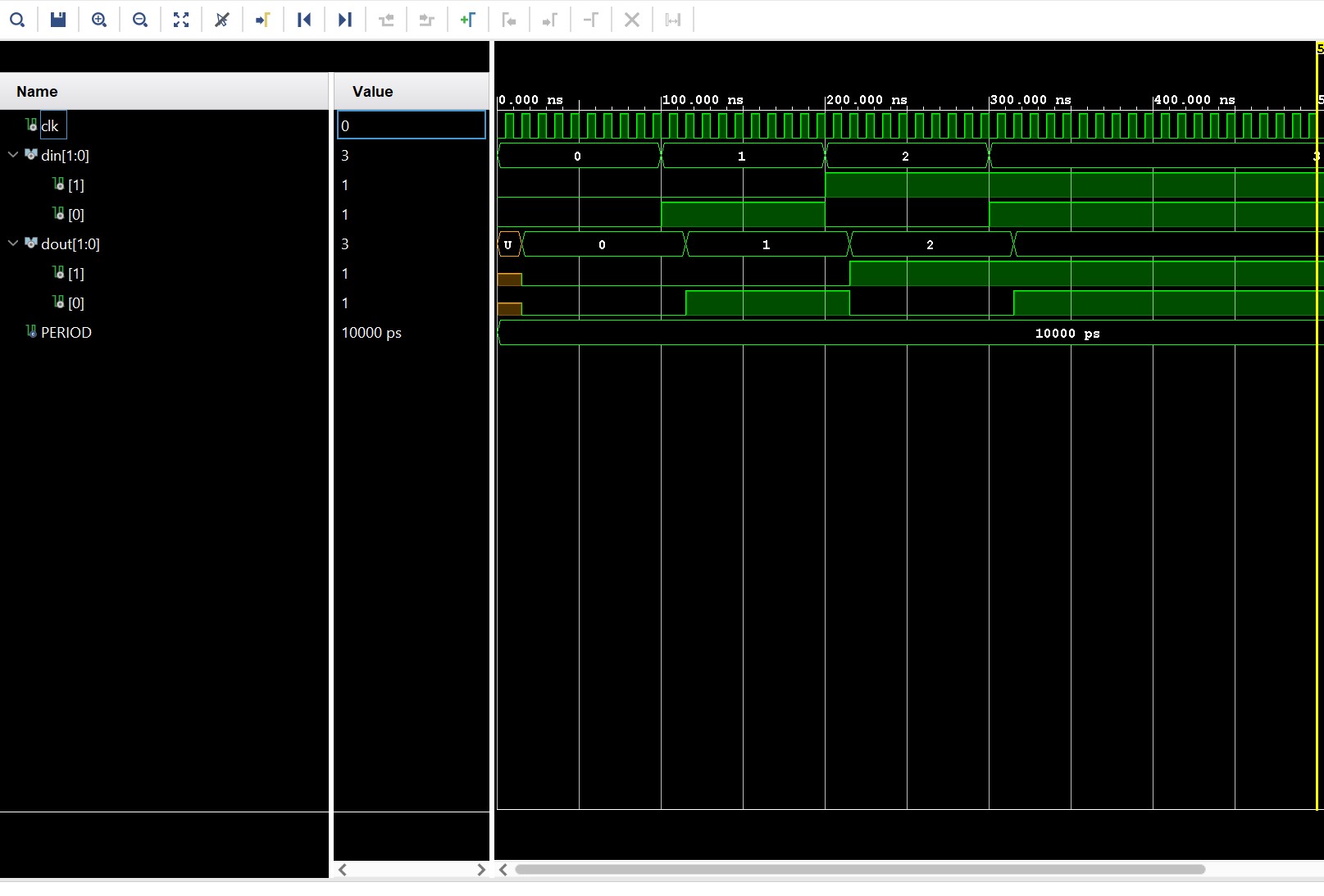
By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

|  |  |
| --- | --- |
| Your Signature: | Brian Ryner |

**Synopsis**

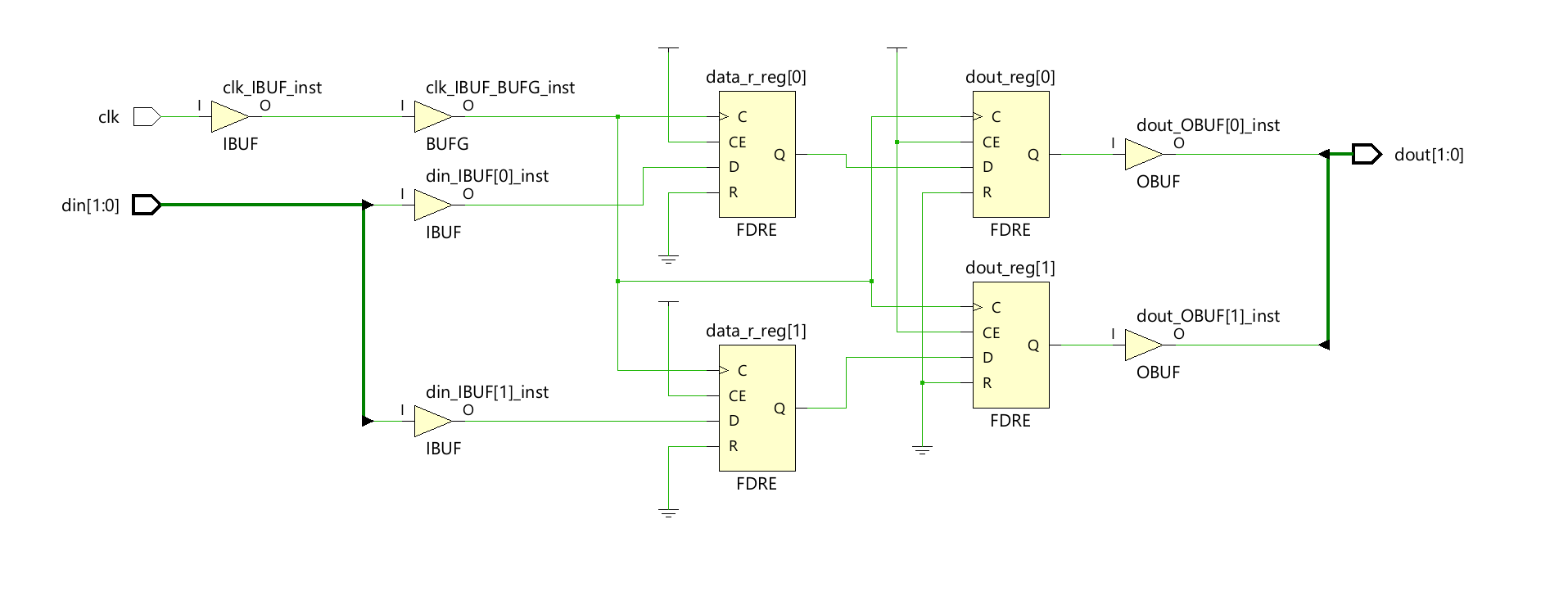
The goal of this initial lab is to introduce us to the xilinx test suite through simple hardware design in which two switches will control the output of two corresponding LEDs. For the purpose a simulating our design, an accompanying testbench is provided as well as instructions for place and route as well as deployment of our bitstream file to the hardware board. We will learn the basics of simulation and synthesizing HDL code as well as how to target to specific devices through device specific constraint files which map our ports to physical pins on the FPGA.

**Waveform**

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Demonstrated in the waveform diagram above, we see the clock cycle being every 10 nS. Our Testbench is written such that the Din values change every 100 nS beginning with an input of 00 representing decimal 0 upto 11 – decimal 3.

**Implementation**

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**Area**

|  |  |
| --- | --- |
| LUTs | 0 |
| FFs | 4 |

**Timing**

|  |  |  |
| --- | --- | --- |
|  | **Blackboard** | **Nexys4DDR** |
| Worst Negative Slack | 8.881 | 8.932 |
| Critical Path Delay | 10 – WNS = **1.119** | 10 – 8.932 = **1.068** |
| Maximum Frequency | 1000/CPD = **893.65 MHz** | 1000/1.068 = **936.33 MHz** |

**Video Demonstration**

[Lab 0](https://youtu.be/k4tWwGe6gUs)

**Filenames**

lab0\_design = design

lab0\_sim = simulation

blackboard\_revD.xdc = **blackboard** constraint file

Nexys-4-DDR-Master.xdc = **Nexys** constraint file (from the digilent github with additional lines supporting our naming conventions outlined in the lab0 instructions.)

(running as a remote student on a different xilinx board so different constraint file is necessary for my implementations. I will be providing that as well as the compatible Nexys constraint file if verification is necessary on your end.)

**Findings and Observations**

What I found interesting is the difference in maximum frequency and slack when targeting for different boards. Particularly the Nexys supporting an FPGA design of an older architecture able to run 40 MHz faster than the zinq 7000 chip on my blackboard fpga.